SUCCESSIVE APPROXIMATION ADCS

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WHAT IS A SUCCESSIVE APPROXIMATION ADC?

- Analog-to-digital signal converter
  - Requires a sampling rate under 10x10^6 samples per second or 10MSPS
- Great for 8-16 bits: higher possible but limited by resolution of DAC

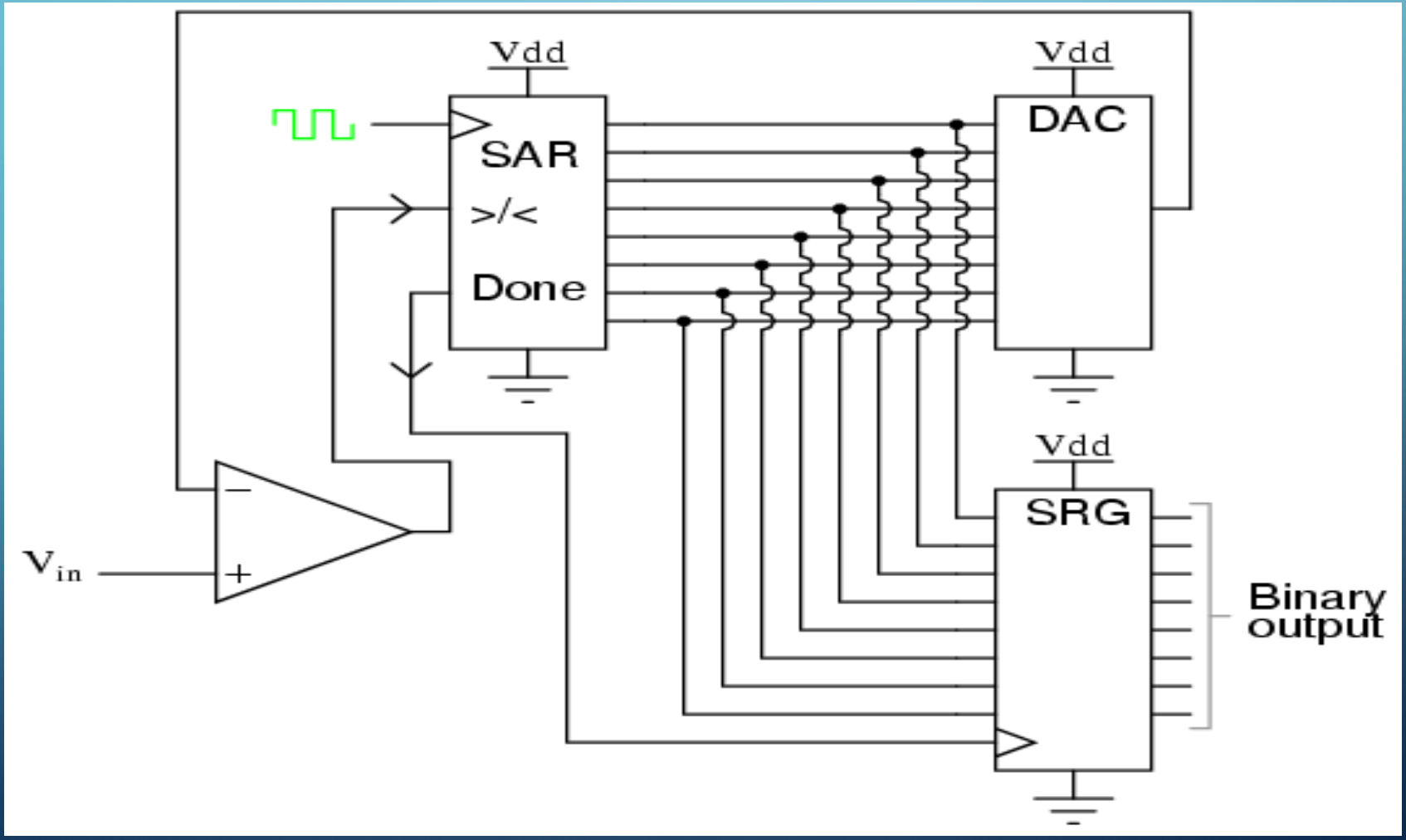
HOW DOES IT WORK?

- Uses a counter circuit, called a SAR (Successive Approximation Register).
- Instead of counting in a binary manner, tries all values of bits
  - Starts from most-significant bit and goes to least-significant bit.
- SAR looks at the comparator's output to check if the binary count is less-than or greater-than the analog signal input.
  - "trial by fit"

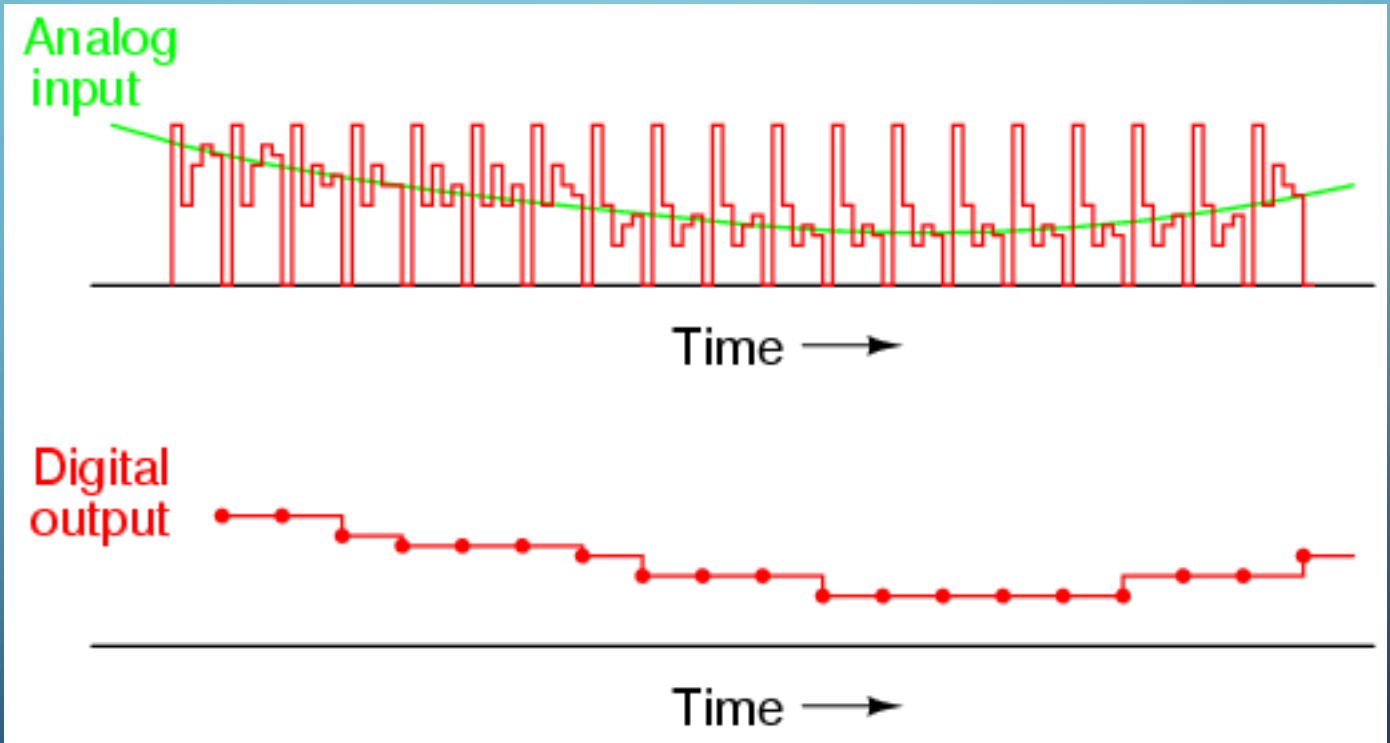
WHY USE A SUCCESSIVE APPROXIMATION ADC?

- offers one distinct advantage
  - Converges much faster to an analog signal than a 0 to full counter.
    - Stepping every clock cycle

DIAGRAM OF ADC



OUTPUT



REFERENCES

- https://www.allaboutcircuits.com/textbook/digital/chpt-13/successive-approximation-adc/ (used for all figures as well as information).