1. **Speedup from Bit Parallelism:** Problem 5.16. From everything you have learned in the class, explain why the problem statement is incorrect.

2. **Fault Simulation Algorithms:** Use the circuit shown below and test vector 111 for all parts.
   a. Show execution for event driven **Differential Simulator** for test vector 111 and fault a/0 followed by fault d/0. How many gates were evaluated for d/0?
   b. **Event reduction in PROOFS:** Consider the complete un-collapsed fault list. Give the list of faults that PROOFS identifies as – 1. Unexcited 2. Excited but not propagated one level and 3. Excited but not propagated 2 levels for the test vector 111.
   c. Perform **PROOFS fault simulation** assuming word length of 4-bits, for test vector 111 on the fault list groups \{a/0, b/0, c/0, n/0\} followed by group \{g/1, k/1, p/0, r/0\}. Use un-encoded symbolic logic 0, 1 and X (do not use V0, V1). Show each group on a different copy of the figure.
   d. Use **Star-Algorithm** to identify faults that will not be detected by vector 111.
   e. Perform **Deductive fault simulation** for test vector 111 on the fault list \{a/0, a/1, b/0, b/1, c/0, c/1, d/1, e/1, h/1, k/1, p/1, m/0, n/0, q/1\}.