2016 Fall
ECE 511 Computer Architecture

Instructor:
Professor Nam Sung Kim
Email: nskim@illinois.edu (Please include “[ECE 511]” in the email subject line if you want any response from me related to the course).
Office: CSL #217
Office Hours: Wed 5:00-6:00p.m. or available by an appointment.

TAs:
Hadi Asgharimoghaddam,
Email: asghari2@illinois.edu
Office: ECEB #3036
Office Hours: Fri 10:00-11:00a.m.
Ahmed Abulila
Email: abulila2@illinois.edu
Office: ECEB #3036
Office Hours: Mon 9:00-10:00a.m.

Course Description:
Advanced concepts in computer architecture: design, management, and modeling of memory hierarchies; pipelined computers; and multiple processor systems. Emphasis on hardware alternatives in detail and their relation to system performance and cost. Course Information: Same as CSE 521. Prerequisite: ECE 411 or CS 433. More specifically, assuming knowledge of pipelined processors with cache memories, as studied in depth in ECE 411, we continue with advanced techniques for extracting greater levels of instruction-level parallelism and memory-level parallelism in ECE 511. The former exploits opportunities for parallel execution of instructions from an inherently serial instruction stream, while the latter attempts to overlap increasing memory access latency with other useful work. We will study the memory hierarchy as well as virtual memory, and will also cover processor chips that with multiple cores, where concurrency is extracted from multiple sequential threads of execution.

Course Prerequisites:
- ECE 411 or CS433.
- UNIX commands
- C/C++ programming
- System Verilog

Course Textbook:

Recommended Textbook:
Lectures:
It is very important that you attend lecture faithfully. Much of the material will be covered only in lecture, as the textbook and readings are by definition out of date. Also, we will have a few unannounced in-class quizzes. Some review lectures will only be presented online.

Homework:
There will be a few assignments using a computer architecture simulator, gem5 (www.gem5.org). These assignment will require C++ programming and LINUX skills. Considering unexpected illness, job interviews, and family matters, each student will be given one chance to submit an assignment within one week of a given deadline.

Project:
Each team is comprised of three or fewer students. You can choose an interesting topic from past papers appeared in top conferences such as International Symposium on Computer Architecture (ISCA), International Symposium on Microarchitecture, and International Symposium on High-Performance Computer Architecture (HPCA), and evaluate them using an architecture simulator such as gem5. However, doing an original study will be encouraged and thus given more credit. Later you may choose some topics that I will suggest.

Quizzes, Paper Reviews, and Examinations:
There will be a few unannounced in-class quizzes throughout the semester. A paper review schedule will be published on the website. The lowest quiz score will be dropped to accommodate absences.

Grading (Tentative):
1. Quizzes and Assignments: 10%
2. Midterm Exam: 20%
3. Final Exam: 30%
4. Project: 40%

“Tentative” Schedule:

<table>
<thead>
<tr>
<th>Date</th>
<th>Topic</th>
<th>Assignments</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>8/23</td>
<td>Course Introduction</td>
<td></td>
<td>[DAS] Ch. 1; Note 1.</td>
</tr>
<tr>
<td>8/25</td>
<td>Quantitative Evaluations</td>
<td></td>
<td>[DAS] Ch. 9; Note 2.</td>
</tr>
<tr>
<td>8/30</td>
<td>Impact of Technology</td>
<td></td>
<td>[DAS] Ch. 2</td>
</tr>
<tr>
<td>9/1</td>
<td>Instruction-Level Parallelism</td>
<td>Assignment 1</td>
<td>[SL] Ch. 4; Note 3.</td>
</tr>
<tr>
<td>9/6</td>
<td>Branch Prediction &amp; Instruction Fetch</td>
<td>Assignment</td>
<td>Note 4</td>
</tr>
<tr>
<td>9/8</td>
<td>Dynamic Scheduling</td>
<td></td>
<td>[SL] Ch. 5</td>
</tr>
<tr>
<td>9/13</td>
<td></td>
<td></td>
<td>Assignment 1 Due</td>
</tr>
<tr>
<td>9/15</td>
<td>Cache &amp; Virtual Memory</td>
<td>Assignment 2</td>
<td>[DAS] Ch. 4; Note 5.</td>
</tr>
<tr>
<td>9/20</td>
<td>Memory System</td>
<td></td>
<td>Assignment 2 Due</td>
</tr>
<tr>
<td>9/27</td>
<td></td>
<td>Assignment 3</td>
<td></td>
</tr>
<tr>
<td>9/29</td>
<td>Emerging Memory</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10/4</td>
<td>SSD &amp; Storage System</td>
<td>Assignment 4</td>
<td>Assignment 3 Due; Note 6</td>
</tr>
</tbody>
</table>
10/6  Multiprocessor Systems [DAS] Ch. 5
10/11
10/13  Interconnection Network [DAS] Ch. 6
10/18  Midterm
10/20  Project Proposal Presentation
10/25  Chip Multiprocessors [DAS] Ch. 7
10/27
11/1  Coherence, Consistency, Synch. [DAS] Ch. 8
11/3
11/8  Vector, SIMD, and GPU Architectures [HP] Ch. 4
11/10
11/15  Accelerators
11/17  Datacenter Architecture [HP] Ch. 6
11/22  No Lecture (Thanksgiving)
11/24  No Lecture (Thanksgiving)
11/29  Project Review (1)
12/1   Project Review (2)
12/6   Final Exam Review

Note:
1. http://ece552.ece.wisc.edu/ece552_15_pipelining/index.htm
   http://ece552.ece.wisc.edu/ece552_16_pipeline_hazards/index.htm or
   https://courses.engr.illinois.edu/ece511/assets/lecture-08--pipelining-spring-2016.pptx
2. We will have two simulator tutorial sessions at 7pm on Aug 29 and Aug 31. A student can choose
   one of these two sessions and need to sign-up.
3. https://courses.engr.illinois.edu/ece511/assets/lecture-12--ooo-spring-2016-updated.pptx
   https://courses.engr.illinois.edu/ece511/assets/lecture-13--ooo-recovery-spring-2016.pptx
   https://courses.engr.illinois.edu/ece511/assets/lecture-14--register-renaming-spring-2016.pptx
4. https://courses.engr.illinois.edu/ece511/assets/lecture-09--branch-spring-2016-updated.pptx
   https://courses.engr.illinois.edu/ece511/assets/lecture-11--branch-advanced-spring-2016.pptx
5. https://courses.engr.illinois.edu/ece511/assets/lecture-05---cache-introduction-spring-2016-updated.pptx
   https://courses.engr.illinois.edu/ece511/assets/lecture-06---cache-policy-spring-2016.pptx
6. Form a project team.