Analog Computing Technique

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Chapter 1

Programming Principles and Techniques

1. Analog Computers and Simulation

An analog computer can be used to solve various types of problems. It solves them in an "analogous" way (pun intended). Two problems or systems are considered *analogous* if certain or all of their respective measurable quantities obey the same mathematical equations. Most general purpose analog computers use an active electrical circuit as the analogous system because it has no moving parts, a high speed of operation, good accuracy and a high degree of versatility. Active electrical networks consisting of resistors, capacitors, and op amps connected together are capable of simulating any linear system since the forward voltage

transfer characteristics of these networks are analogous to the basic linear mathematical operations encountered in the system's mathematical model. By using diode function generators and special circuits which have non-linear voltage transfer characteristics, it is also possible to simulate nonlinear systems.

The mathematical model of an analog computer programmed to simulate a specific physical system is identical to the mathematical model of the system. The voltage transfer characteristics of the electrical networks are analogous to the desired mathematical operations. The input and output voltages (computer variables) are analogous to the corresponding mathematical variables (problem variables) of the problem. Because of limitations of the computer or its associated input/output equipment, it is usually necessary to change the scale of the computer variables, thus forcing the values of a computer variable to differ from the corresponding problem variable values. It is important to understand that an analog computer solution is simply a voltage wave form whose time dependency is the same as that of the desired variable.

The normal procedure for simulating a system starts with determining the mathematical model describing the physical quantities of interest. An analog block diagram is made to relate the sequence of mathematical operations and to aid in scaling the variables. From the analog block diagram the electrical components are connected together (patched). The computer is operated and the computer variables observed on a recorder or oscilloscope. Since the output is a computer variable (voltage wave form) it is necessary to convert the output variable back to the original problem variable.

2. Solving Differential Equations with an Analog Computer.

A typical simulation of a physical system involves a mathematical model consisting of a set of one or more differential equations and initial conditions on the variables. If the system is linear, the differential equations are linear and the operations required are 1) summation, 2) sign inversion, 3) multiplication by a constant, 4) integration and 5) differentiation. For practical reasons, the integration operation is easier to implement than the differentiation operation. The reason lies in the fact that computer signals are real voltages and, therefore, are corrupted by noise to some extent. Since integration has a tendency to average out the effects of noise (while differentiation will accentuate it), a more precise solution can be obtained using integration techniques.

Each of these operations may be represented as shown in Figure 1.1 Actual realization of these will be discussed in the next section.
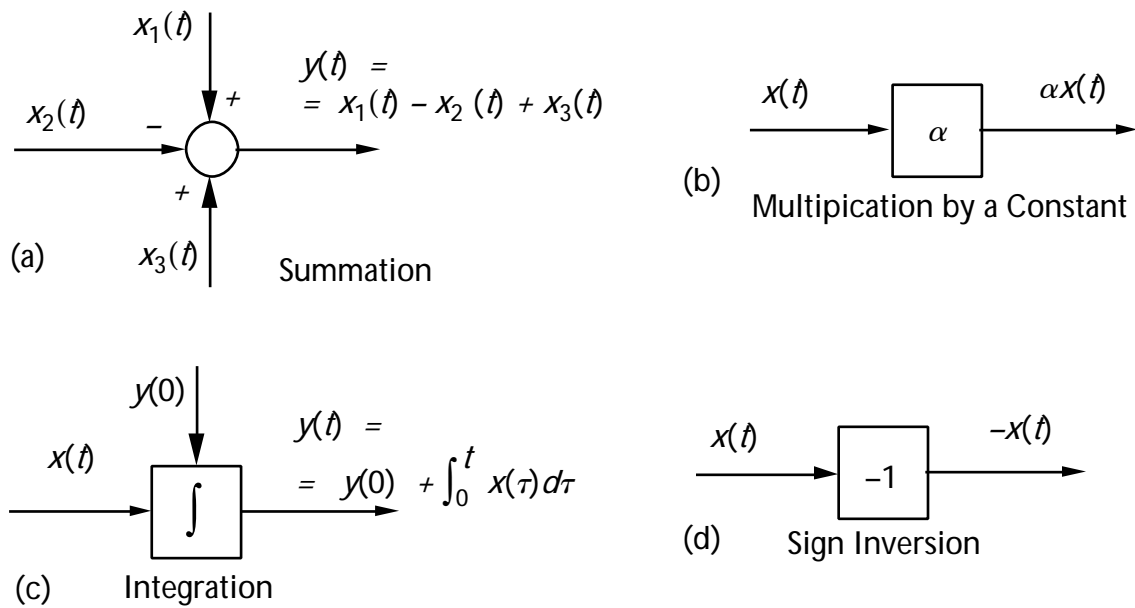
Figure 1.1: Basic Linear Operations

As an example, consider the computer solution of the differential equation

$$\frac{dy}{dt} = y, \quad y(0) = 1 \tag{1.1}$$

Since the analog computer solves the equivalent integral equation, we integrate both sides.

$$y(t) = y(0) + \int_0^t y(\tau)\,d\tau. \tag{1.2}$$

The definition of integration given in Figure 1.1 would represent equation (1.2) if the input were the same as the output. This condition can be easily implemented by connecting the input to the output as shown in Figure 1.2.
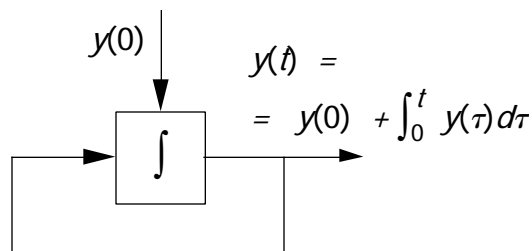
Figure 1.2: Block Diagram Realization of the Integral Equation.

It is important to note that it is not necessary to know the input of the integrator in order to solve equation (1), but only that the input must be equal to the output at all times. The idea of feeding an unknown output back to the input to generate a solution is basic to analog

computer solution of differential equations. This is not unreasonable since the differential equation determines the class of solutions, while the initial conditions determine the specific solution.

A higher order linear differential equation may be handled by reducing it to a set of first–order equations and following a similar procedure. For example,

$$\frac{d^2 y}{dt^2} + \frac{dy}{dt} + y = 0, \quad y(0) = 1, \ \dot{y}(0) = 0, \tag{1.3}$$

may be turned into the set of equations

$$\dot{x}_1 = x_2, \quad x_1(0) = 1 \tag{1.4a}$$

$$\dot{x}_2 = -x_1 - x_2, \quad x_2(0) = 0 \tag{1.4b}$$

where $x_1 = y$, and $x_2 = dy/dt$. The equivalent integral forms are

$$x_1(t) = x_1(0) + \int_0^t x_2(\tau)\, d\tau, \tag{1.5a}$$

$$x_2(t) = x_2(0) - \int_0^t \left[x_1(\tau) + x_2(\tau)\right] d\tau \tag{1.5b}$$

Equations (1.5a) and (1.5b) may be implemented using the circuit shown in Figure 1.3.
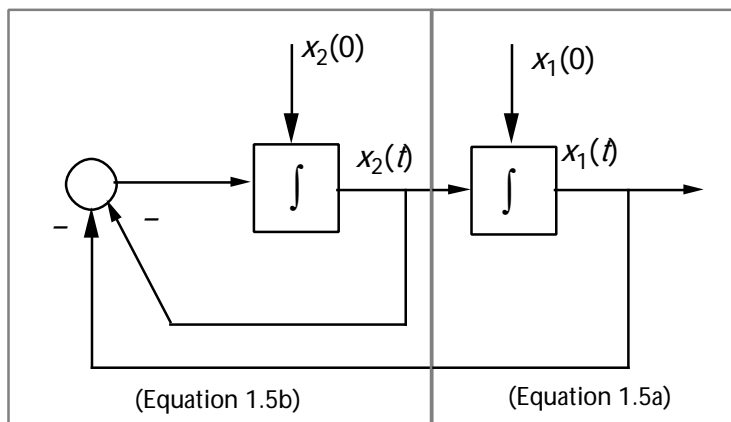

Figure 1.3: Circuit Realization of the Second Order Equation.

3. Physical Realization of Linear Operations on an Analog Computer.

In section 2, the differential equation was expressed in terms of a set of general mathematical operation. No attempt was made to discuss how these operations were realized with physical

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components. In this section, the basic linear operations of summation, multiplication by a constant, and integration will be discussed. The operation of sign inversion will be inherent in the summation and integration operations as a result of construction convenience and versatility.

(a) The Operational Amplifier (Op Amp).

The operational amplifier is a high gain amplifier with a wide variety of applications. The amplifier is usually described in terms of its gain, input impedance, output impedance, bandwidth, and offset characteristics. An operational amplifier usually has two input terminals. The two input terminals are marked with a (+) to indicate the noninverting input and a (–) to indicate the inverting input. An equivalent circuit for an op amp and a standard symbol are shown in Figure 1.4.
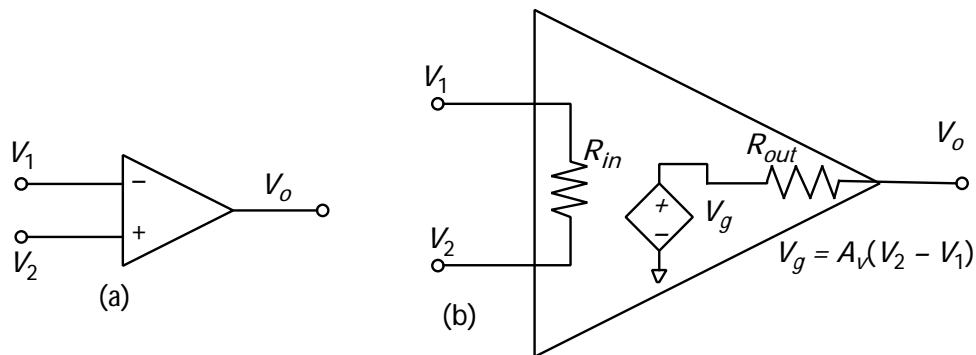

Figure 1.4: (a) The Circuit Symbol for an Op Amp, (b) An Equivalent Op Amp Circuit.

(b) Summers and Inverters.

The electrical circuit whose transfer characteristics are analogous to the mathematical operation of summation is shown in Figure 1.5 (for an n–input summer). Applying Kirchoff's current law at the summing junction gives

$$i_1 + ... + i_n + i_f = i_a \qquad (1.6)$$

or, in terms of voltages

$$\frac{V_1 - V_x}{R_1} + ... + \frac{V_n - V_x}{R_n} + \frac{V_o - V_x}{R_f} = \frac{V_x}{R_{in}} . \qquad (1.7)$$

Note that since $V_o = -A_v V_x$, then equation (1.7) can be rewritten

$$\frac{V_1}{R_1} + ... + \frac{V_n}{R_n} + \frac{V_o}{R_f} = -\frac{V_o}{A_v R} \, , \qquad (1.8)$$

where

$$\frac{1}{R} = \frac{1}{R_1} + \cdots + \frac{1}{R_n} + \frac{1}{R_f} + \frac{1}{R_{in}} . \qquad (1.9)$$
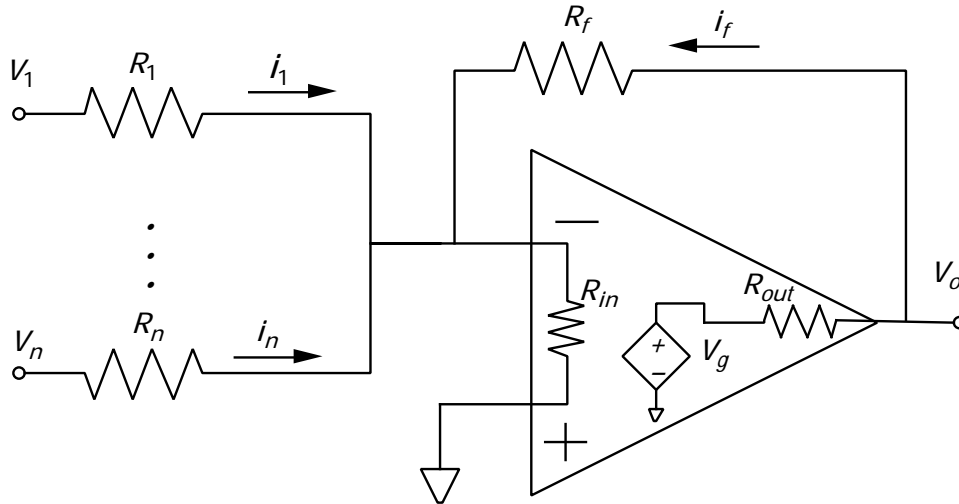

Figure 1.5: Summing Amplifier

By isolating V_o, we obtain,

$$V_o = -\frac{R_f}{R_1\left(1 + \dfrac{R_f}{A_v R}\right)} V_1 - ... - \frac{R_f}{R_n\left(1 + \dfrac{R_f}{A_v R}\right)} V_n . \qquad (1.10)$$

Since the op amp has a very high voltage gain (usually $> 10^5$), we assume that $A_v \to \infty$. Thus, equation (1.12) reduces to

$$V_o = -\frac{R_f}{R_1} V_1 - ... - \frac{R_f}{R_n} V_n . \qquad (1.10)$$

Usually, analog diagrams are given in terms of symbols which represent the electrical circuit. For this weighted summation, the analog symbol is shown in Figure 1.6, and we have the output equation

$$V_o = -K_1 V_1 - ... - K_n V_n \, , \qquad (1.11)$$

and

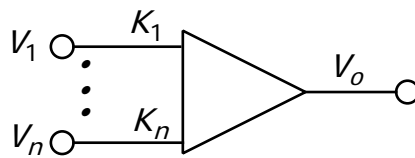$$K_i = \frac{R_f}{R_i}, \quad i = 1, \ldots, n.$$ (1.12)

Figure 1.6: Weighted Summing Amplifier

Since the circuit in Figure 1.5 is to be implemented on the analog computer, it is essential that the summing operation indicated by Figure 1.6 and equations (1.11) and (1.12) be understood thoroughly.

Note that the inherent sign inversion is a result of the negative voltage gain of the op amp. Thus, the *inverter* which inverts the sign of its input is a special case of the summer with only one input and with $K_1 = 1$. The transfer characteristic is given by

$$V_o = -V_1.$$ (1.13)
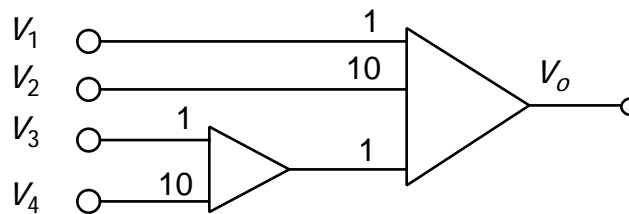
Figure 1.7: Analog Diagram for Example 1.1.

Example 1.1: Determine the circuit to produce the output voltage given by

$$V_o = -V_1 - 10V_2 + V_3 + 10V_4.$$ (1.14)

Solution: An analog diagram (i.e. in terms of symbols) for equation (1.14) is given in Figure 1.7. The circuit diagram which must be patched on the analog computer to realize equation (1.14) is shown in Figure 1.8.
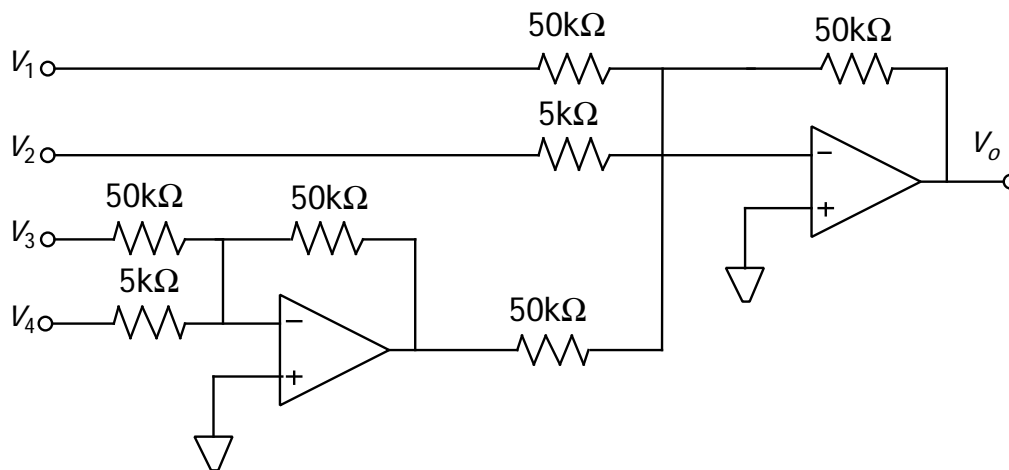
Figure 1.8: Electronic Circuit for Example 1.1.

In an actual amplifier, the output voltage will not be zero when V_i and V_n are zero. This effect is called the offset and is usually measured as is shown in the drawing below. The value of V_{os} required to reduce V_o to zero under the conditions shown is called the offset voltage. Under the conditions shown ($V_o = 0$), the offset current, I_{os}, is defined as $I_x - I_y$. Note the termination attached to the noninverting input in Figure 1.9.

$$R_n = \frac{R_i R_f}{R_i + R_f}$$
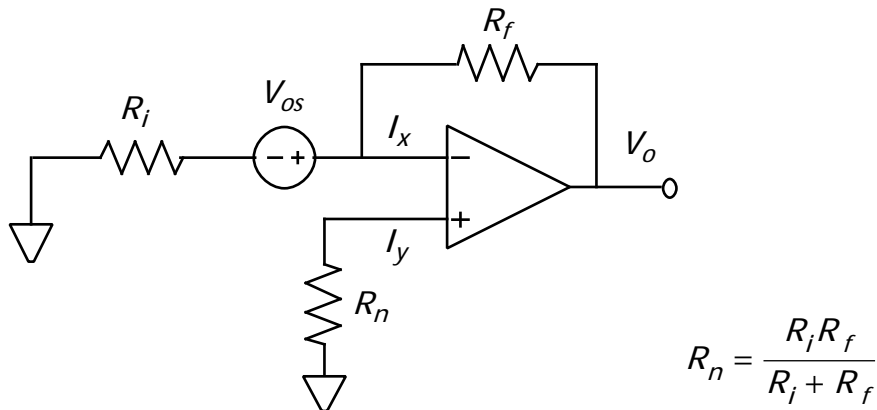
Figure 1.9: Op Amp Circuit Showing the Offset Voltage

In an actual amplifier, the output voltage V_o is not normally zero when $V_x = V_y$. This effect is often described in terms of the common mode gain (CMG) and the common mode rejection ratio (CMRR). Measurement of the CMG and CMRR are illustrated in Figure 1.10.
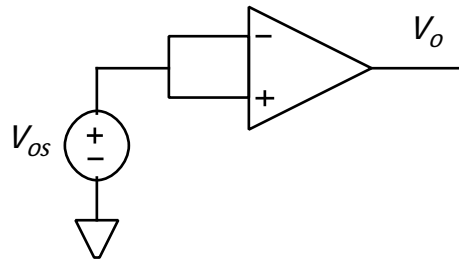
$$CMRR = \frac{kV_o}{V_{CM}} \tag{1.15}$$

Figure 1.10: Op Amp Configuration for Determining CMRR

Operational amplifiers come in many forms. As an example the characteristics of the μA 709 (a simple integrated circuit amplifier) are given below.

A_v	45,000
V_{os}	1 mV (typical for $R_i < 10\text{k}\Omega$)
I_{os}	0.2μA
R_{in}	100kΩ
R_{out}	150Ω
CMRR	90dB

(c) Multiplication by a Constant ; Reference Voltages.

The op amps on the Comdyna GP-6 computer are constructed with 5K and 50k resistors only. Thus, in order to realize gains (constant multipliers) other than 1/10, 1 and 10, another technique must be used. The coefficient potentiometer (pot) is a voltage divider which allows the output voltage to be some fraction of the input voltage. A pot thus has a gain of less than unity. The electrical circuit diagram and analog computer diagram are shown in Figure 1.11. The transfer characteristic is given by

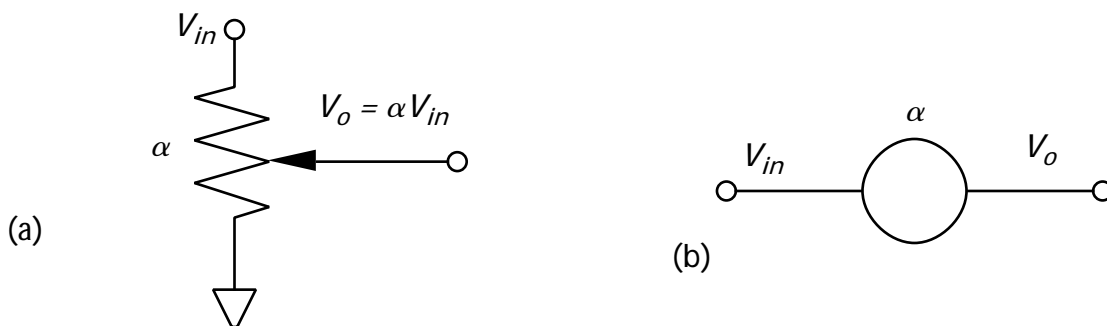$$V_o = \alpha V_{in}, \quad 0 \le \alpha \le 1. \tag{1.16}$$

The gain α is always placed outside the pot with the inside reserved for a pot identification number. A constant term in a differential equation is obtained by using a dc reference voltage which is supplied on the computer. Its value is usually $\pm$ the range of the op amps. For the GP-6, this is ± 10v. Note that the actual dials for the potentiometer are illustrated in Appendix A.

Example 1.2: Determine the analog diagram and circuit to implement the equation

$$V_o = -0.35\,V_1 + 5.24\,V_2 + 2.6. \qquad (1.17)$$

Solution: The analog diagram is given in Figure 1.12 and the electrical circuit in Figure 1.13. A GP-6 wiring diagram is supplied in Figure 1.14 to illustrate the actual connections needed.
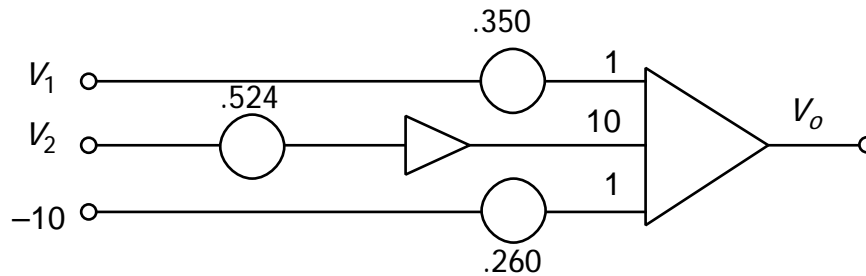

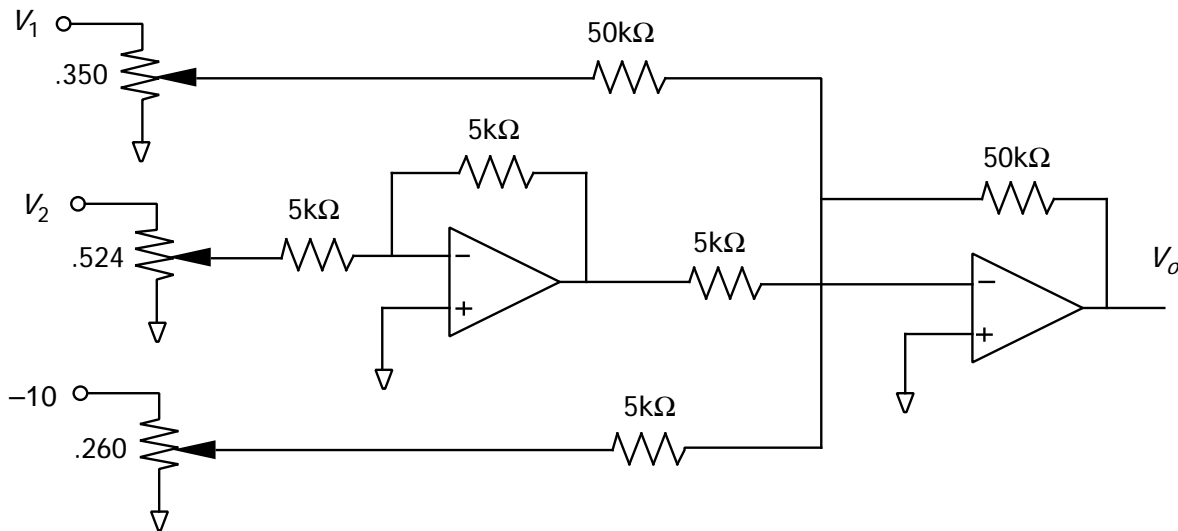**Figure 1.12: Analog Diagram for Example 1.2.**

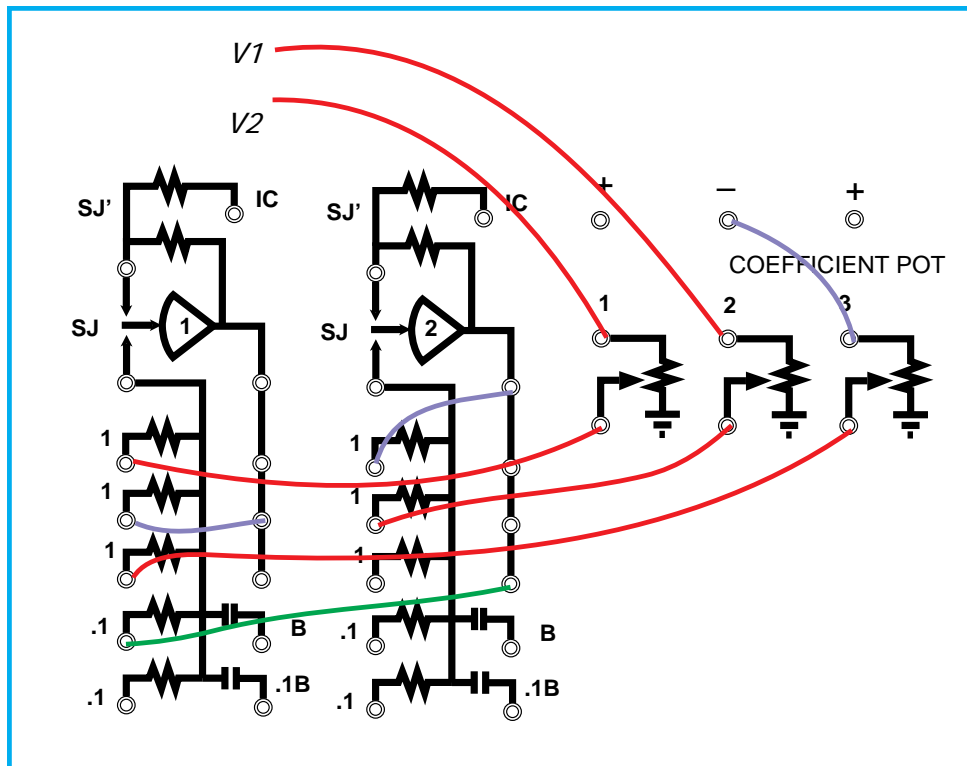**Figure 1.13: Circuit Diagram for Example 1.2.**

Figure 1.14: GP-6 Wiring Diagram for Example 1.2.

(d) Integrators.

Integration is the most important operation available on the analog computer. In fact, analog computers owe their existence to their ability to integrate rapidly. Integration is different from inversion and summation because it is time dependent. Integration can be accomplished by replacing the feedback resistor of the summer with a capacitor. The resulting electrical circuit for an integrator is shown in Figure 1.15.
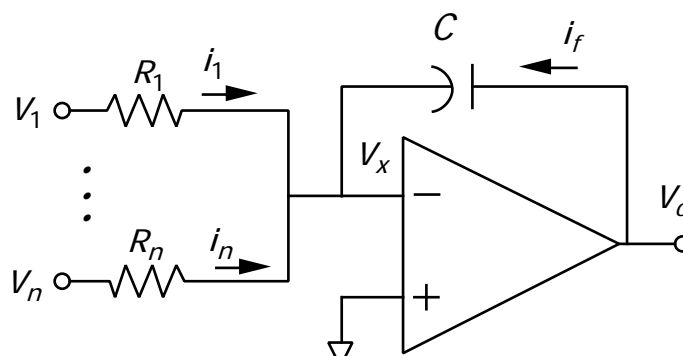

Figure 1.15: Electrical Circuit for an *n*-Input Integrator.

Using the same procedure and approximations as used for the summer, the transfer characteristic for the circuit of Figure 1.15 becomes

$$V_o(t) = V_o(0) - \int_0^t \left[\frac{V_1(\tau)}{R_1 C} + \dots + \frac{V_n(\tau)}{R_n C} \right] d\tau \qquad (1.17)$$

Again, there is a sign inversion in the integration operation as a result of the negative voltage gain of the op amp. Note that summation and integration can be performed with a single amplifier. The analog computer symbol for the integrator is shown in Figure 1.16.
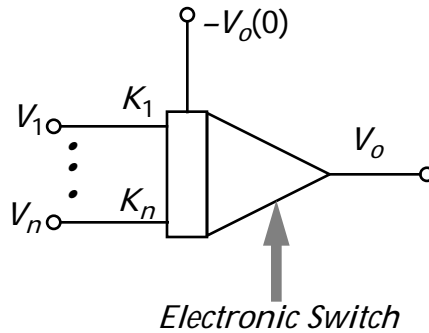

Figure 1.16: Analog Computer Diagram for an Integrator.

The electronic switch terminal (ES) is used to control the operating modes of the integrator. The normal modes of operation are the initial condition (IC) mode and the operate (OP) mode. The IC mode allows the integrator capacitors to be charged to the initial values, while the OP mode causes the solution to occur. This sequence is shown for the example in Figure 1.17. The switches for the IC, HD, OP, and RO are illustrated in Appendix A.
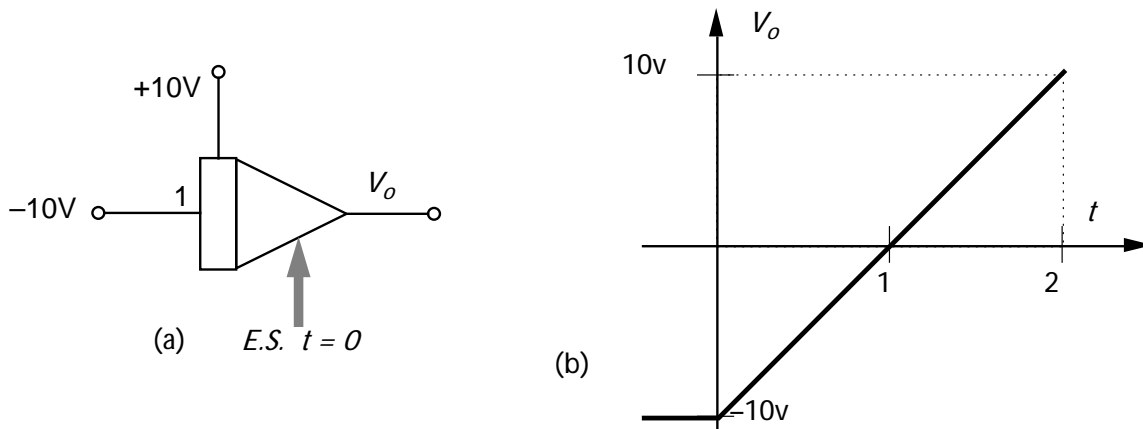

Figure 1.17: (a) Analog Computer Diagram for Example 1.3, (b) Voltage Output for Example 1.3.

The electronic switch is nothing more than a SPDT switch with one pole grounded. Control of the electronic switch is made through a switch driver and logic circuits which are usually controlled by the computer mode control switches on the front panel. It is important to note, concerning the analog symbol for the integrator, that i) $-V_o(0)$ must be applied to the IC

terminal to get $+V_o(0)$ at the output and ii) the electronic switch, ES, is usually implied and not shown unless it is used in an unconventional manner.

Circuit diagrams for the integrator are shown in Figure 1.18. In the initial condition state, illustrated by Figure 1.18a, the capacitor charges to $-V_{ic}$ which can be used to represent an initial condition. When in the OP mode, the output of the system is the negative of the integral of the input starting from the initial condition. The equivalent circuit under these conditions is shown in Figure 1.18b. Note that the initial condition part of the circuit is grounded.
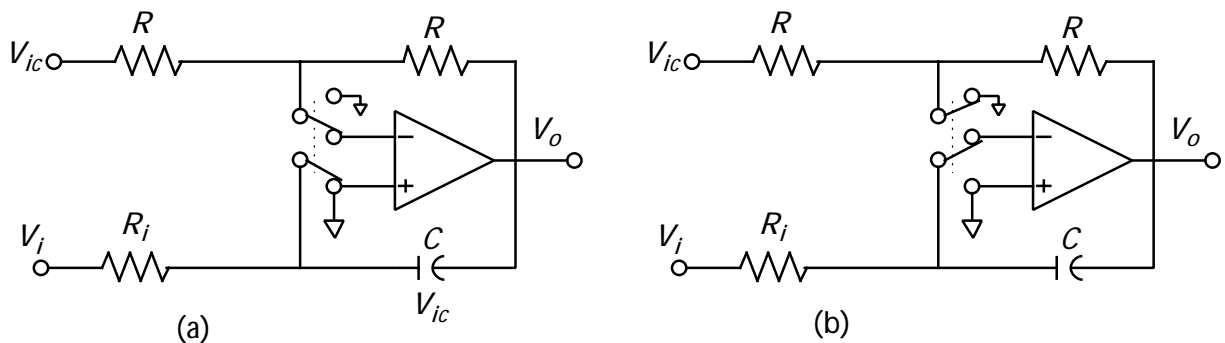

Figure 1.18. (a) Integrator Circuit in IC Mode, (b) Integrator Circuit in OP Mode.

4. A Systematic Procedure for Programming Differential Equations

Although the procedure presented in Section 2 may be used to determine the analog diagram of a linear differential equation, a more systematic version will be developed. This procedure does not require that a first order integral equation be considered for each integrator, but instead requires an equation for the highest order derivative. This equation will correspond to Equation (1.4) in Section 2. There is no essential difference in the theory or results of the two techniques. Only the steps required differ.

Consider, for purposes of illustration, the second order linear differential equation and initial conditions,

$$\frac{d^2x}{dt^2} + 0.5\frac{dx}{dt} + x = 4, \quad x(0) = 0, \dot{x}(0) = 1 \ . \tag{1.18}$$

If any derivative of a variable is known, then it may be integrated to obtain the variable. In the case of Equation (18) if the second order derivative $(d^2 x/dt^2)$ were known, then it could be

integrated once to obtain the first order derivative *(-dx/dt)* and a second time to obtain the variable *(x)*. Note that since the integrator has a sign inversion associated with it, the output of every odd integration is negative. But Equation (1.18) gives the second order derivative in terms of the lower ordered derivative. Thus,

(1)   If d^2x/dt^2 is known, $-dx/dt$ and *x* may be obtained;

(2)   If dx/dt and *x* are known, d^2x/dt^2 may be obtained.

This circular argument states that only the relationship between the inputs and outputs of the integrators are known, not the actual values of the inputs and outputs. This should not seem too strange since a differential equation represents only the class of solutions. The boundary values or initial conditions are necessary to determine a particular solution. The initial conditions have not yet been considered.

    The programming procedure is then as follows:

(a) Assume that the highest order derivative (d^2x/dt^2 in this case) is known and generate all lower order derivatives as shown in Figure 1.19. Note that the output should always be *x*, not -*x*, since *x* is the desired solution.
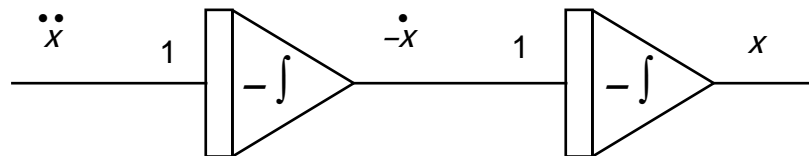

Figure 1.19: Analog Circuit for a Double Integrator

(b) Solve the differential equation for the input to the integrator string and form the indicated sum.

$$\frac{d^2x}{dt^2} = -0.5\frac{dx}{dt} - x + 4 \qquad\qquad (1.19)$$

(Don't forget that the "summer" also inverts!). See Figure 1.20.
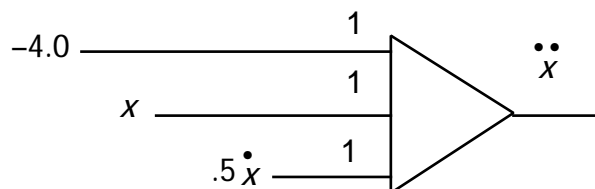

Figure 1.20: Generating the Second Derivative.

(c) Combine the results of (a) and (b) using pots, summers and inverters where required. See Figure 1.21.

(d) Add all the initial conditions. Recall that the applied initial condition should be the *negative* of the *integrator output* at $t = 0$. See Figure 1.21.
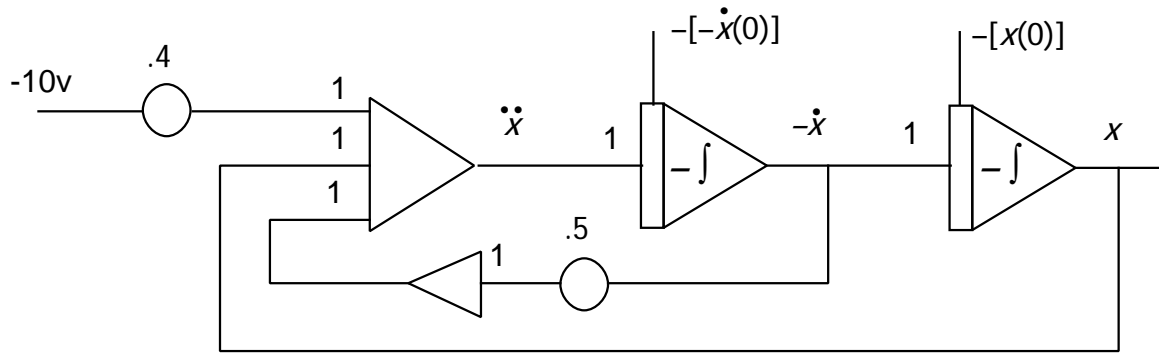

Figure 1.21: Analog Diagram for the Second-Order System.

Although Figure 1.21 is the final diagram, it is possible to remove the summer by recalling that the integrator can also be a summer. Inverters must then be inserted or removed from each feedback loop to take care of the sign inversion. Usually, the form which uses the least number of elements (pots, amps, etc.) is the preferred form since the probability of a bad lead or element in the patched problem is lessened. Figure 1.22 represents the same problem as Figure 1.21, but with the summer removed. Figure 1.23 shows how Figure 1.22 would actually be wired up on the GP-6.
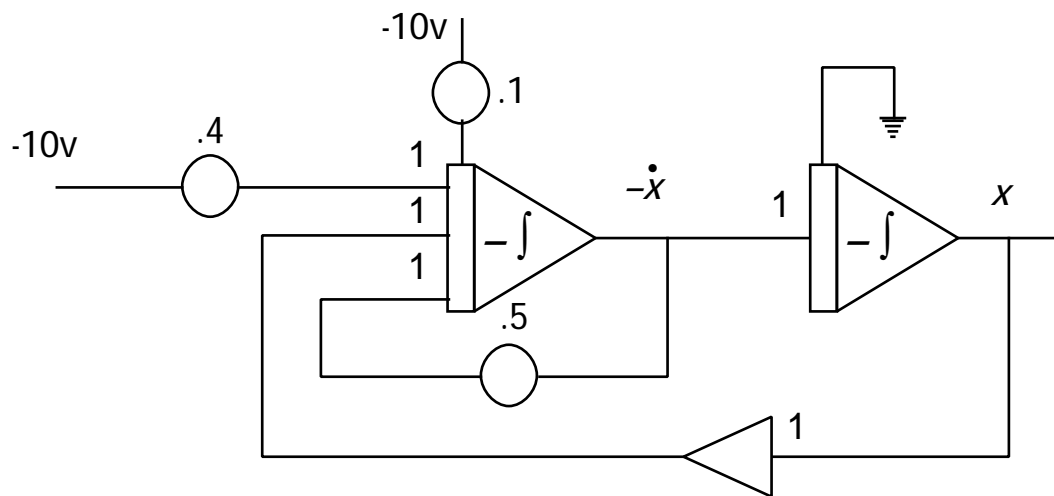

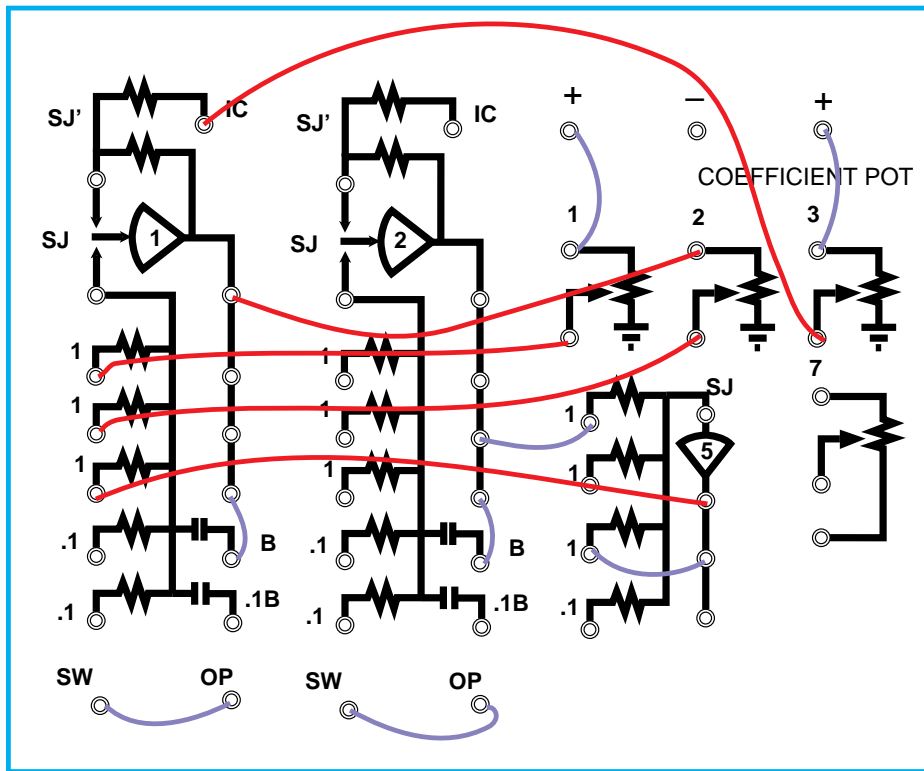**Figure 1.22: Alternate Diagram, with Reduced Number of OpAmps**

Figure 1.23:. GP-6 Wiring Diagram for Figure 1.22

As another example, consider a general third order linear differential equation. The procedure may be extended for a system of any order. We have

$$\frac{d^3 x}{dt^3} + a_2 \frac{d^2 x}{dt^2} + a_1 \frac{dx}{dt} + a_o x = f(t),$$ (1.20)

with initial conditions

$$x(0) = x_o, \dot{x}(0) = \dot{x}_o, \ddot{x}(0) = \ddot{x}_o.$$ (1.21)

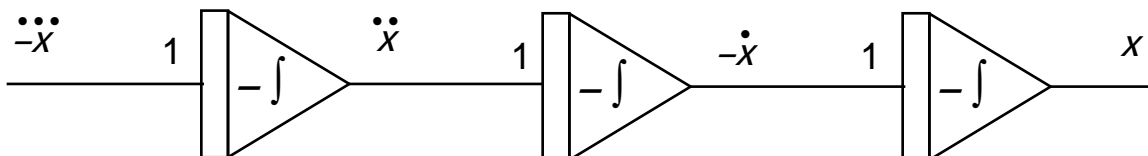Using the procedure outlined above:

(a) Form the integrator string

Figure 1.24: A Third-Order String of Integrators.

(b) Solve for the input to the integrator string and form the indicated sum.

$$-\frac{d^3x}{dt^3} = a_2 \frac{d^2x}{dt^2} + a_1 \frac{dx}{dt} + a_ox - f(t),$$ (1.20)
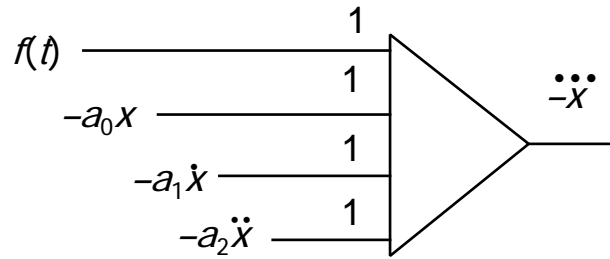

Figure 1.25: Generating the Third Derivative.

(c) Combine the results of (a) and (b).

(d) Add the initial conditions and remove the summer since one less amplifier is required. The result is shown in Figure 1.26.
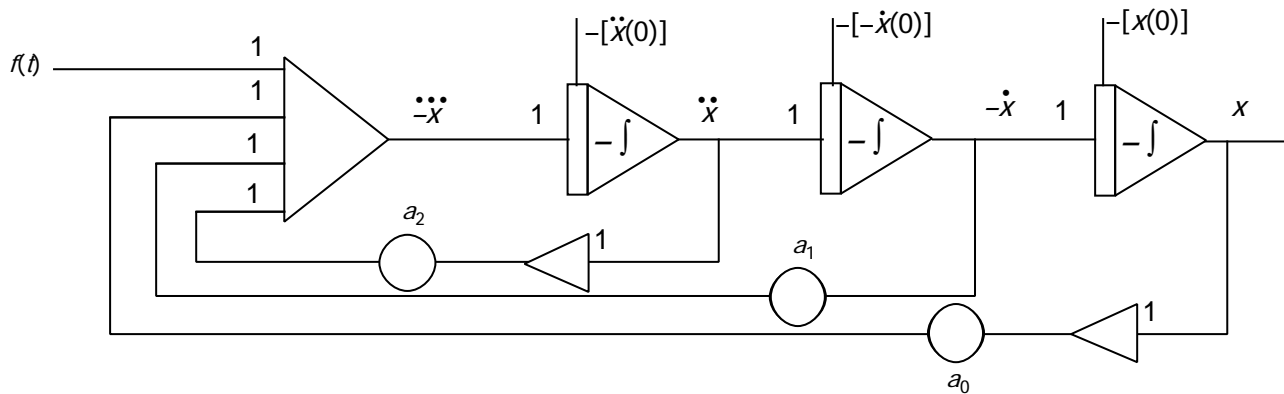

Figure 1.26: The General Third-Order System.

5. Tricks with Transfer Functions

Suppose we have the first-order transfer function

$$G(s) = \frac{Y(s)}{U(s)} = \frac{a}{s+b}, \qquad 0 < a \le 10, 0 < b \le 10$$

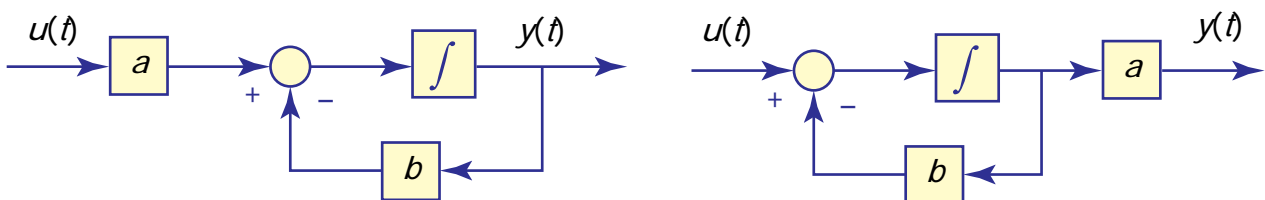This can be drawn in either of the all-integrator diagrams shown in Figure 1.27.

Because the gains are of values less than 10, then nothing more than a 10x input is needed. Example analog computer diagrams are shown for the two block diagrams as shown in Figure 1.28. We note that the analog computer does very well at implementing a first-order system.
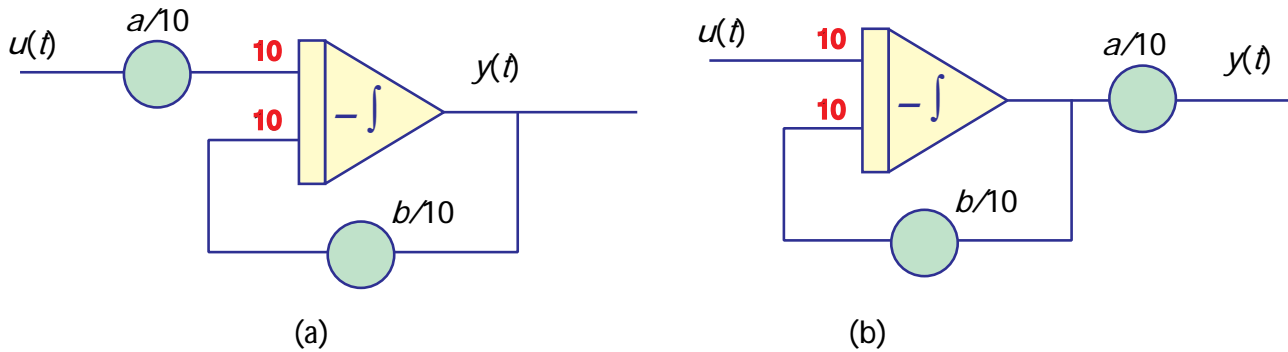

(a)   (b)

Figure 1.28: Analog Computer First Order Diagrams

Of the two circuits, both have advantages and disadvantages. The circuit (a) has the advantage that the output comes directly from an op-amp, and can thus be used to drive another circuit. This circuit is also good if an initial condition, $y(0)$, is given. It has the disadvantage that its input has a pot before entering the op amp. Thus, this circuit will tend to load whatever signal is driving it. The circuit (b) has the advantage that it does not load the circuit that is driving it, but has a pot on the output, and is thus not very useful in driving another circuit. Both of these circuits, however may be used in a higher-order transfer function realization. For example, if a transfer function has simple real poles and the cascade factorization

$$G(s) = \left(\frac{a_1}{s + p_1} \right) \left(\frac{a_2}{s + p_2} \right) \cdots \left(\frac{a_n}{s + p_n} \right)$$

where all the coefficients are of magnitude less than 10, then these circuits may be simply cascaded (put in series) to form the overall transfer function. Some suggestions to this approach include

i) Using circuit (b) to implement the first (input) stage, and (a) as the output stage.

ii) Alternating circuits to combine coefficients and thus reduce the number of required potentiometers.

iii) Using an additional inverter on the output if there are an odd number of poles.

If our transfer function has the partial fraction expansion

$$G(s) = d_1 + \frac{c_1}{s + p_1} + \frac{c_2}{s + p_2} + \cdots + \frac{c_n}{s + p_n}$$

then we may implement this transfer function using the first-order circuits in parallel, with the output of each entering into a summer. In this case, circuit (b) would be preferable to prevent loading the input.

Chapter 2
Magnitude and Time Scaling Techniques

1. Scaling

In the solution of the problems described in Chapter 1, no consideration was given to the magnitudes of the problem variables nor to the time required for solving each problem. Equipment constraints usually restrict the maximum voltage output of each amplifier to 10 volts. If the problem dictates a large voltage output, amplifier overload occurs and the solution is invalid. For example, if the problem of calculating a rocket speed were solved on the GP-6 computer, it would be impossible to relate 1 v on the computer to 1 ft/sec in the real problem. However, the problem might be solved by relating 1 v on the computer to 1 mile/sec in the problem. We see that the problem must be magnitude scaled so that it will fit the computer. Similarly, in the same problem an acceleration term might have a maximum value of 1 ft./sec^2. Using the basic unit of miles for length as determined for scaling the velocity would give a voltage of approximately 0.002 v which corresponds to the acceleration term. This signal is in the noise level of the computer and would yield erroneous results. Thus, the sample solution of one basic change of units for the entire problem will not always work. It is necessary to scale up some parts of a problem and scale down other parts.

Time scaling is needed, for example, when we wish to study a basic physical phenomenon which evolves much faster or much slower than is convenient for the computer operator. If we wish to study planetary motion, we will not have the time to wait for a complete period of revolution about the sun. An actual time of one year may be represented by, say, 10 seconds of computer time. There are other reasons for time scaling, some of which we shall discover shortly.

2. Magnitude Scaling — Basic Principles

Magnitude scaling is needed whenever a problem variable existing as an amplifier output becomes so large that the amplifier overloads or when the problem variable becomes so small that the amplifier output noise is the predominant output signal.

<u>Example 2.1</u>. Consider the following differential equation:

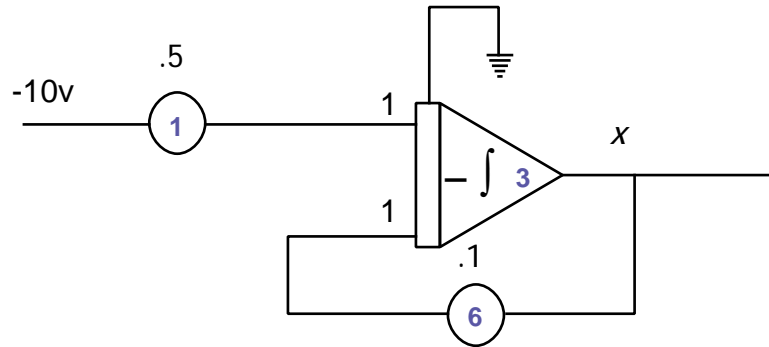$$\frac{dx}{dt} + .1x = 5, \quad x(0) = 0. \tag{2.1}$$

Figure 2.1: Analog Diagram for Example 2.1

To solve this problem, an analog diagram representing Equation (2.1) is drawn following the procedures given in Chapter 1. After patching the analog diagram of Figure 2.1, a trial run on the computer would yield an overload on amplifier 3. The reason is suggested by the analytical solution of Equation (2.1),
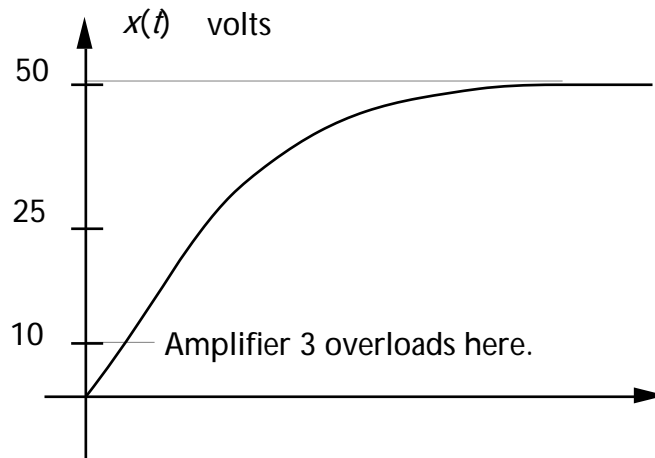
$$x(t) = 50(1 - e^{-.1t}) . \tag{2.2}$$

Figure 2.2 Theoretical Output of the Circuit of Example 2.1.

Clearly, the amplifier overloads because it cannot supply the 50 volts required by the problem. The basic difficulty stems from the fact that 1 volt on the computer corresponds to 1 unit of the problem variable *(x)*. Thus, to avoid this difficulty, a different correspondence must be set up to relate *x* to the computer voltage *(v)*. Since the maximum value of *v* is 10 volts, let 5 units of *x* correspond to 1 volt of *v* (i.e. *v = x/5*). Then when *x* is 50, *v* will be 10 volts and the amplifier will not overload. The basic idea to grasp is that the analog computer does not solve Equation (2.1), but an analogous equation in volts. The analogous equation is

$$\frac{dv}{dt} + .1v = 1, \quad v(0) = 0. \tag{2.3}$$

where $v = x/5$. The solution of equation (2.3) is

$$v(t) = 10(1 - e^{-.1t}). \tag{2.4}$$

3. Analog Voltages Normalized to Units

It is common practice in the literature to redefine the magnitudes of reference voltages and all associated input and output voltages on an analog computer in terms of a quantity called the "analog unit" or just the "unit" By definition, the maximum voltage obtainable on the computer is one unit. Thus, for a ±10 volt computer, 1 unit = 10 volts. Scaling problems in terms of units makes the scaled analog diagram machine-independent (i.e. good for 100 v machines as well as 10 v machines) and sometimes simplifies the scaling of non-linear problems. In these notes most examples are done in terms of volts rather than units because we feel this is somewhat simpler, and more intuitive in terms of the actual circuit.

4. A Systematic Approach to Magnitude Scaling

In light of the discussion given in Section 2, we can develop a systematic approach to magnitude scaling. First, consider the example discussed in that section. A statement of the problem would be: Construct a scaled analog diagram for Equation (2.1) which if patched, will use the maximum range of the amplifier, but will not cause any amplifier overload.

STEP 1. Draw the unscaled analog diagram. Remember that ± 10 volts is the maximum reference available on the computer. See Figure 2.1 for this.

STEP 2. Estimate the maximum value of each variable appearing as an amplifier output. Only the amplifier outputs need to be considered since all other elements have a gain which is less than unity. In this case $x(t)$ is the only amplifier output and its maximum value is known to be 50. A discussion of methods for estimating maximum values of amplifier outputs will be presented later.

STEP 3. Define a scaling relationship between each problem variable and the corresponding computer variable and prepare a scaling table.

For example, if we know $|x|_{max} = 100$ ft. we can represent x on the analog computer as some voltage, v_x. The voltage, v_x can vary from -10v to +10v to +10v whereas x can vary from -100

ft. to +100 ft. Therefore, let 10v represent 100 feet. Then 5 volts corresponds to 50 feet, -10 volts to -100 feet and zero volts to zero feet. Therefore, we may write

$$v_x = \frac{x}{10} \quad . \qquad (2.5)$$

We call the coefficient $(\frac{1}{10})$, the "level of x," and denote it by L_x, so that (2.5) may be written as $v_x = L_x x$. In general, we may choose $L_x = 10/|x|_{max}$. To achieve best accuracy on the analog computer, we utilize the full voltage range of the computer. Therefore, 10 is always used in the numerator of the level equation.

The value of a variable can be computed by reading the voltage of the scaled variable in a simulation, and then dividing it by the level of that variable: $x = v_x/L_x$.

The scaling table for this problem is shown below.

Problem Variable	Estimated Maximum	Level	Computer Variable	I.C.	Scaled I.C.
x	50	1/5	$[x/5]$	0	[0]

STEP 4. Write the scaled analog equations for each amplifier in terms of the computer variables (amplifier outputs)defined in Step 3. *No other variable should appear in these equations*.

Suppose we wish to find an analog simulation to convert feet to inches. Also suppose a maximum of 5 ft. will be converted. Let

$$y = \text{ number of inches}$$
$$x = \text{ number of feet}$$

Then

$$y = ax$$

where

$$a = 12$$

Clearly we must scale the problem so that we can represent 60 inches, (y_{max}), as an analog voltage. We also know:

$$V_x = L_x x, \qquad V_y = L_y y, \qquad\qquad (2.6)$$
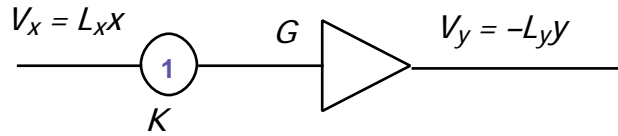
An analog simulation diagram is shown in Figure 2.3.

Figure 2.3: Scaling Diagram

Pot #1 is set to some value which we denote by K. Electronically,

$$(\text{Voltage Out}) = (\text{Overall Gain}) \bullet (\text{Voltage In}),$$

or

$$-L_y y = -K\, G\, V_x.$$

Substituting for the various voltages,

$$-L_y y = -K\, G\, L_x x.$$

Therefore,

$$y = \frac{KGL_x}{L_y}\, x \; .$$

Since we must have

$$a = \frac{KGL_x}{L_y} \; ,$$

then Pot #1 must have the setting

$$K = \frac{aL_y}{GL_x} \; . \qquad\qquad (2.7)$$

In our example, since

$$L_y = \frac{10}{60} = \tfrac{1}{6}, \text{ and } L_x = \frac{10}{5} = 2,$$

then

$$K = \frac{1/6}{2}\frac{12}{1} = 1, \quad \text{and} \quad G = 1.$$

We could also have chosen K = .1, and G = 10. Equation (2.7) leads to the general equation for setting pots:

$$K = \frac{Level\ Out}{Level\ In}\frac{|\ COEF\ |}{gain} \tag{2.8}$$

where

Level Out is the level of the variable immediately following the pot to be set.

Level In is the level of the variable preceding the pot.

COEF relates to the equation to be simulated.

gain is the gain of a summer, inverter or integrator following the pot.

Example 2.2. Simulate $y = a\,x$, where $a = $ -3, $|x|_{max}$ = 20, and $/y/_{max}$ = 40.

Solution: L_x = 1/2, L_y = 1/4. A simulation diagram is shown in Figure 2.4.
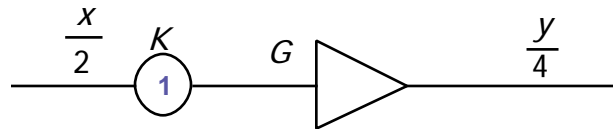
Figure 2.4: Scaling Diagram for Example 2.2.

Thus,

$$K = \left(\frac{1/4}{1/2}\right)\left(\frac{3}{G}\right) = \frac{1.5}{G}\ .$$

If G were a gain of unity pot 1 would have to be set to 1.5 which is impossible. Therefore, let G = 10 and K = 0.15. Finally, we have Figure 2.5.
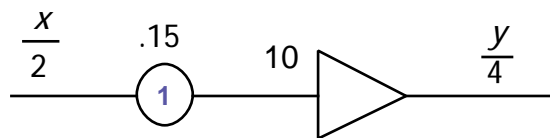

Figure 2.5: Scaling Diagram for Example 2.2 with Gain Values

Once the maximum values and the level constants have been determined we can define the computer variables. Let v_x denote the computer variable corresponding to the problem variable x. We define,

$$v_x = [L_x \, x]. \tag{2.9}$$

Analog Computer variables will always be bracketed in these notes.

Example 2.3. Again consider Equation (2.1). Solving for the derivative we obtain,

$$\frac{dx}{dt} = 5 - .1x, \qquad x(0) = 0 . \tag{2.10}$$

To get this equation in terms of the computer variable, multiply and divide each term by $1/L_x$, which in this case is 5.

$$\frac{d}{dt}\left(\frac{5x}{5}\right) = 5 - .1\left(\frac{5x}{5}\right), \qquad x(0) = 0. \tag{2.11}$$

Regroup the constants so that all variables are computer variables:

$$5\frac{d}{dt}\left[\frac{x}{5}\right] = 5 - .5\left[\frac{x}{5}\right], \qquad \left[\frac{x}{5}\right](0) = 0, \tag{2.12}$$

or

$$\frac{d}{dt}\left[\frac{x}{5}\right] = 1 - .1\left[\frac{x}{5}\right], \qquad \left[\frac{x}{5}\right](0) = 0. \tag{2.13}$$

If other amplifiers were present, a similar procedure would be followed for each.

STEP 5. Draw the scaled analog diagram using the equations obtained in step 4. Label all computer variables on the diagram. The final diagram should have the same form as the unscaled diagram except for different pot values and amplifier gains. Thus, Equation (2.12) results in Figure 2.6.
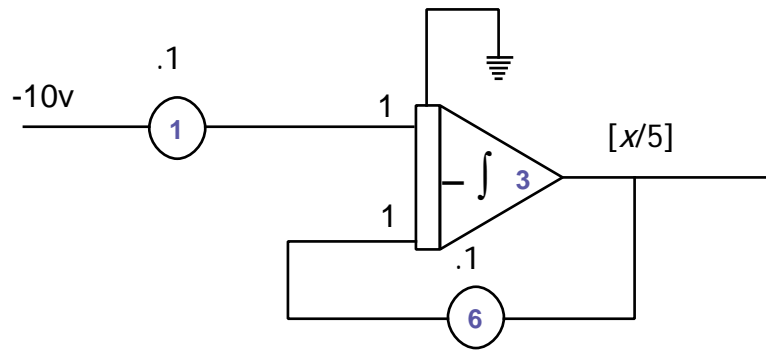
Figure 2.6: Scaled Diagram

The output of the analog diagram of Figure 2.6 is shown in Figure 2.7. It must be remembered that [x/5] represents the analog variable in volts. To find the actual value of x, Equation (2.9) must be used. At t_1 the value of the computer variable [x/5] is measured as 5 volts or 0.5 of a unit, i.e.,

$$[x/5] = 5, \quad \text{or} \quad x = 25.$$

Constants are realized in analog simulations by patching a $\pm$10v reference to a pot set to some value. To be consistent with the method of magnitude scaling, the pot setting must be found by the same formula as before. For this purpose we suppose that *the level of the $\pm$10v reference is* 10, which becomes the "level in" in the formula.
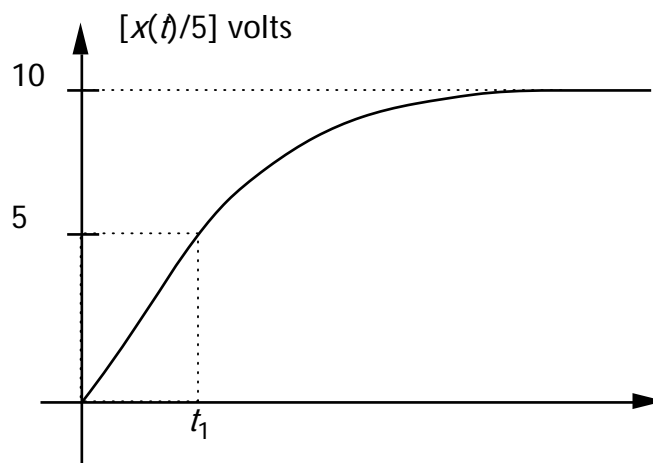
Figure 2.7: Time Response for Example 2.3

When patching an initial condition, the gain is 1, the level is 10, and the level out is the level of the variable for the initial condition. The coefficient is the value of the variable at $t = 0$. The following examples will help to illustrate these concepts and show how Equation (2.8) can be used to find the pot settings.

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5. Magnitude Scaling a Second Order System

We begin this section with an example.

Example 2.4. Simulate the following system and magnitude scale so that no overload occurs and maximum amplifier range is used.

$$\frac{d^2x}{dt^2} + 8\frac{dx}{dt} + 25x = 500, \quad x(0) = 40, \quad \dot{x}(0) = 150 \tag{2.14}$$

and with

$$|x|_{max} = 50, \quad |\dot{x}|_{max} = 250.$$
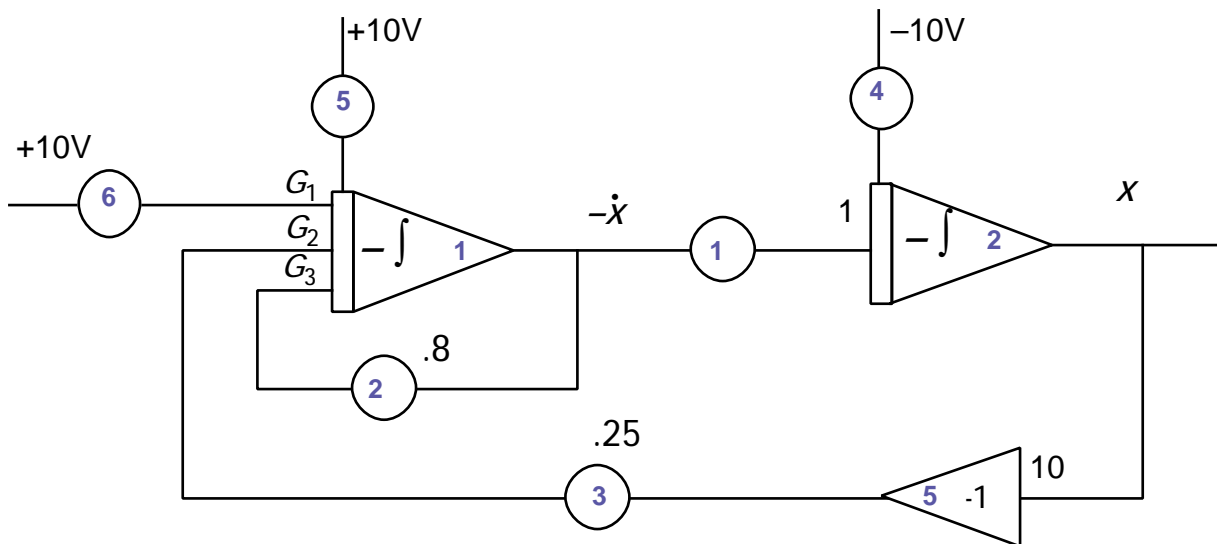
STEP 1. Draw an unscaled analog diagram.

Figure 2.8: Unscaled Analog Diagram for Example 2.4.

STEP 2. This step is not necessary since the maximum values are already specified in the problem statement.

STEP 3. Prepare a scaling table.

Problem Variable	Estimated Maximum	Level	Computer Variable	IC	Scaled IC
$-\dot{x}$	250	1/25	$[-\dot{x}/25]$	-150	[-6]
x	50	1/5	$[x/5]$	40	[8]
-2.5 x	125	1/12.5	$[-x/5]$	---	---

STEP 4. Write the scaled equations for each amplifier. Here is where we illustrate the use of Equation (2.8). Start with Figure 2.9.
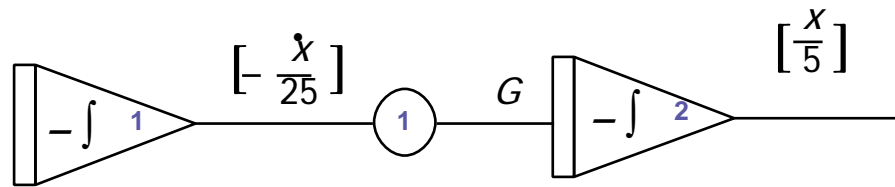

Figure 2.9: Establishing Integrator Outputs

$$K_1 = \left(\frac{1/5}{1/25}\right)\left(\frac{1}{G}\right) = \frac{5}{G} = .5, \quad \text{when} \quad G = 10.$$

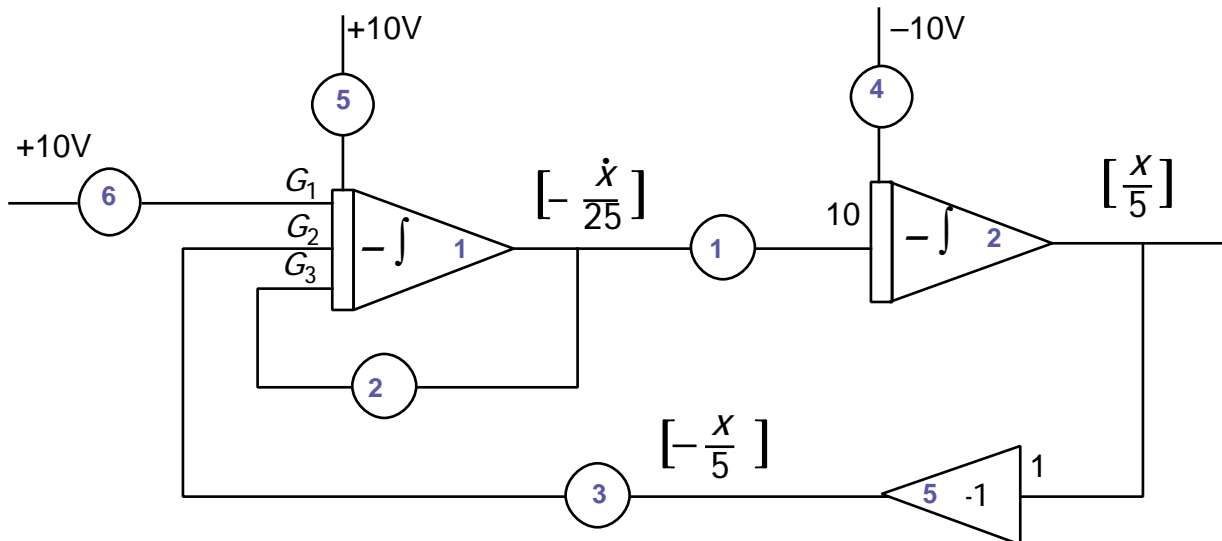Proceeding on, we complete the rest of the diagram,

Figure 2.10: The Final Scaling Process

and compute

$$K_2 = \left(\frac{1/25}{1/25}\right)\left(\frac{8}{G_1}\right) = .8, \quad \text{when} \quad G_1 = 10$$

$$K_3 = \left(\frac{1/25}{1/5}\right)\left(\frac{25}{G_2}\right) = .5, \quad \text{when} \quad G_2 = 10$$

$$K_4 = \left(\frac{1/5}{10}\right)\left(\frac{40}{1}\right) = .8, \qquad K_5 = \left(\frac{1/25}{10}\right)\left(\frac{150}{1}\right) = .6$$

$$K_6 = \left(\frac{1/25}{10}\right)\left(\frac{500}{G_3}\right) = .2, \quad \text{when} \quad G_3 = 10,$$

Note that on the Comdyna GP-6 computer resistor values of 5KΩ and 50KΩ and capacitors 2 μfd and 20 μfd are supplied with each integrator. Thus, any gain value between 0 and 100 may be obtained by proper choice of the input resistor-feedback capacitor combination and by using a pot.

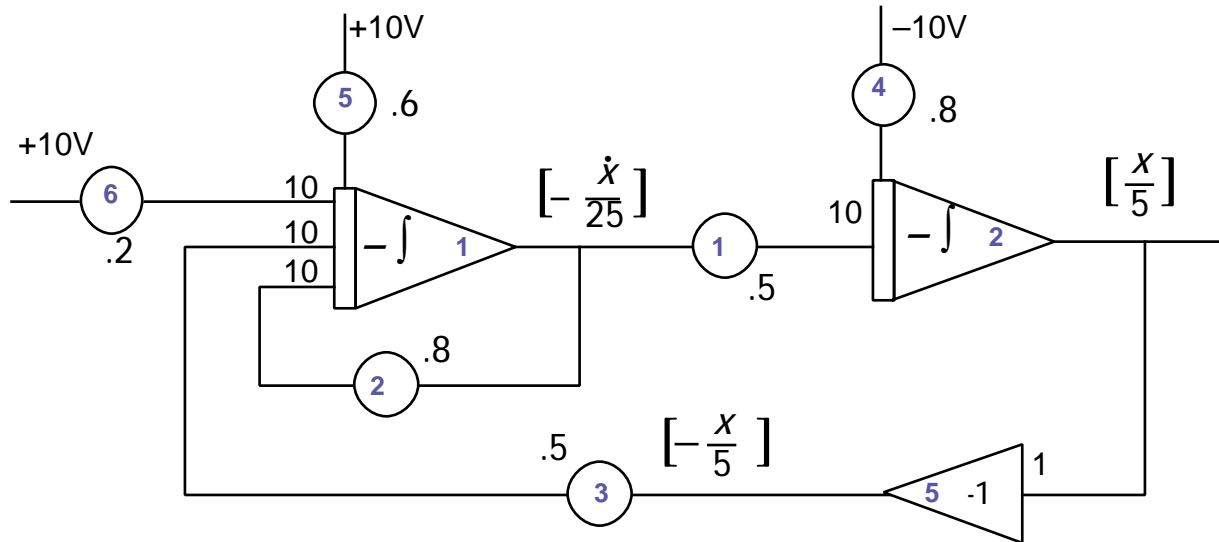**STEP 5**. Draw the scaled analog computer diagram. A patch panel diagram is included in Fig. 2.12.
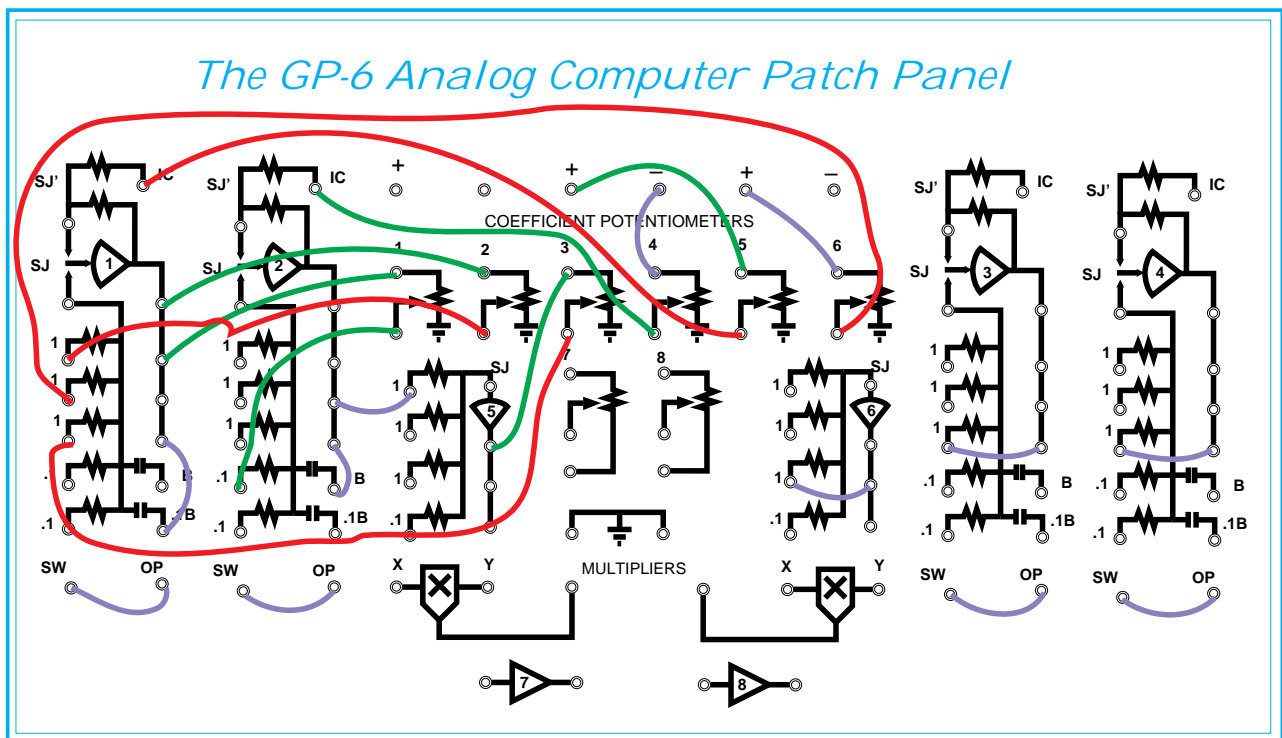

Figure 2.11: A Fully Scaled Diagram

Figure 2.12: GP-6 Wiring Diagram for the System of Example 2.4

Example 2.5. As another example, magnitude-scale the following problem so that no overload occurs and maximum amplifier range is used.

$$\frac{d^2x}{dt^2} + 2\frac{dx}{dt} + 25x = 0, \quad x(0) = 20, \dot{x}(0) = 0. \tag{2.15}$$

This example will be worked by a short cut method. Estimated maximum values are,

$$|x| \leq 20, \quad \text{and} \quad |\dot{x}| \leq 100. \tag{2.16}$$

Methods to obtain these estimates will be derived in Section 7 of this chapter. Solving for the highest order derivative,

$$\ddot{x} = -25x - 2\dot{x}. \tag{2.17}$$

The level constants are:

$$L_x = \frac{10}{20} = 1/2, \quad L_{\dot{x}} = \frac{10}{100} = 1/10 . \tag{2.18}$$

Multiplying and dividing Equation (2.17) by the level constants, we obtain

$$\ddot{x} = -25(2)\left[\frac{x}{2}\right] - 2(10)\left[\frac{\dot{x}}{10}\right], \tag{2.19}$$

where $\left[x/2\right]$ and $\left[\dot{x}/10\right]$ are the computer variables. From the initial conditions we obtain,

$$\left[\frac{x}{2}\right](0) = 10, \qquad \left[\frac{\dot{x}}{10}\right](0) = 0. \tag{2.20}$$

In order for $-\left[\dot{x}/10\right]$ to be the output of an amplifier, $\left[\ddot{x}/10\right]$ must be its input. Realizing this, we divide Equation (2.17) by 10 to obtain,

$$\frac{\ddot{x}}{10} = -5\left[\frac{x}{2}\right] - 2\left[\frac{\dot{x}}{10}\right]. \tag{2.21}$$

The magnitude-scaled analog computer simulation diagram appears in Figure 2.5.
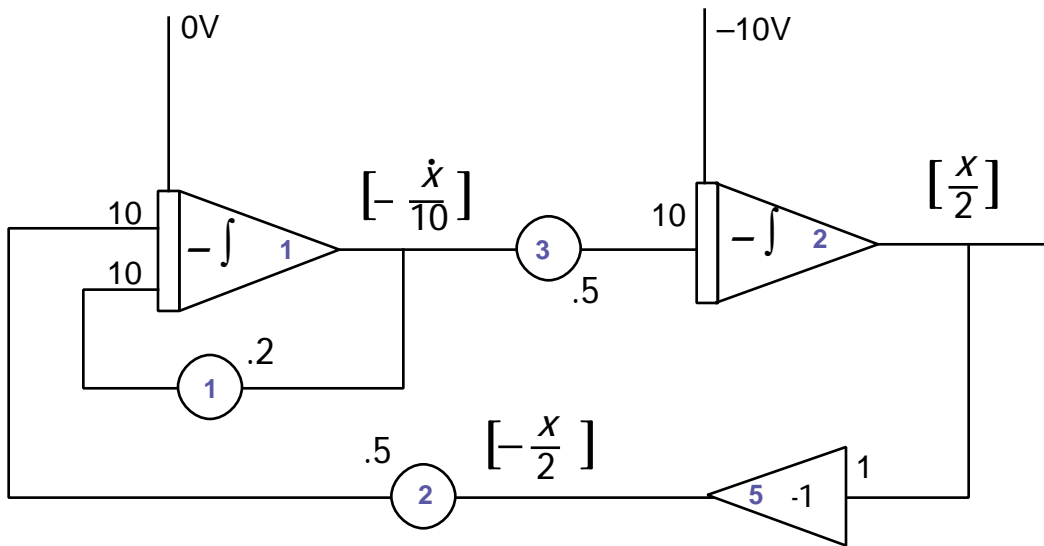
Figure 2.13: Scaled Diagram for Example 2.5

NOTE: While setting pots in any circuit containing amplifiers, overloads may occur. The reason for this is that in the POT SET mode of the computer 10 volts is internally applied to the upper terminal of each potentiometer. If any amplifier has a gain 10 input it is likely to cause an overload. These overleads can be avoided during the pot setting operation as follows. Connect a wire between an output junction and the summing junction of each amplifier output to vanish and solve the overload problem. *DO NOT FORGET TO REMOVE THESE SHORT CIRCUITS* before attempting the problem solution.   See Figure 2.14 for location of the short.
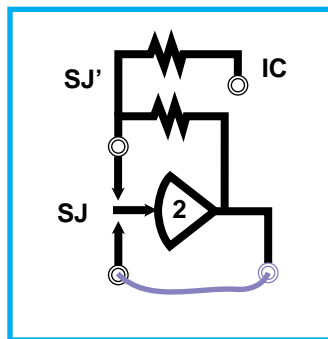
Figure 2.14: Short Circuit for Setting Potentiometers

6. Estimating Maximum Values in First Order Systems

Consider the first-order system

$$\frac{dx}{dt} = -ax + aK, \quad x(0) = x_o. \tag{2.22}$$

The solution of this differential equation is given by

$$x(t) = e^{-at}x(0) + K(1 - e^{-at}) \qquad (2.23)$$

The solution, (2.23), is shown in Figure 2.15a, for $0 < K < x(0)$, and in Figure 2.15b, for $0 < x(0) < K$. Graphing equation (2.23) for other possible combiniations of $x(0)$ and K, should convince the reader that

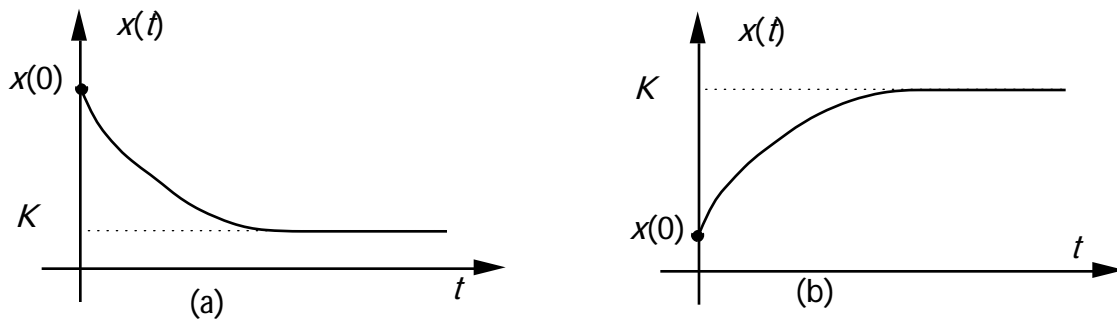$$|x|_{max} = \max\{|x(0)|, |K|\} \qquad (2.24)$$

Figure 2.15: First-Order Time Responses, (a) $0 < K < x(0)$, (b) $0 < x(0) < K$

7. Estimating Maximum Values in the Second Order Homogeneous Underdamped System.

We now consider the system

$$\ddot{x} + 2\zeta\omega_n\dot{x} + \omega_n^2 x = 0 \qquad (2.25)$$

where the initial conditions $x(0)$, and $\dot{x}(0)$ are given. We shall suppose that ζ and ω_n are positive (for stability), and also that $0 \leq \zeta < 1$ (so that the system is underdamped). If $\zeta = 0$, (undamped), the solution of (2.25) is given by

$$x(t) = \sqrt{x^2(0) + \frac{\dot{x}(0)^2}{\omega_n^2}} \sin(\omega_n t + \theta), \qquad (2.26)$$

where

$$\theta = \tan^{-1}\left(\frac{x(0)\omega_n}{\dot{x}(0)}\right). \qquad (2.27)$$

Differentiating (2.26), we get

$$\dot{x}(t) = \omega_n \sqrt{x^2(0) + \frac{\dot{x}(0)^2}{\omega_n^2}} \cos(\omega_n t + \theta) . \qquad (2.28)$$

To obtain estimates of the maximum values, we note that when $\zeta = 0$, that

$$|x|_{max} = \sqrt{x^2(0) + \frac{\dot{x}(0)^2}{\omega_n^2}}, \qquad |\dot{x}|_{max} = \omega |x|_{max} \qquad (2.29)$$

If the system is underdamped, and $\zeta << 1$ Equations (31) and (32) give pretty good estimates for the maximum values of $|x|$ and $|\dot{x}|$. If $\zeta \geq 1$, these estimates are conservative.

8. Estimating Maximum Values in the Forced Second Order Underdamped System

We consider the system

$$\ddot{x} + 2\zeta\omega_n\dot{x} + \omega_n^2 x = u(t), \quad x(0) = \dot{x}(0) = 0 \qquad (2.30)$$

We shall make a rough estimate of the maximum values by assuming $u(t) = Au_s(t)$ and $\zeta = 0$. The equation becomes

$$\ddot{x} + \omega_n^2 x = Au_s(t), \quad x(0) = \dot{x}(0) = 0 \qquad (2.30)$$

with the solution

$$x(t) = \frac{A}{\omega_n^2}(1 - \cos\omega_n t) \qquad (2.31)$$

or, by a trig. identity,

$$x(t) = \frac{2A}{\omega_n^2}\sin(\omega_n t/2) \qquad (2.32)$$

Thus, from (2.32) and by differentiating (2.31), we obtain

$$|x|_{max} = \frac{2A}{\omega_n^2}, \qquad |\dot{x}|_{max} = \frac{A}{\omega_n}, \qquad (2.33)$$

and thus that $|\ddot{x}|_{max} = A$. These estimated maximum values will again be quite good if the damping is low ($\zeta \approx 0$), but will be conservative if the system is critically damped or overdamped. How would you estimate max values if the initial conditions are not zero?

9. Time Scaling

Analog simulations can be adjusted to run faster or slower than real time. The time relation is:

$$\tau = \beta t \, , \tag{2.34}$$

where

$$\tau = \text{computer time,} \quad t = \text{real time,} \quad \beta = \text{scale factor}$$

A person can physically understand this equation and avoid confusion by remembering the following sentence:

The computer runs $1/\beta$ times as fast as real time.

Time scaling can be achieved by multiplying the gains of each input of every integrator by $1/\beta$. Therefore, we can adjust the previous pot setting formula to take care of magnitude *and* time scaling. We simply use a single pot for each input to the integrators such that:

$$\text{Pot Setting} = \left(\frac{L_{out}}{L_{in}} \right)\left(\frac{COEF}{gain} \right)\left(\frac{1}{\beta} \right) . \tag{2.35}$$

where the $1/\beta$ factor is added to the formula *only* when the pot to be set is patched to the input of an integrator.

NOTES:

1. There is no time variation on an initial condition, so the $1/\beta$ factor should be left out of the formula to set I.C. pots.

2. There is likewise no time variation for a non-integrating amplifier. Therefore $1/\beta$ factor should also be omitted from the formula to set pots at inputs to such an amplifier.

Example 2.6. Given:

$$\ddot{x} + 10\dot{x} + 25x = 20, \qquad x(0) = \dot{x}(0) = 0, \beta = 2.5. \tag{2.36}$$

Using the results of section 8, we estimate

$$\left| x \right|_{max} = \frac{2A}{\omega_n^2} = \frac{40}{25}, \quad \left| \dot{x} \right|_{max} = \frac{A}{\omega_n} = \frac{20}{5} = 4, \tag{2.33}$$

$$L_x = (10)\frac{25}{40} = 6.25, \quad L_{\dot{x}} = \frac{10}{4} = 2.5.$$
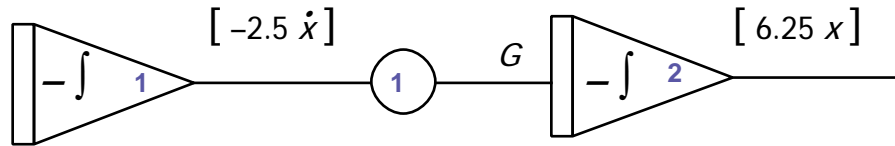
First, we draw the integrators.

Figure 2.16: Integrator Diagram for Example 2.6

$$G_1 \times \text{Pot Setting for \#1} = \left(\frac{6.25}{2.5}\right)\left(\frac{1}{2.5}\right) = 1.$$

Therefore, we may choose $G_1 = 1$ and $K_1 = 1$. Note that pot #1 may actually be eliminated. Now the feedback, I.C.'s, and constants may be entered onto the diagram (Figure 2.17). Here,

$$G_2 \times K_2 = \left(\frac{2.5}{2.5}\right)(10)\left(\frac{1}{2.5}\right) = 4, \quad \Rightarrow \quad G_2 = 10, K_2 = .4,$$

$$G_3 \times K_3 = \left(\frac{2.5}{6.25}\right)(25)\left(\frac{1}{2.5}\right) = 4, \quad \Rightarrow \quad G_3 = 10, K_2 = .4,$$

$$G_4 \times K_4 = \left(\frac{2.5}{10}\right)(20)\left(\frac{1}{2.5}\right) = 2, \quad \Rightarrow \quad G_4 = 10, K_2 = .2.$$
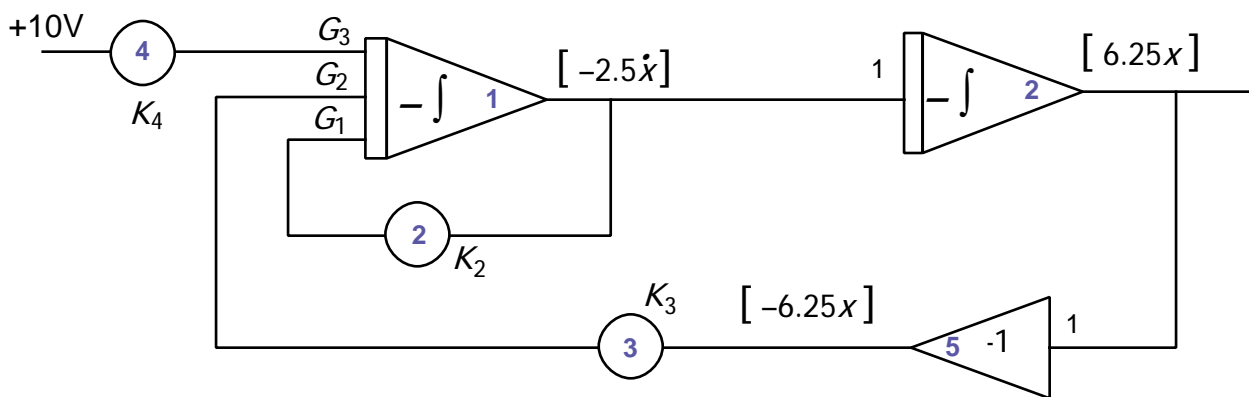
Figure 2.17: Setting the Scaling Values

Thus we have the final diagram
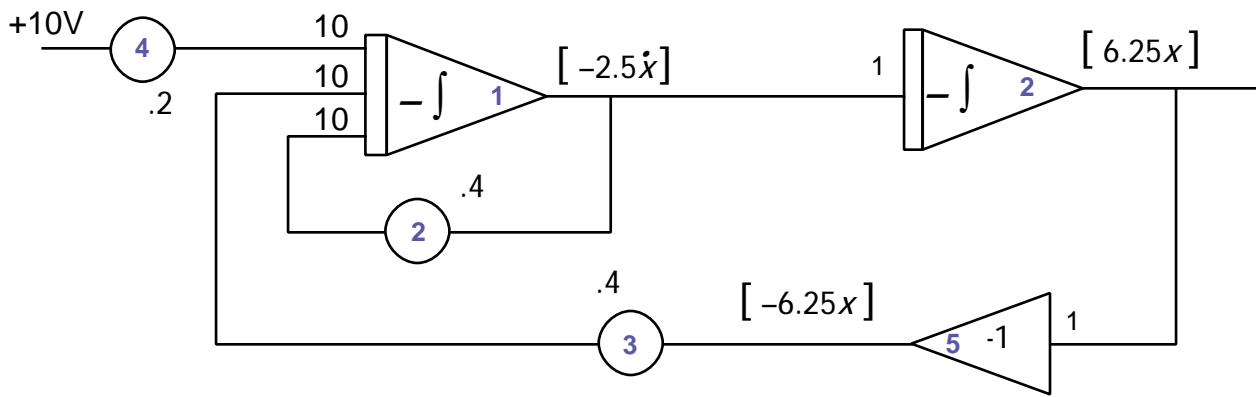
Figure 2.18: A Fully Time/Amplitude Scaled Diagram

10. Summary of Procedures for Developing a Scaled Analog Diagram

1. Write the differential equation to be solved in normal form.

2. Estimate maximum values for variables.

3. Determine all levels.

4. Draw all integrators needed. Put a pot between each pair of integrators and set them:

$$K = \left(\frac{L_{out}}{L_{in}} \right) \left(\frac{1}{gain} \right) \left(\frac{1}{\beta} \right) \; .$$

5. Fill in the feedback paths setting the pots by:

$$K = \left(\frac{L_{out}}{L_{in}} \right) \left(\frac{COEF}{gain} \right) \left(\frac{1}{\beta} \right) .$$

6. Add I.C.'s, setting the pots by:

$$K = \left(\frac{L_{out}}{10} \right) \left(\frac{COEF}{1} \right) \; .$$

7. Add constants, setting the pots by:

$$K = \left(\frac{L_{out}}{10} \right) \left(\frac{COEF}{gain} \right) \left(\frac{1}{\beta} \right) \; .$$

11. Repetitive Operation

At times it is desirable to repeat a solution many times in rapid succession, such as on an oscilloscope. Without any storage capability, it would be difficult to see details of the solution unless it is repeatedly swept across the screen at a rate that the eye would not be able to distinguish each individual sweep. The repetitive operation (**RO**) mode is available on most analog computers for this purpose. In order to repeat the solution it is necessary to backup in time and then repeat the desired time interval. Thus, the time dependent elements (integrators) must be controlled. Basically, when the computer is placed in the **RO** mode, the integrators are internally placed in the **IC** state for a time period sufficient to charge the capacitors to the initial condition value and then internally changed to the **OP** state for the desired time interval. Then the procedure is repeated.

Repetitive operation requires that a computer's integrator time constants be small enough to permit a high rate of repetitive solutions. Also, a timing unit is required to alternately place integrators in the **IC** and **OP** modes.

When the Mode selector is positioned to "**RO**:"

1. The repetitive operation timing unit provides a logic control that alternately changes integrator modes from initial condition to operate, the length of operate time period determined by the computer time setting.

2. The repetitive operation time unit provides a ramp output that may be used as the readout display's time base.

3. High speed repetitive operation capacitors are the summer/integrator amplifier's integration capacitors.

4. The meter input bus is connected to the rear terminal, meter input.

5. The high ends of all coefficient pots are connected to their patch panel terminations.

The Comdyna GP-6 provides some special outputs to facilitate the use of an oscilloscope or xy plotter as an output device both in slow time and repetitive operation.

In slow time mode, computer time and program time are the same. In the repetitive operation mode, 1 second of computer time corresponds to 2.5 msec real time, a ratio of 400:1. The

computer time selector is calibrated in program seconds, and hence, a setting of 20 would indicate 20 program seconds. To accurately set this variable output called **CTP** (compute time period) has been provided on the **x**-address switch. This is displayed in the pot set mode by setting the **y**/pot address to **GND/x** and **x** to **CTP**. The DVM will display program seconds/100 [i.e. .25 means 25 program seconds]. In both cases: during program operation, setting the **x** address to TIME will produce a -10 to +10 ramp at the **x** output on the back of the computer. This ramp can be used to drive the horizontal (or time) line of any desired output device. Thus, a display controlled by the computer time base will show exactly the same output display regardless of the mode of operation. This facility provides a means of displaying a solution on an oscilloscope during the preliminary design phase.

Chapter 3
Simulation of Transfer Functions

1. Differential Equations and Transfer Functions.

The primary usefulness of the analog computer is for simulating systems which can be modeled by a set of differential equations. A special case to be considered is the simulation of a system described by a transfer function. A transfer function is the ratio of the Laplace transform of the output variable to the Laplace transform of the input variable with all initial conditions equal to zero. Consider a system which is modeled by the differential equation,

$$\frac{d^2 x}{dt^2} + a_1 \frac{dx}{dt} + a_o x = b_o u + b_1 \frac{du}{dt}. \tag{3.1}$$

Here, $x(t)$ is the system output and $u(t)$ is the input. (Note that for a transfer function, the initial conditions are considered to be zero). Not only does the input appear, but a derivative of the input is also present. The transfer function describing this equation may be found by taking the Laplace transform of equation (3.1) and rearranging

$$s^2 X(s) + a_1 s X(s) + a_o X(s) = b_o U(s) + b_1 s U(s) \tag{3.2}$$

and factoring

$$(s^2 + a_1 s + a_o) X(s) = (b_o + b_1 s) U(s) \tag{3.3}$$

yields

$$\frac{X(s)}{U(s)} = \frac{b_1 s + b_o}{s^2 + a_1 s + a_o}. \tag{3.4}$$

Thus, if the differential equation describing a system is given, the transfer function for that system may be obtained. Also, given the transfer function (e.g. equation (3.4)), the differential equation (3.1) may be obtained by cross multiplying, taking the inverse Laplace transform, and rearranging.

Since a transfer function may be converted to a differential equation, then it seems possible to simulate transfer functions. There are, however, two difficulties that arise. The first difficulty is that the straight-forward implementation of some differential equations (such as in equation (3.1)) require the input to be differentiated. This is a problem because the analog computer does not have a differentiator, and because analog differentiators are inherintly noisy, high–bandwidth devices (unlike integration which is noise resistant).

The second difficulty arises because with a transfer function, usually only the input and the output are available and of interest. Programming the transfer function does not usually result in the intermediate derivatives, while programming the differential equation yields all the intermediate derivatives. Since the intermediate derivatives are not of immediate interest and programming the differential equation usually requires the use of more amplifiers, programming the transfer function is preferred.

Transfer function simulation is particularly useful when a problem can be described in terms of a block diagram. The transfer function representing each block can then be programmed on the computer and each block connected with the other blocks as dictated by the block diagram. In this way, the input and output of each block (transfer function) on the computer can be related to a meaningful physical variable of the system.

2. Programming Transfer Functions

The fundamental idea behind any kind of system programming on the analog computer is that when initial conditions are zero at $t = 0$, the Laplace variable, s, corresponds to differentiation in the time domain, and $1/s$ corresponds to an indefinite integration having $t = 0$ as its lower limit. Thus, if $\mathscr{L}\{f(t)\} = F(s)$, then $\mathscr{L}\left\{\frac{df(t)}{dt}\right\} = sF(s)$, while

$$\mathscr{L}\left\{\int_0^t f(\tau)\,d\tau\right\} = \frac{F(s)}{s}. \tag{3.5}$$

There are many *canonical* (standard) ways of breaking up a transfer function to obtain an *all–integrator realization*. An all–integrator realization of a transfer function is a circuit that has the given transfer function, but that uses only integrators as dynamic elements (no differentiators). We will not concentrate on all the possible realization, but will focus on one particular form.

3. The Direct Programming Technique

This approach, also called the "Solving for the Highest Derivative" approach, is one of the simplest, because it does not require knowledge of any of the system poles or zeros[*]. All the examples of Chapter 2 used this approach. The difference between what is considered here, and what was done in Chapter 2 is that it is possible for the transfer functions to have zeros. (The examples in Chapter 2 had no zeros). We will explain this method by example. Suppose we have the transfer function:

$$G(s) = \frac{Y(s)}{U(s)} = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + b_2 s + b_o} = \frac{N(s)}{D(s)},$$ (3.6)

where

$$N(s) = a_2 s^2 + a_1 s + a_o, \qquad D(s) = s^2 + b_2 s + b_o.$$ (3.7)

This is illustrated in Figure 3.1.
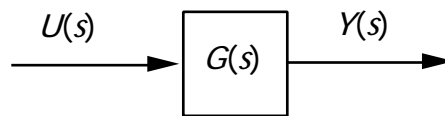
Figure 3.1: System Block Diagram

We decompose this system into two systems cascaded as in Figure 3.2.
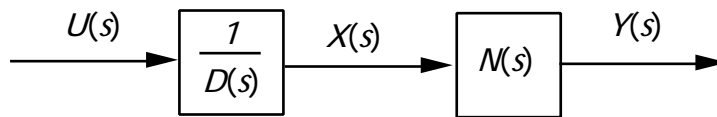
Figure 3.2: Cascaded Equivalent System

Notice that in cascading the two parts of the system, we have created the intermediate variable, $X(s)$. The transfer function from $U(s)$ to $X(s)$ has no zeros, and thus may be realized by using the approach of Chapter 2. Thus, we have

$$\frac{X(s)}{U(s)} = \frac{1}{s^2 + b_1 s + b_o} \quad \Rightarrow \quad s^2 X(s) = -b_o X(s) - b_1 s X(s) + U(s) .$$ (3.8)

Note that in the Laplace domain, $s^2 X(s)$ corresponds to the highest derivative of X. Thus, this highest derivative is given in terms of lower powers of s times $X(s)$ plus the input. Figure 3.3. shows the all-integrator diagram for this. Note that the time domain and the Laplace domain variables are shown.

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[*] This approach gives rise to the *controllable canonical form*.
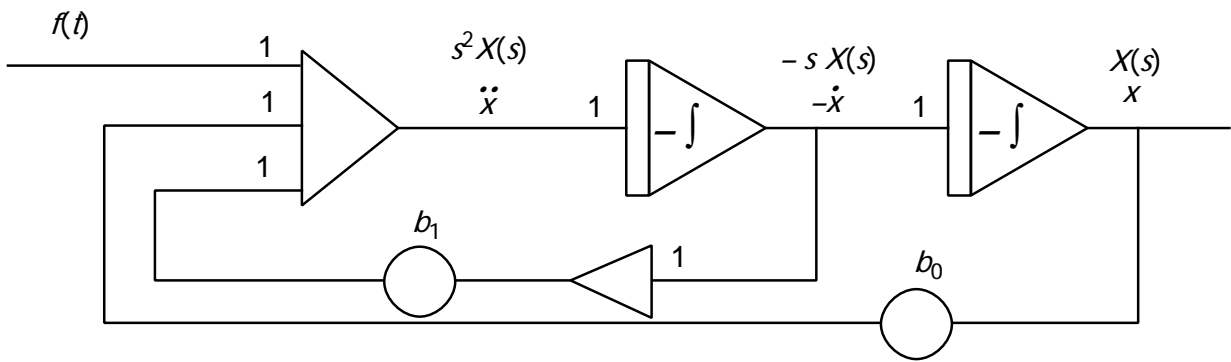
Figure 3.3: All–Integrator Diagram for the First Stage

The remaining tranfer function is given by

$$\frac{Y(s)}{X(s)} = N(s) = a_2 s^2 + a_1 s + a_o.$$

Multiplying through by $X(s)$, we obtain

$$Y(s) = a_2 s^2 X(s) + a_1 s X(s) + a_o X(s). \tag{3.9}$$

It would appear that because of the $s X(s)$ term and the $s^2 X(s)$ term, differentiators would be needed to obtain the necessary signals. However, these signals appear naturally in the realization of the transfer function from $U(s)$ to $X(s)$. Figure 3.4 illustrates the full integrator diagram.
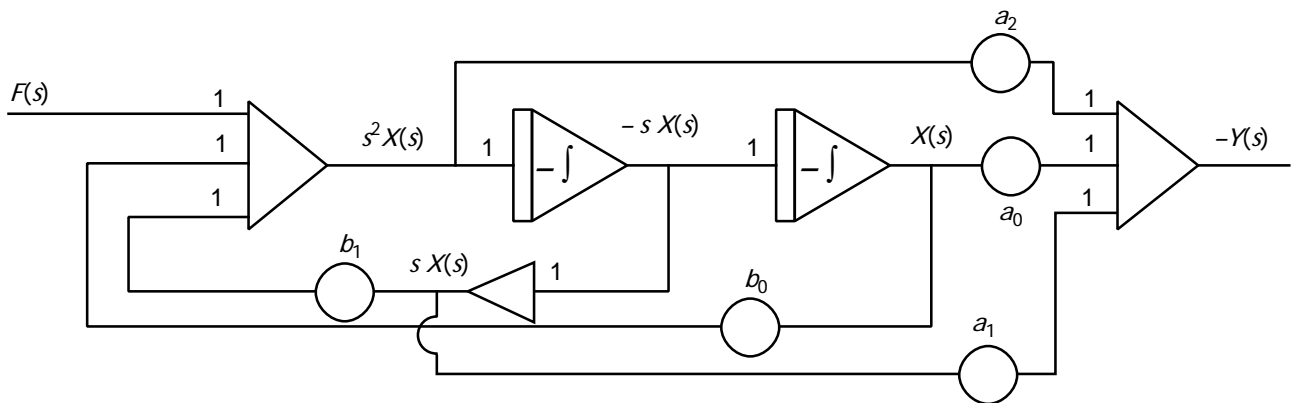
Figure 3.4: Complete All-Integrator Diagram

From Figure 3.4, three observations may be made. The first is that the output is actually $-Y(s)$. To obtain $+Y(s)$, it would be necessary to insert an inverter. The second observation is the use of the use of the inverter that yields $sX(s)$. Since that signal was already generated, it is certainly advantageous to use it than to insert another inverter to

generate the same signal. The third observation is that the summing inverter on the input cannot be incorporated into the first integrator.

4. Initial Conditions

Suppose that we wish to simulate a transfer function, but with initial conditions included. This is not a well-posed problem, as such, but we can work around that. Suppose that we are given the transfer function (3.6), but with the initial conditions:

$$y(0^-) = y_o, \qquad \dot{y}(0^-) = y_1. \qquad (3.10)$$

In order to incorporate these initial conditions, we need to "translate" them into the initial conditions of the actual integrators, and possibly the input.. We see, according to Figure 3.4,

$$
\begin{aligned}
y(0^-) &= a_o x(0^-) + a_1 \dot{x}(0^-) + a_2 \ddot{x}(0^-) \\
&= a_o x(0^-) + a_1 \dot{x}(0^-) + a_2 \left\{ -f(0^-) - b_1 \dot{x}(0) - b_o x(0) \right\} \qquad (3.11) \\
&= (a_o - a_2 b_o) x(0^-) + (a_1 - a_2 b_1) \dot{x}(0) - a_2 f(0^-)
\end{aligned}
$$

and also that

$$
\begin{aligned}
\dot{y}(0^-) &= a_o \dot{x}(0^-) + a_1 \ddot{x}(0^-) + a_2 \dddot{x}(0^-) \\
&= a_o \dot{x}(0^-) + a_1 \left\{ -f(0^-) - b_1 \dot{x}(0) - b_o x(0) \right\} \\
&\quad + a_2 \left\{ -\dot{f}(0^-) - b_1 \ddot{x}(0) - b_o \dot{x}(0) \right\} \qquad (3.12) \\
&= -b_o(a_1 - a_2 b_1) x(0^-) + \left[a_o - a_2 b_o - b_1(a_1 - a_2 b_1) \right] \dot{x}(0^-) \\
&\quad -(a_1 - a_2 b_1) f(0^-) - a_2 \dot{f}(0^-)
\end{aligned}
$$

We note that the initial states of the integrators can be rewritten in terms in the initial states of y and $\dot{y}$, and upon the input and its derivative. Note that when we take the Laplace transform of a signal, (like $f(t)$), we assume the signal to be zero, and all its derivatives to be zero. Thus, (3.11) and (3.12) simplify down to

$$
\begin{aligned}
y(0^-) &= (a_o - a_2 b_o) x(0^-) + (a_1 - a_2 b_1) \dot{x}(0^-) \\
\dot{y}(0^-) &= -b_o\left(a_1 - a_2 b_1\right) x(0^-) + \left[a_o - a_2 b_o - b_1(a_1 - a_2 b_1) \right] \dot{x}(0^-)
\end{aligned}
\qquad (3.13)
$$

or

$$y(0^-) = a_{11}x(0^-) + a_{12}\dot{x}(0^-)$$
$$\dot{y}(0^-) = a_{21}x(0^-) + a_{22}\dot{x}(0^-)$$

<div align="right">(3.14)</div>

giving us two equations and two unknowns. Thus, we may solve for $x(0^-)$ and $\dot{x}(0^-)$ in terms of $y(0^-)$ and $\dot{y}(0^-)$. We write equations (3.14) as a single matrix equation:

$$\begin{bmatrix} y(0^-) \\ \dot{y}(0^-) \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} x(0^-) \\ \dot{x}(0^-) \end{bmatrix} \quad \Rightarrow \quad \begin{bmatrix} x(0^-) \\ \dot{x}(0^-) \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}^{-1} \begin{bmatrix} y(0^-) \\ \dot{y}(0^-) \end{bmatrix} \qquad (3.15)$$

and thus we obtain

$$x(0^-) = \frac{\alpha_{22}\, y(0^-) - \alpha_{12}\, \dot{y}(0^-)}{\alpha_{11}\alpha_{22} - \alpha_{12}\alpha_{21}} \qquad (3.17a)$$

$$\dot{x}(0^-) = \frac{-\alpha_{12}\, y(0^-) - \alpha_{22}\, \dot{y}(0^-)}{\alpha_{11}\alpha_{22} - \alpha_{12}\alpha_{21}} \qquad (3.17b)$$

5. Scaling

The main difference between analog diagrams which simulate transfer functions and analog diagrams which simulate differential equations is that the amplifier inputs of the former are not simple derivatives, but are actually sums of problem variables. This makes scaling somewhat more difficult, but recalling our scaling principles will always enable us to muddle through!
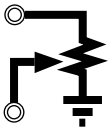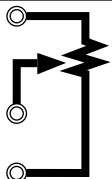
APPENDIX A

1. The GP–6 Display Panel
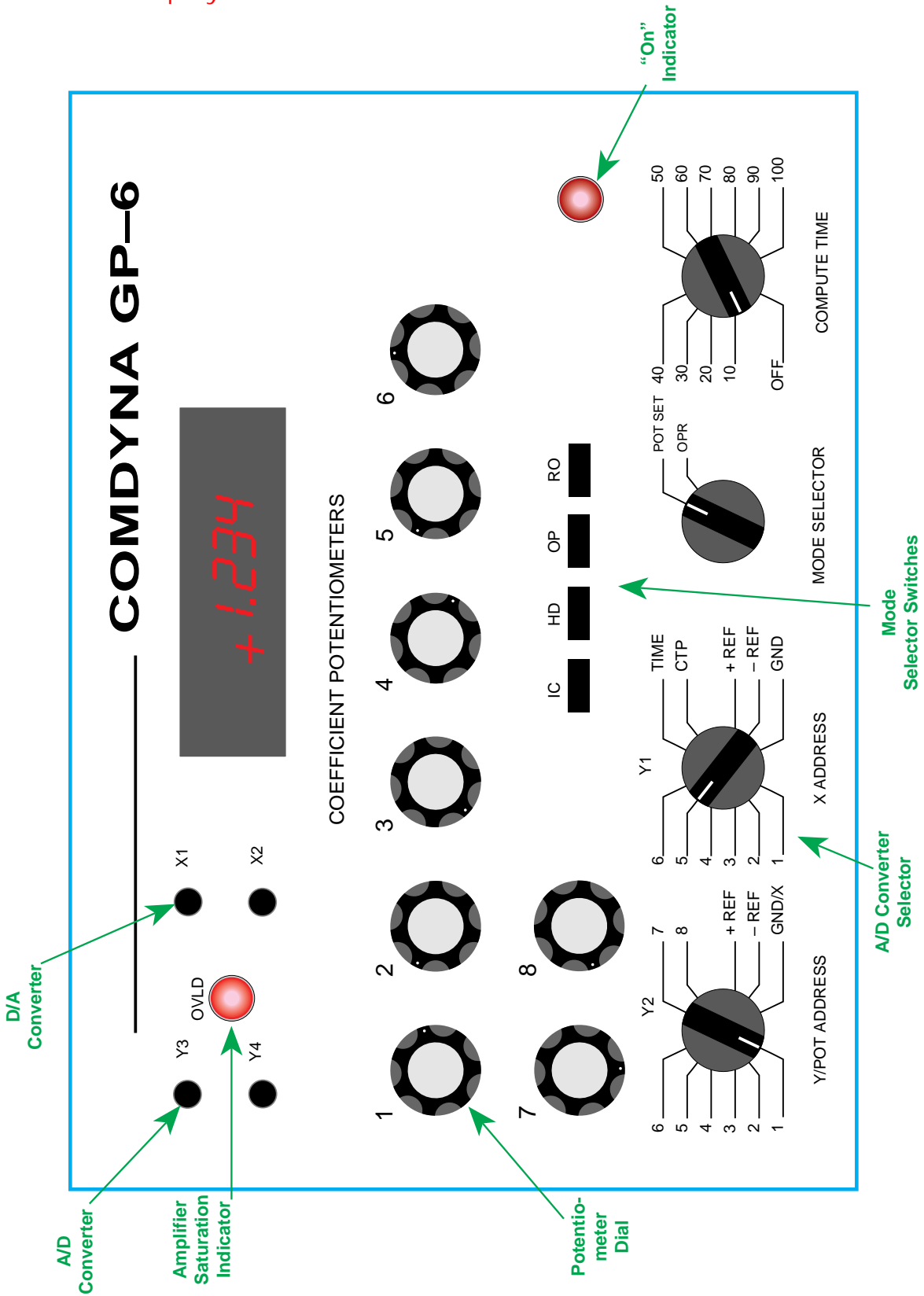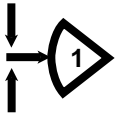
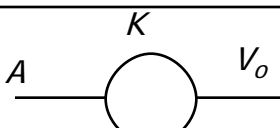## 2. The GP–6 Patch Panel
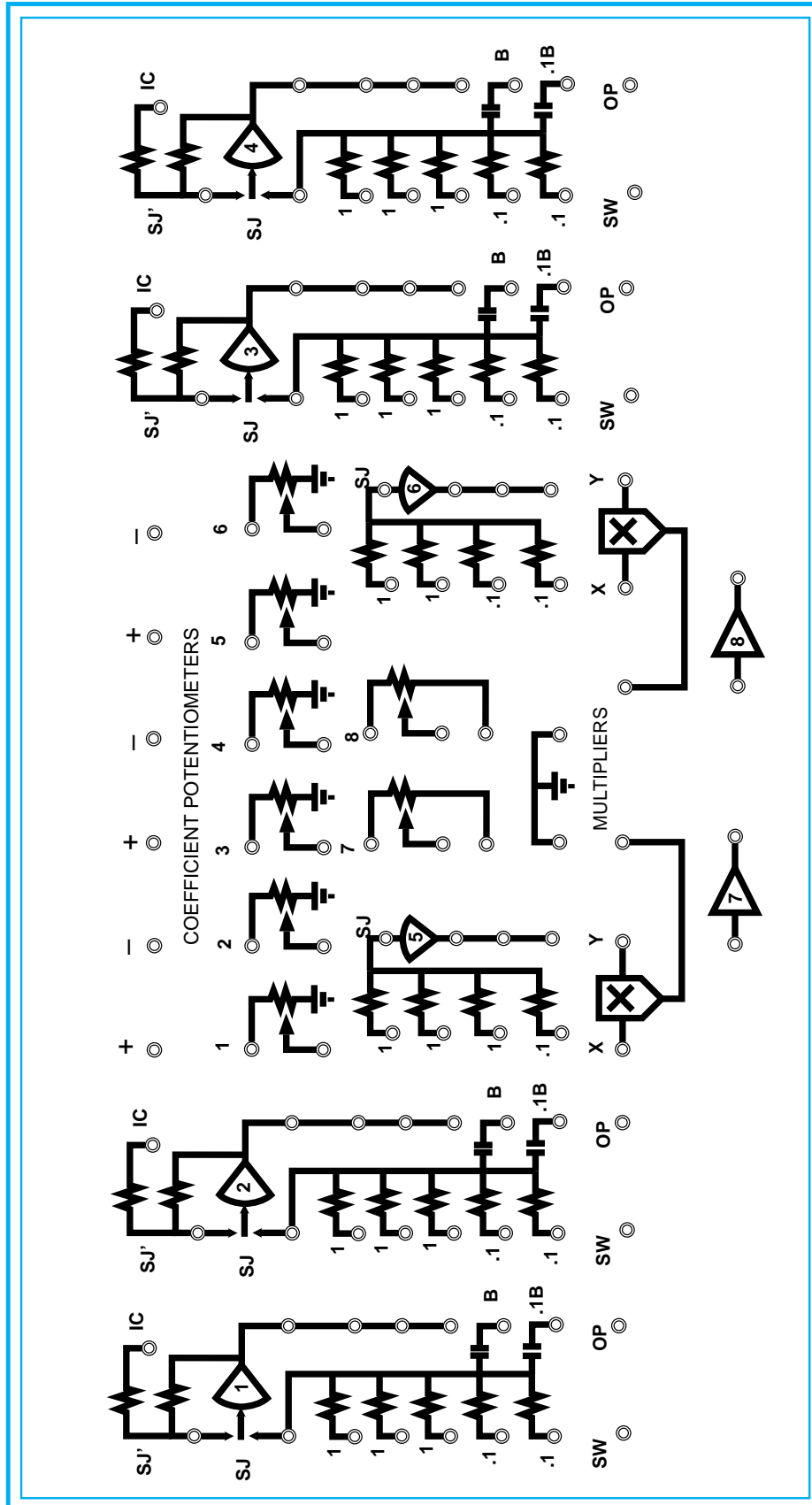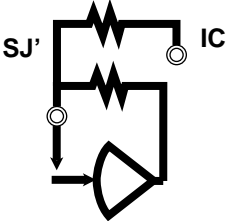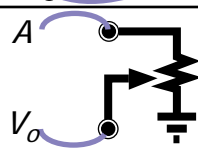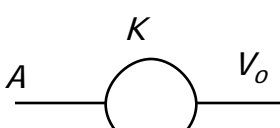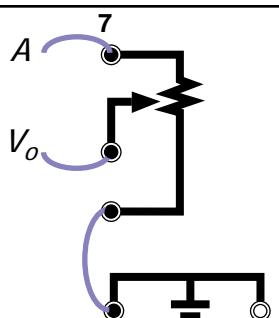
3. Patch Panel Components.
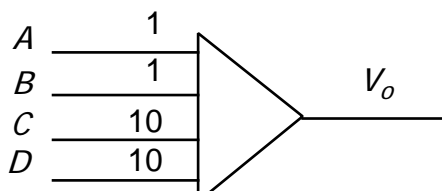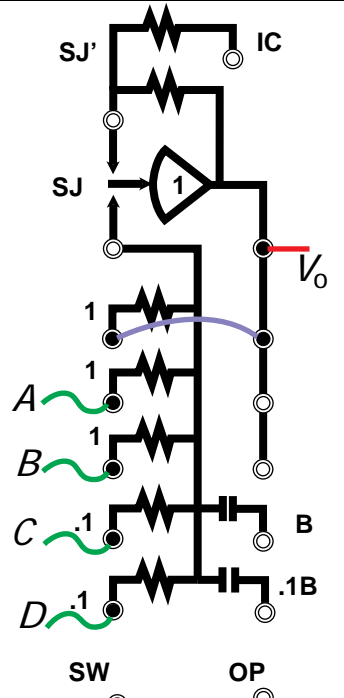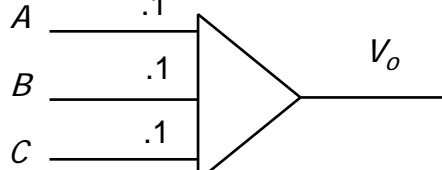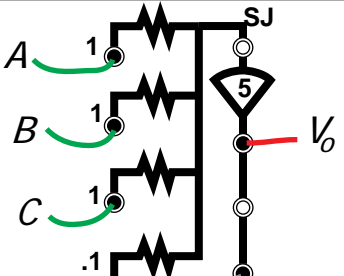
Patch panel graphics represent networks as they are applied in normal analog computer programming. Amplifiers 1 thru 6 may be used as summers or high gain operational amplifiers; amplifiers 1 thru 4 have electronic switch networks and may also be programmed as integrators. Amplifiers 7 and 8 are exclusively inverters. Potentiometers 1 thru 6 are attenuators. Potentiometers 7 and 8 have their bottom ends open and may be used as voltage dividers or attenuators. Multiplier networks have current output; with one amplifier each may be used as a multiplier, divider, squarer or square–root extractor.
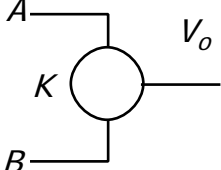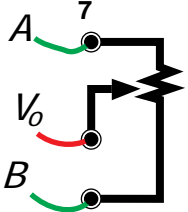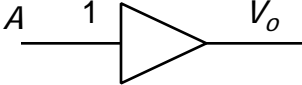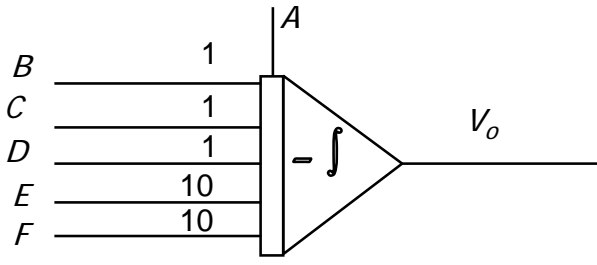
The following is a description of patch panel symbols:

SYMBOL		DESCRIPTION
+		Positive reference, considered unity for normalized programming. (Actual amplitude is 10 volts).
—		Negative reference, (Actual amplitude is 10 volts).
▽5		High gain operational amplifier
▷1		High gain operational amplifier with electronic switch
▷7		Inverter
SJ		The summing junction for amplifiers 1 thru 6. (Active for amplifiers 1 thru 4 when a logic "1" is applied to the "**SW**" switch control jack or when there is no switch control patching.)
SJ'		Alternate summing junction for amplifiers 1 thru 4. (Active when a logic "0" is applied to the "**SW**" switch control jack).
1 ⎰⎱		Standard input summing resistor, normalized to a unity value to simplify programming. (Actual value is 50 kΩ)
.1 ⎰⎱		Summing input resistor that has a value one tenth the standard (Actual value is 50 kΩ)
⊣⊢ B		Standard integrating capacitor input, normalized so that the 1 resistor and the B capacitor combination produces a one second time constant as referred to programming time scales. (Actual value is 20 μfd in the slow time mode and .05 μfd in the repetitive operation mode.)
⊣⊢ .1B		Integrating capacitor input that has a value one tenth the standard (Actual value is 2 μfd in the slow time mode and .005 μfd in the repetitive operation mode.)

SJ' (symbol with resistors, IC)		Resistor input to the **SJ'** summing junction. Amplifier becomes an inverter when **SJ'** is active. Normally used for integrator initial conditions. Input and feedback resistors may be used for summer operations. Input and feedback resistors may be used for summer operation by patching **SJ'** to **SJ**. (Actual value of input and feedback resistor is 50 kΩ)
(Attenuator symbol)		Attenuator, with input and wiper indicated by standard electrical symbol.
(Voltage divider symbol)		Voltage divider; top, bottom and wiper indicated by standard electrical symbol. Bottom must be patched to ground for attenuator operation. (Potentiometer value is 5 kΩ)
(System Ground symbol)		System Ground.
X (multiplier symbol) Y		Multiplier network. Produces a current proportional to the product of the inputs "**X**" and "**Y**"; normalized so that when connected to the summing junction of an operational amplifier with a 1 resistor feedback, and with reference applied to "**X**" and "**Y**," the amplifier output equals the reference.
SW		Electronic switch control input. With a logic "0" (ground, or positive voltage) the **SJ'** summing junction of the above amplifier is active and **SJ'** shuts off. With a logic "1" (–5 thru –15 volts) **SJ** is active and **SJ'** shuts off, the **SJ** summing junction is active but the summing resistor network is disconnected. "**HD**" logic is used for normal integrator hold mode operation.
OP		The computer's operate bus; provides integrator mode logic (slow time, repetitive operation or slave) as selected by the operator. Normal integrator operation requires that the "**OP**" bus be patched to the "**SW**" switch control input.

APPENDIX B: WIRING BASIC LINEAR COMPONENTS

FUNCTION	OPERATION	PATCHING
Summer Amplifiers 1 – 4	$V_o = -(A + B + 10C + 10D)$	
Summer Amplifiers 5 & 6	$V_o = -.1(A + B + C)$	
Attenuator Pots 1 – 6	$V_o = KA,\quad 0 \le K \le 1.$	
Attenuator Pots 7 & 8	$V_o = KA,\quad 0 \le K \le 1.$	

FUNCTION	OPERATION	PATCHING
Voltage Divider Pots 7 & 8	$$V_o = KA + (1-K)B$$	
Inverter Amplifiers 7 & 8	$$V_o = -A$$	
Integrator Amplifiers 1 – 4	$$V_o = -A - \int_0^t (B + C + D + 10E + 10F)\, d\tau$$	