ECE 482
Course Information

Fall Semester 2016
Professor E. Rosenbaum

Lectures
MWF 3:00 PM – 3:50 PM, 2017 ECEB

Instructor
Professor Elyse Rosenbaum (elyse@illinois.edu)
Office Hours: Tuesday 11:00 AM – 12:00 PM, 407 CSL
Friday 10:00 PM – 11:00 PM, 407 CSL
I occasionally need to shift my office hours to accommodate prelim exams, travel, etc., so always check the class webpage before coming to office hours on any given day. Any changes to my office hours will be listed under “Announcements.”

Teaching Assistants
Nicholas Thomson (nthomso2@illinois.edu)
Office Hours: Tuesday 4:00 PM – 6:00 PM, 3034 ECEB
Brady Salz (salz2@illinois.edu)
Office Hours: Monday 10:00 AM – 12:00 PM, 4034 ECEB

Textbook (required)

Other Reference Books (on reserve at Grainger Engineering Library)

Grading
First Midterm Exam 15%
Second Midterm Exam 15%
Final Exam 30%
Design Project Report 25%
The project assignment will be provided on Oct. 17. Students will work in instructor-assigned groups. Reports will be due at 3:00 PM on Dec. 7 (last day of classes). All the members of a group will receive the same grade except in the case that a group member does not make a good faith effort to contribute significantly.
Weekly Homework 15%
Homework is due in class on the due date, preferably before the lecture begins. Solutions will be posted on the class webpage. If you will not be able to attend class due to a job interview, conference trip, etc., you may turn in your homework early by giving it to a TA or the instructor. Late homework will not be accepted. We will drop each student’s lowest homework grade of the semester before calculating the total score; therefore, students who fall ill should not request a make-up assignment. A student who is seriously ill for more than 7 consecutive days should contact the instructor. Students are permitted to engage in discussion of the course material and approaches to solving the homework problems with each other. Ultimately, however, homework is to be completed individually. Plagiarized work will receive a score of zero and the student will be reported to the ECE department for possible disciplinary action.
ECE482 Web Site
http://courses.engr.illinois.edu/ece482/
Check the web site a few times per week - this is where all announcements will be posted, including corrections to homework assignments and changes to office hours. It is your responsibility to check the website regularly. Tutorial material and user guides for the EDA tools are available on the web site.

ECE482 Piazza
http://piazza.com/illinois/fall2016/ece482/home
All questions regarding the homework assignments, homework solutions or exams should be posted to Piazza. If you haven’t used Piazza before, it’s a web board which helps to coordinate common questions. If you were not automatically registered, clicking the above link should allow you to join the forum. It is the primary means of staff-student communication outside of class hours. The TAs or instructor will check this forum multiple times per day and will post responses to any queries. Email should be used only for matters of a personal nature.

Classroom Decorum
Students are welcome and encouraged to ask questions anytime during the class period. Class lectures will often cover material that is not in the textbook; therefore, it is recommended that you be present both physically and mentally for the entire 50 minutes. Cell phones and other handheld communication devices should be turned off and placed out of sight. If you miss class, you should obtain a copy of a classmate’s notes. If you arrive late to class, do not disrupt the lecture by walking to the front of the room to hand in your homework; instead, give it to the instructor or the TA immediately after the lecture has concluded.
8/22 Introduction
8/24 MOSFET threshold voltage
8/26 MOSFET I-V model
8/29 Static characteristics of inverters
8/31 Previous topic, continued
9/2 Dynamic characteristics of inverters
9/7 Previous topic, cont.
9/9 Device and interconnect capacitance; Power
9/12 Circuit simulation; Layout tools (Class may be held in the ECEB Linux EWS lab – details will be posted on the class website)
9/14 Layout tools, cont.; Design rules; IC fabrication
9/16 Transistor sizing
9/19 Previous topic, cont’d
9/21 Inverter chain (super buffer)
9/23 Combinational logic: complementary static CMOS
9/26 Gate layout; Estimating gate delay
9/28 Midterm 1
9/30 Previous topic, cont.
10/3 Logical effort
10/5 Previous topic, cont.
10/7 Ratioed logic
10/10 Pass transistor logic
10/12 Dynamic logic; Domino logic
10/14 np-CMOS; MODL
10/17 Sequential logic circuits
10/19 Static latches and registers
10/21 Dynamic latches and registers
10/24 Midterm 2
10/26 Pipelining
10/28 RLC interconnect models
10/31 Buffer insertion
11/2 Previous topic, cont.
11/4 Adder designs
11/7 Low power design techniques
11/9 Previous topic, cont.
11/11 Semiconductor memories
11/14 Control logic for memory
11/16 SRAM
11/18 Previous topic, cont.
11/28 DRAM
11/30 Previous topic, cont.
12/2 New CMOS technologies
12/5 I/O circuits; Variability and yield
12/7 Review
12/9 Final Exam (8:00 AM – 11:00 AM)