Diffusion Capacitance

\[ C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sw}} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER} = C_j L_S W + C_{jsw}(2 L_S + W) \]

Drawing assumes LOCOS isolation. Obsolete, but consistent with many examples in text. Formula is ok.
Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\phi_0})^m} \]

- \( m = 0.5 \): abrupt junction
- \( m = 0.33 \): linear junction
Interconnect: Wires connecting transistors

http://www.avii-ic.com/Figure5r.gif

Interconnect has parasitic resistance and capacitance