ECE 482
Final Exam: Useful Formulas

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Unified Model

\[ V_T = V_{T0} + \gamma \left( \sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right) \]

\[ I_D = 0: \text{ valid for NMOS if } V_{GS} \leq V_{Tn}; \text{ valid for PMOS if } V_{GS} \geq V_{Tp} \]

\[ I_D = k \left( V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot \left( 1 + \lambda \cdot V_{DS} \right): \text{ valid for NMOS if } V_{GS} > V_{Tn}; \text{ valid for PMOS if } V_{GS} < V_{Tp} \]

\[ |V_{min}| = MIN \left( |V_{DS}|, |V_{GT}|, |V_{DSAT}| \right); \quad k = k \frac{W}{L} \]

\[ C_{DB} = C_{j0} \cdot AD \cdot K_{eq} + C_{jsw} \cdot PD \cdot K_{eqsw}, \quad C_{SB} = C_{j0} \cdot AS \cdot K_{eq} + C_{jsw} \cdot PS \cdot K_{eqsw} \]

\[ K_{eq} = \frac{\phi_0^m}{(V_{final} - V_{init})(1-m)} \left[ (\phi_0 - V_{final})^{1-m} - (\phi_0 - V_{init})^{1-m} \right], \text{ where } V_{init} \text{ and } V_{final} \text{ refer to the} \]

\[ \text{voltage across the PN junction (these values are generally less than or equal to zero)} \]

CMOS Inverter

The following equations for \( V_{M}, V_{IL} \) and \( V_{IH} \) are valid if both devices are velocity saturated when \( V_{in} = V_{M} \).

\[ V_M = \frac{V_{Tn} + \frac{V_{DSATn}}{2}}{1 + r} \cdot \left( V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2} \right) \]

\[ r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} \]

\[ \text{Or, given the value of } V_M, \quad \frac{(W)_p}{(W)_n} = \frac{k_p V_{DSATp} \left( V_M - V_{Tn} - \frac{V_{DSATn}}{2} \right)}{k_n V_{DSATn} \left( V_{DD} - V_M + V_{Tp} + \frac{V_{DSATp}}{2} \right)} \quad (\text{Assumes } L_n = L_p.) \]

\[ V_{IH} \equiv V_M - \frac{V_M}{g}, \quad V_{IL} \equiv V_M + \frac{V_{DD} - V_M}{g}, \quad g = -\frac{1}{I_{Dn}(V_M)}, \quad k_n V_{DSATn} + k_p V_{DSATp} \]

Other cases:

Condition 1: \( V_M < (V_{DSATn} + V_{Tn}) \)

Condition 2: \( V_M > (V_{DD} + V_{DSATp} + V_{Tp}) \)

If Condition 1 is satisfied but not Condition 2, then

\[ \frac{W_p}{W_n} = \frac{k_n(V_M - V_{Tn})^2}{2k_p V_{DSATp}(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2} - V_M)} \]

If Condition 2 is satisfied but not Condition 1, then

\[ \frac{W_p}{W_n} = \frac{2k_n V_{DSATn}(V_M - V_{Tn} - \frac{V_{DSATn}}{2})}{-k_p(V_M - V_{DD} - V_{Tp})^2} \]

If both Condition 1 and Condition 2 are satisfied, then

\[ \frac{W_p}{W_n} = \frac{k_n(V_M - V_{Tn})^2}{-k_p(V_M - V_{DD} - V_{Tp})^2} \]

Dynamic Power: \( P_{dyn} = C_L V_{DD}^2 f_{0-1} \)
\[ t_{pLH} \approx \frac{0.5V_{DD}C_{L}}{W(W/\mu n)^{2/3}l_{DSATp}}, \quad t_{pHL} \approx \frac{0.5V_{DD}C_{L}}{W(W/\mu p)^{2/3}l_{DSATn}}, \quad \text{where } I_{DSAT} \equiv k \cdot V_{DSAT} \cdot \left( V_{DD} - |V_T| - \frac{|V_{DSAT}|}{2} \right) \]

\[ t_p = (t_{pLH} + t_{pHL})/2; \quad t_p = t_p0 \cdot \left( 1 + \frac{C_{EXT}}{C_{int}} \right) \]

This may also be written as \( t_p = t_p0 \cdot \left( 1 + \frac{C_{EXT}}{S \gamma C_{min}} \right) \), where \( \gamma = C_{int}/C_G \) is a technology-dependent constant. In the equation, \( S \) denotes the size of the inverter whose delay is being calculated, relative to the size of a minimum-sized inverter. \( t_p0 \) denotes the delay of an unloaded inverter and \( C_{min} \) is the input capacitance of a minimum-sized inverter.

**Transistor Sizing**

In the circuit shown below, \( t_{p1} \), the delay of inverter #1 is minimum when \( \beta = \beta_{opt} \).

\[
\beta_{opt} = \sqrt{\frac{1 + C_{wire}}{C_{in1} + C_{in2}}}, \quad \alpha = \frac{k_v V_{DSATn} (V_{DD} - V_{n} - V_{DSATn}/2)}{k_p V_{DSATp} (V_{DD} + V_{p} + V_{DSATp}/2)}
\]

A superbuffer is a chain of \( N \) inverters driving a load \( C_{OUT} \) (\( C_{OUT} \) does not include the intrinsic capacitance of the \( N^{th} \) inverter). To minimize the delay through the inverter chain, size each inverter \( f \) times bigger than the one before it, and let \( f = \left( \frac{C_{OUT}}{C_{g1}} \right)^{1/N} \). The corresponding propagation delay is

\[ t_p = N t_p0 \left( 1 + \frac{f}{\gamma} \right) \]. If you are able to adjust the value \( N \), you can minimize the delay from the input of the first inverter to the output load by setting \( N = N_{opt} \), where \( N_{opt} = \frac{\ln(C_{OUT}/C_{g1})}{\ln(f_{opt})} \) and \( f_{opt} \) is the solution to the design equation \( f_{opt} = \exp\{1 + \gamma/f_{opt}\} \). The numeric solution of the design equation is plotted below.
Elmore delay formula: \( t_p = 0.69 \tau \). For the case of a simple RC chain (no branches), \( \tau = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j \), and if \( R_i = R \) and \( C_i = C \) for all \( i \), then \( \tau = \frac{CRN(N+1)}{2} \).

**Logical Effort**

\[
D \equiv \frac{t_p}{t_{p0,_{inv}}} = \sum_{j=1}^{m} \left( p_j + \frac{f_j g_j b_j}{\gamma} \right), \text{m = # gates along delay path}
\]

- \( g \) – logical effort; \( g_{inverter} = 1 \), \( g_{nandN} = (N+2)/3 \), \( g_{norN} = (2N+1)/3 \)
- \( p \) – parasitic term; \( p_{inverter} = 1 \), \( p_{nandN} = N \), \( p_{norN} = N \)
- \( f \) – electrical effort; \( f_j = \frac{C_{g,j+1}}{C_{g,j}} \) where \( C_{g,m+1} = C_{out} \)
- \( b \) – branching effort; \( b_j \) is equal to the number of identical gates connected at the output of the \( j \)th gate. Or, more generally, \( b_j = \frac{C_{on} + C_{off}}{C_{on}} \), where \( C_{on} \) is the input capacitance of the \((j+1)\)th gate along the signal path (the path whose delay you are trying to minimize) and \( C_{off} \) is the capacitance contributed by any other gates at the \( j \)th gate’s output (these other gates belong to signal branches).

To minimize \( D \), choose \( g_j \cdot f_j \cdot b_j = h \) for all \( j = 1 \) to \( m \).

\[
h = \left[ \frac{C_{out}}{C_{g1}} \prod_{j=1}^{m} g_j \cdot b_j \right]^{\gamma/m}
\]

**Charge Sharing:**

\( C_i \) is the total internal node capacitance that participates in charge sharing; \( C_o \) is the capacitance at the output (dynamic) node. Equations are given for the case of n-type dynamic logic and the case that the internal nodes are initially discharged (this gives worst case \( \Delta V_{out} \)). The analysis also assumes that the gate voltage of all “on-state” n-channel transistors in the circuit is \( V_{DD} \).

If \( \frac{C_i}{C_o} \leq \frac{V_{Th}}{V_{DD} - V_{Th}} \), then \( V_{out} = V_{DD} - \frac{C_i}{C_o} \cdot (V_{DD} - V_{Th}) \). Else, \( V_{out} = \frac{C_o}{C_o + C_i} \cdot V_{DD} \).