Init

Before we begin:

- Open a terminal
- Type “module load ece482”
- Type “module load Synop<tab>”
- Type “source /class/ece482/init.sh”
  - Hopefully optimized soon
- If it doesn’t work, run “module --ignore_cache avail”
What is SPICE?

- **SPICE** stands for
  - Simulation
  - Program with
  - Integrated
  - Circuit
  - Emphasis

- Developed at UC Berkeley by Laurence Nagel

- Lots of flavors:
  - Open source simulators include ng-spice, gnuCAP
  - Closed source can be free (LTSpice, TINA-TI) or expensive (PSpice, HSPICE)
Why SPICE?

```
.MODEL nmos NMOS (
+LMIN = 2.4E-07 LMAX = '5.1E-07-dxl'
+LEVEL = 49 TNOM = 25 XL = '3E+8-dxl'
+XW = '0 + dxw' VERSION = 3.1 TOX = toxn
+CALCACM = 1 SVFTFLAG = 0 VFBFLAG = 1
+XJ = 1E-07 NCH = 2.354946E+17 LLN = 1
+LWN = 1 WLN = 1 WNN = 1
+BUNIT = 2 DWG = 0 DWB = 0
+VTH0 = '0.4321336+dvthn' LVTH0 = 2.081814E-08 WWTH0 = 3.470342E-11
+PVTH0 = -6.721795E-16 K1 = 0.32812529 LK1 = 9.238362E-08
+WK1 = 2.878255E-08 PK1 = -2.426481E-14 K2 = 0.0402828
+LK2 = -3.208392E-08 WK2 = -1.154901E-08 PK2 = 9.192045E-15
+K3 = 0 DVT0 = 0 DVT1 = 0
+DVT2 = 0 DVTOW = 0 DVT1W = 0
+DVT2W = 0 NLX = 0 DW = 0
+K3B = 0 VSAT = 7.586954E+04 LVSA = 3.094656E+03
+WVSAT = -1.747416E-03 PVSAT = 8.820956E+10 UA = 8.924498E+10
+LUA = -1.511745E-16 WUA = -3.509821E+17 PUA = 3.08778E-23
+UB = 8.928832E-21 LUB = -1.655745E-27 WUB = 2.03282E-27
+PUB = 3.4578E-34 UC = -1.364265E-11 LUC = 1.170473E-17
+WUC = -1.256705E-18 PUC = -6.249644E-24 RDSW = 447.8871
+PRWB = 0 PRWG = 0 WR = 0.99
+U0 = 0.06005258 LU0 = -6.31976E-09 WU0 = -8.819531E-09
+PU0 = 3.57209E-15 A0 = -1.468373 LAO = 6.419548E-07 2.579193E-12
+WAO = 5.512414E-07 PA0 = -9.22928E-14 KETA = -0.04922795
+UKETA = 2.360844E-08 WKETA = 1.560385E-08 PKETA = -5.93877E-15
+A1 = 0.02659908 LA1 = -6.511454E-09 A2 = 1
+AGS = -4.01637 LAGS = 1.090294E-06 WAGS = 1.162021E-06
+PAGS = -3.108579E-13 B0 = 0 B1 = 0
+VOFF = -0.1829426 LVOFF = 9.941631E-09 WVOFF = 1.585862E-08
+PVOFF = -2.832958E-15 NFACTOR = 0.6790636 LNFACOR = 3.454948E-08
+WNFACTOR = 1.501016E-07 PNFACTOR = -2.955951E-14 CIT = 2.218499E-04
+LCIT = 1.076934E-10 WCIT = -3.286884E-10 PCIT = 1.656928E-16
+CDS = 0 CDSCB = 0 CDSCD = 0
+ETAO = 1.2155758E-04 LETAO = -1.037758E-11 WETA0 = 3.030225E-11
+PETA0 = 1.529656E-17 ETAB = 3.548681E-03 LETAB = 1.791374E-09
+WETAB = 6.892628E-10 PETAB = 3.481742E-16 DSUB = 0
+PCLM = 3.593838 LPCLM = -6.874146E-07 WPCLM = 5.664574E-08
+PPCLM = -1.33176E-15 PDIBLC1 = 0 PDIBLC2 = 5.379674E-03
+LPDIBLC2 = 7.808481E-09 WPDDIBC2 = 5.516945E-10 PDIBLC2 = -2.784957E-16
+PDIBLCB = -0.1229374 LPDIBLCB = 4.956215E-08 WPDDIBC = 3.299946E-08
+PPDDIBC = 9.624918E-15 DROUT = 0 PSCBE1 = 5.98377E-09
+LPSCBE1 = 28.64041 WPSCBE1 = 15.1754 PPSCBE2 = 7.93313E-06
+PSCBE1 = 1.842585E-06 LPSCBE2 = 2.871008E-12 WPSCBE2 =
+PPSCBE2 = -1.301972E-18 PVAG = -2.015254E-03 LPVAG = 1.017757E-09
+WPVAG = 3.67622E-10 PPVAG = -1.55418E-16 DELTA = 0.01
+LDELTA = 1.492454E-08 WDELTA = -6.71663E-09 PDELTA = 3.40752E-15
+ALPHA0 = 0 BETA0 = 30 KT1 = -0.2579945
+LKT1 = -1.664985E-08 WKT1 = -1.633463E-08 PKT1 = 3.755864E-15
+KT2 = -0.05347481 LKT2 = 8.244731E-09 WKT2 = 1.13705E-09
+PKT2 = -1.240924E-15 AT = 1.132632E-04 LAT = 6.469047E-03
+WAT = 6.82922E-04 PAT = -4.152429E-10 UTE = -2.309089
+LUTE = 1.662427E-07 WUTE = 1.244801E-07 PUTE = 5.627924E-14
+UA1 = -3.461758E-10 LUA1 = 1.747495E-16 WUA1 = 1.420656E-14
+PUA1 = 7.171442E-23 UB1 = 0 UC1 = -2.38157E-12
+LU1C = -2.895726E-18 WUC1 = -1.990052E-17 PUC1 = 1.004497E-23
+KT1L = 0 PRT = -1E-18 CJ = cj
+MJ = 0.4960069 PB = -0.9173808 CJSW = cjsw
+MJSW = 0.443145 PBSW = -0.9173808 CJSWG = cjswen
+MJSW = 0.443145 PBSW = 0.9173808 HDIF = hdfs
+RS = 0 RD = 1.0e-5
+ACM = 12 LDIF = 1.2E-07 RSH = 4.5
+CTA = 7.707813E-04 CTP = 5.512283E-04 PTA = 1.167715E-03
+PTP = 1.167715E-03 N = 1 XTI = 3
+CGDO = 'cgon CGSO = 'cgon' CAPMOD = 0
+QNQSMOD = 0 XPART = 1 CF = 0
+TLEV = 1 TLEVC = 1 JS = 1E-06
+JSW = 5E-11 )
```
Netlists

- “The resistor is connected to the voltage source, which is also connected to the other resistor and a capacitor to ground”

Vsource VDD 0  Vsource VDD 0  Vsource VDD 0
R1 VDD 0       R1 VDD midpoint R1 VDD midpoint
R2 VDD midpoint R2 midpoint 0   R2 midpoint topcap
C1 midpoint 0   C1 VDD 0       C1 topcap 0
SPICE Decks

- The decks describe the netlist + simulations
- Write a deck in your favorite text editor

```plaintext
CMOS Inverter by Dabin Zhang
.lib '/class/ece482/models25' TT
mn1 VSS INPUT OUTPUT VSS nmos l=0.24u w=0.36u
mp1 VDD INPUT OUTPUT VDD pmos l=0.24u w=0.72u
cLoad OUTPUT VSS 50fF
vSupply VDD 0 2.5
vGND VSS 0 0
vIn INPUT 0 pulse( 0 2.5 0.1ns 0.1ns 0.1ns 2ns 4ns )
.dc vIN start=0 stop=2.5 step=0.01
.tran 1ps 8ns
.option post
.end
* This is a comment line
```
First Impressions Count

- SPICE classifies each line by the first character in it (case insensitive)

<table>
<thead>
<tr>
<th>Character</th>
<th>Type</th>
<th># of Ports</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>. (period)</td>
<td>Command</td>
<td>N/A</td>
<td>Many!</td>
</tr>
<tr>
<td>+</td>
<td>Continue previous</td>
<td>N/A</td>
<td>Many!</td>
</tr>
<tr>
<td>M</td>
<td>MOSFET</td>
<td>4</td>
<td>Model + Params</td>
</tr>
<tr>
<td>R</td>
<td>Resistor</td>
<td>2</td>
<td>Value</td>
</tr>
<tr>
<td>L</td>
<td>Inductor</td>
<td>2</td>
<td>Value</td>
</tr>
<tr>
<td>C</td>
<td>Capacitor</td>
<td>2</td>
<td>Value</td>
</tr>
<tr>
<td>V</td>
<td>Voltage Source</td>
<td>2</td>
<td>Value</td>
</tr>
<tr>
<td>I</td>
<td>Current Source</td>
<td>2</td>
<td>Value</td>
</tr>
</tbody>
</table>
Comments

- First line is always a comment
- * comments out the rest of the line

```verbatim
CMOS Inverter by Dabin Zhang
.lib '/class/ece482/models25' TT
mn1 VSS INPUT OUTPUT VSS nmos l=0.24u w=0.36u
mp1 VDD INPUT OUTPUT VDD pmos l=0.24u w=0.72u
cLoad OUTPUT VSS 50fF
vSupply VDD 0 2.5
vGND VSS 0 0
vIn INPUT 0 pulse( 0 2.5 0.1ns 0.1ns 0.1ns 2ns 4ns )
.dc vIN start=0 stop=2.5 step=0.01
.tran 1ps 8ns
.option post
.end

* This is a comment line
```
Libraries + Corners

- We have 3 libraries available in this class:
  - .lib '/class/ece482/models25' [TT, SS, FF, SF, FS]
  - .lib '/class/ece482/models18' MOS
  - .lib '/class/ece482/models13' MOS

<table>
<thead>
<tr>
<th>Corner</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Wire</th>
<th>$V_{DD}$</th>
<th>Temp</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>T</td>
<td>T</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>timing specifications (binned parts)</td>
</tr>
<tr>
<td>T</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>timing specifications (conservative)</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>DC power dissipation, race conditions, hold time constraints, pulse collapse, noise</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>S</td>
<td>subthreshold leakage noise, overall noise analysis</td>
</tr>
<tr>
<td>S</td>
<td>S</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>S</td>
<td>races of gates against wires</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>S</td>
<td>F</td>
<td>F</td>
<td>S</td>
<td>races of wires against gates</td>
</tr>
<tr>
<td>S</td>
<td>F</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>pseudo-NMOS &amp; ratioed circuits noise margins, memory read/write, race of PMOS against NMOS</td>
</tr>
<tr>
<td>F</td>
<td>S</td>
<td>T</td>
<td>F</td>
<td>F</td>
<td>F</td>
<td>ratioed circuits, memory read/write, race of NMOS against PMOS</td>
</tr>
</tbody>
</table>
Components

MOSFETs

CMOS Inverter by Dabin Zhang
.lib '/class/ece482/models25' TT

mn1 VSS INPUT OUTPUT VSS nmos l=0.24u w=0.36u
mp1 VDD INPUT OUTPUT VDD pmos l=0.24u w=0.72u
cLoad OUTPUT VSS 50f

Sources

vSupply VDD 0 2.5
vGND VSS 0 0
vIn INPUT 0 pulse( 0 2.5 0.1ns 0.1ns 0.1ns 2ns 4ns )

Commands

.dc vIN start=0 stop=2.5 step=0.01
.tran 1ps 8ns
.option post
.end

* This is a comment line
Component Options

- **MOSFET**
  - M<name> <drain> <gate> <source> <body> <model> [L=] [W=] [AD=] [AP=] [AS=] [PS=]
  - mn1 OUTPUT INPUT VSS VSS nmos L=0.24u W=0.36u

- **Capacitor**
  - C<name> <node 1> <node 2> [value]
  - cLoad OUTPUT VSS 50f

- **Independent DC Source**
  - V<name> <node 1> <node 2> [value]
  - vSupply VDD 0 2.5

- **Pulse Source**
  - V<name> <node 1> <node 2> PULSE(V1 V2 Tdelay Trise Tfall Width Period)
  - vIN INPUT 0 pulse( 0 2.5 0.1n 0.1n 0.1n 2n 4n )
Commands

- HSPICE has a huge command set, here are common ones we’ll use
- You ALWAYS NEED THE FIRST TWO in this class

<table>
<thead>
<tr>
<th>Command</th>
<th>Function</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>.lib</td>
<td>Load a library (first line)</td>
<td>.lib '/class/ece482/models25' TT</td>
</tr>
<tr>
<td>.end</td>
<td>End the sim file (last line)</td>
<td>.end</td>
</tr>
<tr>
<td>.subckt</td>
<td>Defines a subcircuit</td>
<td>N/A</td>
</tr>
<tr>
<td>.dc</td>
<td>DC sweep</td>
<td>.dc vIN start=0 stop=2.5 step=0.1</td>
</tr>
<tr>
<td>.tran</td>
<td>Transient sweep</td>
<td>.tran 1ps 8ns [timestep timestep]</td>
</tr>
<tr>
<td>.option</td>
<td>Output options</td>
<td>.option post</td>
</tr>
<tr>
<td>.param</td>
<td>Create a variable</td>
<td>.param myVariable = 1e-12</td>
</tr>
<tr>
<td>.measure</td>
<td>Measure a value</td>
<td>.meas tran i(mp1) WHEN v(vIN) = 2.5</td>
</tr>
<tr>
<td>.print</td>
<td>Print a value</td>
<td>.print v(vIN)*i(mp1)</td>
</tr>
</tbody>
</table>
Complex Examples

- **Subcircuit with parameter**

```
.param wp=0.72u
.subckt xinv IN OUT VDD VSS
mn1 VSS IN OUT VSS nmos l=0.24u w=0.72u
mp1 VDD IN OUT VDD pmos l=0.24u w=wp
.ends
```

```
myinv IN OUT VDD VSS xinv
```

- **Measuring delay (+ continues the line, written to .mt#)**

```
.measure tran rise_delay trig v(IN) val=1.25 fall=1
+ targ v(OUT) val=1.25 rise=1
```
Parameter Sweeps

- Can do sweeps during analysis to see many results at once
- Syntax is “sweep var start stop step”

```
.param wp=0.72u
<more netlist>
mp1 VSS INPUT OUTPUT VSS pmos l=0.24u w=wp
<more netlist>

.tran 50ps 8ns sweep wp 1u 5u 1u
```
How to Run

- Save the file as “example-inv.cir” or “example-inv.net”
  - File extension doesn’t matter, just to help organization

- Run the command “hspice example-inv.cir > example-inv.out”
  - Output redirection optional but easier to debug if things aren’t working
  - “>error ***** hspice job aborted” means error
  - “>info: ***** hspice job concluded” means successful simulation

- Now run “scope &” to start the visual analyzer
C Scope

CosmosScope (TM)

File Plotfile Signals

Signal filter

Open Plotfiles

Plotfiles

Close Plotfiles

Display Plotfiles

Setup...

Match All

Close

Open Plotfiles

Directory: /home/salz2/ece482.work/ECE482Test

test.sw0
test.tr0

File names: 

Files of type: HSPICE (*.tr*, *.ac*, *.sw*, *.ft*)
Examples + Questions?