Init

Before we begin:

- Open a terminal

- Type “module load ece482”

- Type “module load Synop<tab>”

- Type “source /class/ece482/init.sh”
  - Hopefully optimized soon

- If it doesn’t work, run “module --ignore_cache avail”
IC Design

- Circuit design is an iterative process
- We have models
- We estimate using math
- Implement estimations
- Simulate implementations
- Verify simulations vs specs
- Repeat till satisfactory
Cadence Design Systems

- Start by making sure you’re in “~/ece482.work”
- Type “virtuoso &” to launch the program

- Cadence has 3 levels of hierarchy:
  - Libraries
    - Attached to a certain technology node [250nm, 180nm]
    - Contain lots of cells, grouped by functionality
  - Cells
    - Represent circuit elements [MOSFET, AND gate, ALU]
    - Contains numerous views
  - View
    - Represents individual cell implementation
    - Schematic Symbol, Verilog, Layout
Getting Started

- Two windows pop up immediately
- Library manager
- Command Interface Window (CIW)
Making A Library

- File -> New -> Library
- “Attach to an existing technology library”
- Most important step is CHOOSING THE RIGHT TECHNOLOGY
- 250nm is tsmc03d
- 180nm is tsmc02d
- 130nm may be available later
Basic Layout

- Schematic capture is handled well by the tutorial on the website
- Quickly go over a simple inverter layout (no p-cells)
- Select the library you just made
- File -> New Cell
  - Name: “Example482”
  - Type: “layout”
Slicing

- Most likely used to seeing circuits sliced vertically like below
- ICs are three-dimensional, layout done “top-down”
- Refer to the tutorial on the website for tool questions
Inverter Comparisons

- Let’s look at a simple inverter in schematic, cross-section, and layout views

![Inverter Diagram](image-url)
Inverter Comparisons

- Device Identification

![Inverter Diagram]

W = 0.72um
L = 0.24um
Inverter Comparisons

- **Body/Bulk Ties**

![Inverter Diagram](image)
Inverter Comparisons

- Sources

![Diagram of an inverter circuit with labels W=0.72um, L=0.24um for both NMOS and PMOS transistors.]
Inverter Comparisons

- Gates + Drains

VDD

IN

W=0.72um
L=0.24um

OUT

W=0.72um
L=0.24um

VSS
Inverter Comparisons

- Contacts!
- Not shown on cross section
- Small black boxes in layout
- Need a something in order to go between layers
Three Letters

- **Design Rule Check [DRC]**
  - Foundry gives us rules on minimum, maximum dimensions
  - How small wire can be, how close two wires can be, dimensions of contacts
  - Run DRC, fix errors before going to next step

- **Layout Vs Schematic [LVS]**
  - Checks if your layout matches your schematic

- **Parasitic EXtraction [PEX]**
  - Models interconnects with resistance and capacitance
  - Returns that info as a netlist
  - Simulate netlist in HSPICE, see performance difference
Just For Fun

- Here’s a chip I made this Spring [TSMC 65nm CMOS]
- Let’s zoom until we see individual transistors
Just For Fun

- Here’s a chip I made this Spring [TSMC 65nm]
- Let’s zoom until we see individual transistors
Just For Fun

- Here’s a chip I made this Spring [TSMC 65nm]
- Let’s zoom until we see individual transistors
Just For Fun

- Here’s a chip I made this Spring [TSMC 65nm]
- Let’s zoom until we see individual transistors
Just For Fun

- Here’s a chip I made this Spring [TSMC 65nm]
- Let’s zoom until we see individual transistors
Questions?