Fall Semester 2017

ECE 482
Course Information

Professor E. Rosenbaum

Lectures
MWF 3:00 PM – 3:50 PM, 2017 ECEB

Instructor
Professor Elyse Rosenbaum (elyse@illinois.edu)
Office Hours: Tuesday 11:00 AM – 12:00 PM, 407 CSL
Thursday 3:00 PM – 4:00 PM, 407 CSL
I occasionally need to shift my office hours to accommodate prelim exams, travel, etc., so always check the class webpage before coming to office hour on any given day. Any changes to my office hours will be listed under “Announcements.”

Teaching Assistants
Yang Xiu (yangxu2@illinois.edu)
Office Hours: Monday 4:00-6:00 PM, 2036 ECEB
Jie Xiong (jiex2@illinois.edu)
Office Hours: Tuesday 1:30-3:30 PM, 2036 ECEB

Textbook (required)

Other Reference Books (on reserve at Grainger Engineering Library)

Grading
First Midterm Exam 15%
Second Midterm Exam 15%
Final Exam 30%
Design Project Report 25%
The project assignment will be provided at the end of October. Students will work in instructor-assigned groups. Reports will be due at 3:00 PM on Dec. 13. All the members of a group will receive the same grade except in the case that a group member does not make a good faith effort to contribute significantly.

Weekly Homework 15%
Homework is due at 3:00 PM, unless otherwise noted. Solutions will be posted on the class webpage. If you will not be able to attend class due to a job interview, conference trip, etc., you may turn in your homework early by giving it to the TA or the instructor. We will drop each student’s lowest homework grade of the semester before calculating the total score. Late homework will not be accepted. A student who is seriously ill for more than 7 consecutive days should contact the instructor so as not to be penalized for missing more than one assignment. Students are permitted to engage in discussion of the course material and approaches to solving the homework problems with each other. Ultimately, however, homework is to be completed individually. Plagiarized work will receive a score of zero and the student will be reported to the ECE department for possible disciplinary action.
ECE482 Web Site and Q&A Forum on Piazza

http://courses.engr.illinois.edu/ece482/
Check the web site a few times per week; this is where all announcements will be posted, including corrections to homework assignments and changes to office hours. It is your responsibility to check the website regularly. Tutorial material will also be available on the class web site.

http://piazza.com/illinois/fall2017/ece482/home
All questions regarding the homework assignments, homework solutions or exams should be posted to piazza. Registered class members should already be registered for this on-line forum; otherwise, clicking the above link will allow you to join. Piazza is the primary means of staff-student communication outside of class hours. The TAs or instructor will check this forum multiple times per day and will post responses to any queries. Email should be used only for matters of a personal nature.

Weekly reading assignments

A reading assignment will be written at the top of each problem set. Problem sets (i.e., homework assignments) will be posted each Wednesday at 3:00 PM. It is your responsibility to download the problem set and make note of the reading assignment. Paper copies of the assignments will not be provided after the first week of class.
8/28 Introduction to CMOS technology and digital circuits
8/30 Previous topic, continued
9/1 Threshold voltage
9/6 MOSFET I-V
9/8 Previous topic, cont’d
9/11 EDA Tools: layout, netlist extraction, and circuit simulation
9/13 Device and interconnect capacitance
9/15 Static characteristics of inverters
9/18 Previous topic, cont’d
9/20 Dynamic characteristics of inverters
9/22 Previous topic, cont’d
9/25 Elmore delay estimation
9/27 Transistor sizing
9/29 Previous topic, cont’d
10/2 Super buffer
10/4 RLC interconnect models
10/6 **Midterm 1**
10/9 Buffer insertion
10/11 Previous topic, cont’d
10/13 Combinational logic: complementary static CMOS
10/16 Gate layout
10/18 Estimating gate delay
10/20 Logical effort
10/23 Previous topic, cont’d
10/25 Ratioed logic; pass transistor logic
10/27 Previous topic, cont’d
10/30 Dynamic logic
11/1 Previous topic, cont’d
11/3 Sequential logic circuits
11/6 Static latches and registers
11/8 Dynamic latches and registers
11/10 **Midterm 2**
11/13 Previous topic, cont’d
11/15 Pipelining
11/17 Adder designs
11/27 Low power design techniques
11/29 Previous topic, cont’d
12/1 Semiconductor memories
12/4 Control logic for memory
12/6 SRAM
12/8 Previous topic, cont’d
12/11 DRAM
12/13 Review
12/18 **Final Exam** (1:30 PM – 4:30 PM)