Lab 8. Broadband Amplifier

Introduction

The goal of this lab is to design, simulate, and characterize a broadband small-signal amplifier that will operate over a frequency range of (at least) 10-100 MHz. You will investigate:

- S-parameter measurements using the network analyzer
- use of ADS software to simulate the linear performance of an amplifier
- measurement of 1 dB compression point
- measurement of two-tone third-order intercept level
- measurement of noise figure

The following amplifier design specifications are to be met:

1. \( \sim 18 \) dB gain over 1 decade (10-100 MHz). The gain characteristic should be as flat as possible.
2. \( \sim 50 \) Ω input and output impedances when used in a 50 Ω system (i.e. at least \( 15 \) dB input and output return loss from 10-100 MHz). Return loss is defined as \(-20 \log |S_{ii}|\) where \( i = 1 \) for input return loss and \( i = 2 \) for output return loss.
3. the amplifier should be unconditionally stable at all frequencies (verification, if time permits)

The nonlinear characteristics such as gain compression, intermodulation distortion, and noise are not specified in the requirements, but will be measured and evaluated.

Theoretical analysis of the linear regime of the broadband amplifier

There are basically two approaches that can be taken when designing an amplifier that must operate with reasonable gain and good input/output impedance match over a wide bandwidth. One approach is to use impedance transformation networks at the input and output of the active network and to design the networks so that the frequency-dependent variations in the active network’s gain and impedance are compensated for (to a certain extent) by the impedance transformation networks. It is difficult to simultaneously obtain a “flat” gain characteristic together with good impedance match over a wide bandwidth using this approach. The other approach, which is employed in this lab, is to employ negative feedback around the active device in an attempt to modify its characteristics (input/output impedance and power gain) such that they become more-or-less independent of frequency (over some bandwidth) and equal to some desired target values. Another advantage of employing negative feedback is that the properties of the circuit can be made to depend primarily on the values of the feedback circuit elements and to be more-or-less independent of the particular characteristics of the active device (such as transistor \( \beta \), etc.).

The circuit that will be used for the broadband amplifier is shown in Figure 8.1. Negative feedback is provided by series feedback resistor \( R_e \) and shunt feedback resistor \( R_f \). Both types of feedback are necessary in order for us to be able to control both the gain and the input/output impedances of the amplifier. As we shall see, the shunt feedback resistor can be selected to provide a simultaneous match to 50 Ω at both ports, and the series feedback resistor can be selected to set the gain of the amplifier. The transformer shown in the circuit functions as a broadband 4 : 1 impedance transformer which transforms a 50 Ω load impedance to approximately 200 Ω at the collector of the transistor, adds 6 dB to the gain (see Appendix details), and also provides a convenient pickoff point for the feedback provided by \( R_f \). This transformer must be constructed so that its properties are nearly independent of frequency. This circuit
should operate over a fairly wide bandwidth. In practice, bandwidth will be limited by parasitics (in the board, passive components, and transistor) and the properties of the broadband transformer.

![Figure 8.1: Unlabeled capacitors are coupling and bypass elements. The transformer is an off-the-shelf one: T1-1-KK81 from Mini-circuits. Unlabeled resistors are DC bias elements and have no essential function at RF frequencies (although they cannot be neglected when modeling the amplifier).](image)

In the circuit shown in Figure 8.1, it is assumed that the value of the feedback resistor, \( R_f \), is large enough so that it can also serve as one of the two resistors in the voltage divider that develops the base voltage. If RF circuit design considerations dictate that \( R_f \) should be chosen to be smaller than is reasonable for the bias network, an additional resistance can be used in series with \( R_f \) and this resistor would then be bypassed with a capacitor.

An approximate theoretical analysis of input/output impedance and power gain is presented in Appendix A. You are not responsible for the details of the analysis, but should understand which steps were taken to derive the two main design equations. Specifically, the Appendix develops the design equations by deriving the conjugate match condition, i.e. setting \( Z_{in}=Z_{out}=R=50 \). The first design equation, which relates power gain to \( R_e \) and transconductance is based on equation 3.15 in the Appendix.

\[
G \approx \frac{2R}{g_m R_e} \quad \text{(Design Eq. 1)}
\]

In the equation above, \( R = 50 \, \Omega \), is the assumed input and output resistance. The second equation, based on equation 3.12 in the Appendix, allows to choose \( R_f \) to achieve the conjugate match.

\[
R_f \approx \frac{2R^2}{g_m R_e} \quad \text{(Design Eq. 2)}
\]

In the equations above, \( r_n \) has been replaced by \( \beta/g_m \), which allows to cancel \( \beta \). Recall that \( g_m \approx 40 \, I_{CQ} \) at room temperature, and is determined by the bias.

**Nonlinear characterization of the broadband amplifier**

For the time being, the students are referred to the appropriate sections in Chapters 10 and 12 of the Course Notes. The background information for the lab is under development.
**Procedures**

You will be provided with a populated PCB containing a broadband amplifier. After replicating the design in an ADS simulation, you will plot its simulated S-parameters. Finally, using the physical amplifier circuit, you will measure gain compression, intermodulation distortion, and noise figure.

**ADS simulation of the linear regime of the broadband amplifier**

First, to familiarize yourself with the amplifier design and ensure the amplifier will meet the design specifications, you will create an ADS simulation of the provided amplifier. The amplifier will have the same basic topology as shown in the schematic below, but resistance values may differ somewhat. Replace resistor values in the schematic below with the actual values in your circuit. These values may be determined through visual inspection or use of the DMM.

Note that the amplifier has been designed to provide a bias of 6 V at the base, which results in R1 = R2. The $g_m$ value is set by the choice of R4, and will be approximately 510 ohms.
ADS simulation hints:

1. Start ADS and create a schematic
2. From the upper left drop down list choose 'Simulation-S_param' create two 'term' items (Row 3, Col 2), make sure the termination resistance is 50 ohms.
3. From 'Devices-BJT' create a generic BJT Model (Row 3, Col 2)
4. From 'Devices-BJT' create a generic BJT (Row 1, Col 2), make sure the BJT is using BJT Model create in 5, the default name of the model is 'BJTM1'
5. From 'Source-Time Domain' create a V_DC (Row1, Col1)
6. From 'Lumped-Components' create a mutually coupled inductor (Row 5, Col2), change the K factor to 1. Specify the inductors' names (Default are 'L1' and 'L2'), this tells the simulator which two inductors are coupled.
7. From 'Simulation-S_Param' create a S-parameter simulation. Change start frequency to 1Mhz and stop frequency to 200MHz with frequency step 1MHz.
8. Run the simulation. Make the plots. Add markers. Plots should be similar to the examples below:
Measuring Amplifier S-parameters with the N5230C VNA

Configure the network analyzer to sweep over the 1 – 200 MHz frequency range, 201 points. Next, reduce the input power—go to the [Channel][Power and Attenuators] menu and set Attenuation to 20 dB. (your menu might be slightly different). Perform an unguided 2-port calibration using the Kirkby SMA SOLT calibration standards.

Save the data in .s2p format. Go to the data display window that contains your simulated S-parameter plots. Open the data file tool and import the measured .s2p file as S_meas. Overlay plot each of the measured S-parameters on the appropriate graph.

Measuring Gain Compression with the N5230C VNA

Gain compression can be observed and characterized by setting up the VNA to operate at a fixed frequency while sweeping the input power over a defined range. The instrument will show a plot of insertion power gain in dB (20 log |S21|) verses input available power level in dBm. The gain will be relatively constant at very low input powers, and will decrease as the input power increases.

1. Select the “power sweep” mode: [Sweep][Sweep Type], select “Power Sweep”. Set desired start and stop power. Set CW freq to 50 MHz. Set start power to -25dBm, the stop power to 0 dBm.

2. Go to the [Channel][Power and Attenuators] menu and set Attenuation to 20 dB. (your menu might be slightly different)

3. The instrument will display gain vs. input power (actually, Pav). Use a marker to identify the input power level at which the gain has decreased by 1 dB from the small-signal value. This is the input power for 1 dB compression. Save a screenshot for your report.

Two-tone Measurement for Intermodulation Distortion

1. Connect the outputs of two signal generators to a signal combiner/splitter (labeled PSCQ-2-90). Ports 1 and 2 serve as inputs for this experiment.

2. Take the output of the combiner from the port marked ‘S’. This signal will be used to drive the amplifier.


4. Setup for the function generators: RF Output should be -20 dBm (as seen after the combiner on the MXA). Frequencies: Set one at 50.01 MHz and the other to 49.99 MHz.

5. Using the combiner to drive the amplifier, record the output power of the components given by the VSA at the frequencies: 49.97 MHz, 49.99 MHz, 50.01 MHz, and 50.03 MHz as the drive power from the signal generators is decreased in 1 dB steps. Take as many points as possible (at least ten). Make sure that you have several sets of points at drive levels where gain compression can be neglected.

6. (Optional, if you didn’t pre-calibrate) Remove the amplifier and feed the output of the combiner directly to the VSA to find Pin at each of the drive levels that you used in step 5.

7. Using your power measurements, find the $P_{i}^{(i)}$ and $P_{i}^{(o)}$ using linear interpolation and extrapolation.
Noise Figure Measurement with the Agilent N9020A

1. Set the measurement mode of the MXA to Noise Figure Analyzer.

2. In the FREQ menu, set the start frequency to 10 MHz, stop frequency to 100 MHz, and the number of points to 91. Then set the BW to be something less than 4 MHz. If the characteristics of the DUT change appreciably over 4 MHz, then choose a smaller bandwidth.

3. Now we calibrate. First plug in a calibration thru between the noise diode and the VSA. Then press Meas Setup -> Calibrate Now to calibrate. This might take a while.

4. After calibration, the display should show 0 dB for gain and a noise figure across the frequency span. If it does not, check all connections and recalibrate, then ask your TA for help.

5. To test the calibration further, place an attenuator between the noise diode and the VSA to measure its noise figure. We remember that the noise figure of an attenuator in dB should be equal to the attenuation it supplies in dB.

6. Now measure the noise figure of the DUT. Gain and NF can be read directly at the frequencies of interest by using markers. DUT will show up as “spikes” in the measured NF. Take your readings at frequencies well away from any such spikes. Save a screenshot of gain and noise figure for your report.
Lab 8 Grading Checklist

- Brief introduction of the lab (2 pts)
- List the design specifications of the amplifier (2 pts)
  - Include and explain the two main design equations (gain and conjugate match) (2 pts)
- Include the ADS amplifier schematic diagram of the measured amplifier (featuring your board's component values) (2 pts)
  - Include the overlaid measured and simulated S-parameter graphs (4 pts)
  - Why did we adjust the VNA power settings prior to S-parameter measurement? (1 pt)
- Include the gain compression plot. (2 pts)
  - State the 1dB compression point input power. (2 pts)
- Describe the measurement setup for the two-tone third-order intercept measurement (2 pts)
  - Include the table and your calculation of the intercept. Show the resulting plot. (5 pts)
- Define Noise Figure. Explain its measurement. (2 pts)
  - Include the noise figure (and gain) plot for the amplifier. Comment. (3 pts)
- Each partner contributes a reflection paragraph (2 pts)
  - Information in the report is comprehensive and organized (2 pts)

- Total Points: 33
Appendix A. Analysis details of input/output impedance and power gain

For approximate analysis of this circuit using pencil and paper, we can use a simplified (low-frequency) hybrid-π model for the transistor and assume that the transformer is an ideal 1:1 transformer, i.e. that the two windings are perfectly coupled. An ideal transformer can be described by two equations. Denoting the voltage across each of the windings by $V_1$ and $V_2$, and the current directed into the dot associated with each winding by $I_1$ and $I_2$, then an ideal 1:1 transformer satisfies:

\[ V_1 = V_2 \]  \hspace{1cm} (3.1)
\[ I_1 = -I_2 \]  \hspace{1cm} (3.2)

The small signal equivalent circuit for the amplifier is shown in Figure 3.2. The ideal transformer relationships have been incorporated into the figure by explicitly showing that the currents flowing through each of the windings of the transformer are equal to $I$ and the voltage across each winding is equal to $V_o$.

![Small signal model for the amplifier](image)

The input impedance of the amplifier (i.e., the impedance seen by the source with Thevenin impedance $R_s$) can be shown to be:

\[ Z_{in} = \frac{(R_L + R_f)(R_e + r_\pi + g_m R_e r_\pi)}{R_e + r_\pi + R_L + R_f + g_m r_\pi (R_e + 2R_L)} \]  \hspace{1cm} (3.3)

The output impedance of the amplifier is:

\[ Z_{out} = \frac{(R_s + R_f)(R_e + r_\pi + g_m R_e r_\pi) + R_s R_f}{R_s + R_e + r_\pi + g_m r_\pi (R_e + 2R_s)} \]  \hspace{1cm} (3.4)

The voltage gain is (note that $V_i$ is the voltage across the amplifier input terminal, i.e. the voltage between the base of the transistor and ground):

\[ A_v = \frac{V_o}{V_i} = -\frac{2g_m}{R_f} \left( \frac{R_L R_f}{R_f + R_f} + \frac{1}{R_e (g_m + \frac{1}{r_\pi})} + \frac{1}{R_L + R_f} \right) \]  \hspace{1cm} (3.5)

We can now use equations 3.3 through 3.5 to derive values for the independent parameters $g_m$, $R_e$, $R_f$, that will yield useful impedance and gain properties. One of our goals is to design an amplifier that will be simultaneously matched to 50Ω at both ports. To develop a design equation that will enforce the simultaneous conjugate match requirement we specify:
Later, we will set $R = 50\Omega$. Using constraints 3.6 and 3.7 in equations 3.3 and 3.4 we obtain two equations:

$$Z_{in}|_{R_L=R} = R$$  
(3.6)

$$Z_{out}|_{R_c=R} = R$$  
(3.7)

\[
R = \frac{(R + R_f)(R_e + r_\pi + g_m R_e r_\pi)}{R_e + r_\pi + R + R_f + g_m r_\pi (R_e + 2R)} \quad (3.8)
\]

\[
R = \frac{(R + R_f)(R_e + r_\pi + g_m + R_e r_\pi) + RR_f}{r + R_e + r_\pi + g_m r_\pi} \quad (3.9)
\]

Multiply both sides of equation 3.8 by the denominator of the right-hand side to obtain:

\[
RR_e + R r_\pi + R^2 + RR_f + g_m r_\pi R(R_e + 2R) = RR_e + R r_\pi + g_m RR_e r_\pi + R_f R_e + R_f r_\pi + g_m R_e R_f r_\pi
\]

Combine terms to obtain:

\[
R^2 (1 + 2g_m r_\pi) - R_f (R_e + r_\pi + g_m r_\pi R_e - R) = 0 \quad (3.10)
\]

Carrying out the same procedure on equation 3.9 yields:

\[
R^2 (1 + 2g_m r_\pi) - R_f (R_e + r_\pi + g_m r_\pi R_e + R) = 0 \quad (3.11)
\]

Equations 3.10 and 3.11 differ in the second term, and they cannot be satisfied simultaneously unless $R \ll R_e + r_\pi + g_m r_\pi R_e$, in which case the equations become essentially identical. In practical applications, the approximation $\beta = g_m r_\pi \gg 1$ will hold, and if we choose values of $R_e, R_f$, and $r_\pi$, such that $R \ll R_e + r_\pi + g_m r_\pi R_e$ equations 3.10 and 3.11 yield, approximately:

\[
R_f \simeq 2\beta R_e \frac{2R^2}{r_\pi + \beta R_e} \quad (3.12)
\]

We can view equation 3.12 as one of the design equations for the amplifier, as it specifies what value of feedback resistor must be used once the other parameters have been determined.

Next, consider the voltage gain with $R_L = R$, under the assumption that $\beta \gg 1$:

\[
A_v \simeq \frac{-2\beta R R_f}{(R + R_f)(r_\pi + \beta R_e)} + \frac{R}{R + R_f} \quad (3.13)
\]

The second term will be less than 1. We will be interested in the parameter regime where the amplifier has voltage gain significantly greater than 1 so this term can be neglected. Since we have specified a simultaneous conjugate match with equal source and load impedances, the power gain is simply the square of the voltage gain. (If we had specified a simultaneous conjugate match with different source and load impedances, this wouldn’t be true!) Also, recall that under conjugate matched conditions, the operating, transducer, and available power gains are equal. The power gain of the amplifier is:

\[
G = \left[ \frac{-2\beta R R_f}{(R + R_f)(r_\pi + \beta R_e)} \right]^2 \quad (3.14)
\]

So far, the approximations that we have employed are $\beta \gg 1$ and $R \ll R_e + r_\pi + g_m r_\pi R_e$. If we make one more approximation by constraining the value of $R_f$ to be much larger than $R = 50\Omega$, ($R_f \gg R$), then equation 3.14 simplifies to
This extra constraint is useful because it makes the gain independent of the feedback resistance \( R_f \). We can use equation 3.15 to choose \( R_e \) to set the gain of the amplifier once \( R \), \( \beta \), and \( r_\pi \) are determined. Then the value required for \( R_f \) can be determined using equation 3.12 in order to satisfy conjugate match criterion. In practice, the value of \( \beta \) will be determined by the transistor that is chosen for the amplifier, and then the quiescent collector current will determine \( r_\pi \). We are free to choose the value of collector current (and therefore \( r_\pi \)) to satisfy some other criterion such as minimum noise figure, or we may choose to use the collector current that optimizes the transistor’s gain-bandwidth product in an attempt to achieve highest gain.

Now consider some typical numbers. Suppose that \( R = 50 \, \Omega \), \( \beta = 100 \), and \( I_{CQ} = 10 \, mA \) so that \( r_\pi \cong 250 \, \Omega \). To satisfy the approximation \( R \gg R_f \), it is reasonable to require that \( R_f \) be at least 10 times as large as \( R \), i.e. \( R_f \geq 500 \, \Omega \). Likewise, to satisfy the approximation \( R \ll R_e + r_\pi + g_m r_\pi R_e \) we require \( 500 \, \Omega \leq R_e + r_\pi + \beta R_e \), or \( R_e \geq 2.4 \, \Omega \). Then the power gain of the matched amplifier can be written (in dB) as:

\[
G = 80 - 20 \log(260 + 100R_e)
\]  

The power gain as a function of the series feedback resistance \( R_e \) is summarized in Table 3.1. For each value of \( R_e \), the value of \( R_f \) that would give a simultaneous match to 50 \( \Omega \) is also given.

<table>
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<th>Re (( \Omega ))</th>
<th>G (dB)</th>
<th>Rf (( \Omega ))</th>
</tr>
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<tbody>
<tr>
<td>0</td>
<td>31.7</td>
<td>1923</td>
</tr>
<tr>
<td>1</td>
<td>28.9</td>
<td>1389</td>
</tr>
<tr>
<td>2</td>
<td>26.7</td>
<td>1087</td>
</tr>
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<td>3</td>
<td>25.0</td>
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<td>21.3</td>
<td>582</td>
</tr>
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<td>20.4</td>
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<td>431</td>
</tr>
<tr>
<td>10</td>
<td>18.0</td>
<td>397</td>
</tr>
</tbody>
</table>

Table 3.1: Gain and shunt feedback resistance as a function of series feedback resistance.

Notice that smaller values of \( R_e \) (less negative feedback) result in larger power gain. In order to satisfy the approximations that were made in the analysis it is necessary to have \( R_e \geq 2.4 \, \Omega \) and \( R_f \geq 500 \, \Omega \). From Table 3.1 this implies that \( 2.4 \, \Omega \leq R_e \leq 7.5 \, \Omega \), since choosing \( R_e \) to be larger than about 7.5 \( \Omega \) would require \( R_f \) to be smaller than 500 \( \Omega \).