Phasor Measurement Unit

Project 7
ECE 445 Spring 2013
Design Review

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1 INTRODUCTION

1.1 Overview

This project was deemed appropriate due to current status of Phasor Measurement Units (PMU); existing PMUs have proven to be very expensive and bulky. One of the reasons for the high cost and large size is due to their ability to take three phase measurements. Another factor comes from the fact that existing PMUs are made to be compatible with relays to be able to automatically correct for errors within the grid.

This project, however, focuses on making a unit that can be much cheaper and smaller, with functionality optimization; instead of three-phase measurements, by implementing only one phase and voltage measurement, the important functionality of the PMU is kept while keeping the cost low.

With lower price and more compact size, the distribution of PMU units across the U.S. power grid can greatly increase. Ultimately, relevant industries will be able to monitor the status of the grid, potentially increasing the stability of the grid.

Most useful data collected by the PMU will be what is called a synchrophasor data. A synchrophasor is defined as the magnitude and angle of a sinusoidal function as referenced to an absolute point in time. The difference in wave magnitudes at different points down the transmission and distribution system indicates losses. Furthermore, the phase difference between voltage waves with respect to an absolute point in time indicates power transfer. There is a breakdown value which the phase difference must not reach in order to keep the system stable. Also, the difference in the frequencies between voltage waves indicates instability.

1.2 Objective

- Successfully acquire voltage and calculate frequency and synchrophasor data with GPS timestamp
- Deploy PMUs across the country
- Cost to be less than $14,000, which is the cost of existing PMUs
- Size to be no bigger than 300mm x 100mm x 100mm

1.3 Functions

- Sample voltage and calculate phase, frequency, and RMS voltage magnitude with GPS timestamp precise to a second
- Output/save data to a web server
- LED to show status of the PMU

1.4 Benefits

- Real-time monitoring the state of the U.S. power grid will enable avoidance of blackouts
- Ability to be deployed world-wide due to cost and size benefits.
- Will assist with higher level PMU research due to its “open-box” nature

1.5 Features

- Compact size
- Cheaper than current PMUs
- User friendly
- Data can be observed anywhere with computer access

2 DESIGN

2.1 Block Diagram

Figure 1 shows the block diagram of the PMU.

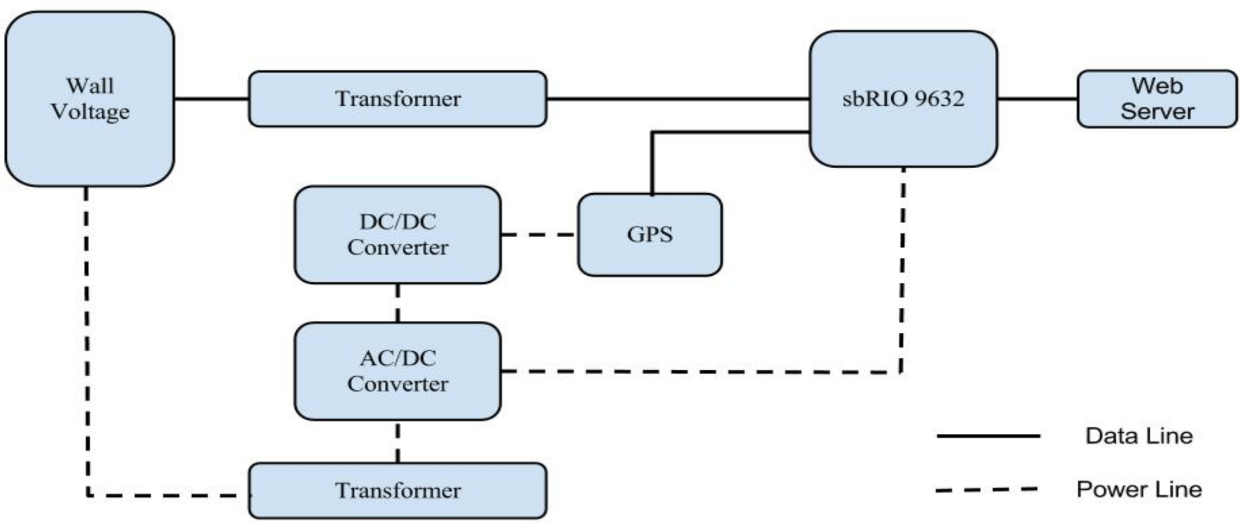

Figure 1. Block Diagram

Figure 2 and Figure 3 shows the dataflow and power flow, respectively.

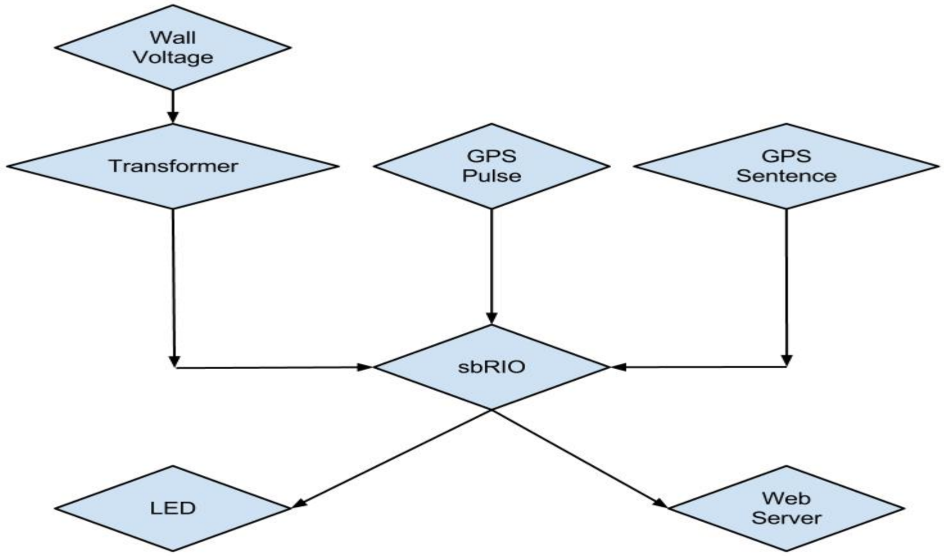

Figure 2. Dataflow

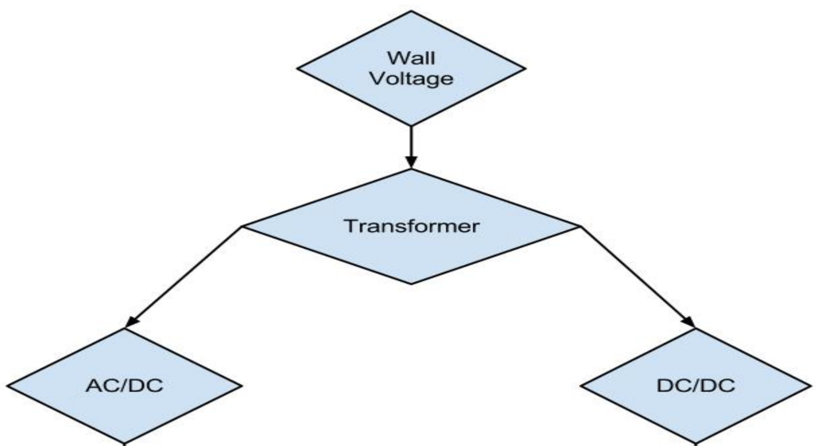

Figure 3. Power flow

2.2 Block Descriptions

2.2.1 Wall Outlet

Any wall outlet is a viable source of data sampling. It will connect to a transformer via modified NEMA 5-15 (AC power plugs).

2.2.2 Transformer

A transformer will be used to step down the wall voltage to a voltage that can be sampled from the Single Board RIO. Desired transformer will step down $120V_{RMS}$ to $5V_{RMS}$.

Another transformer will be used for the purpose of stepping down the wall voltage from $120V_{RMS}$ to $22V_{RMS}$ to act as an input for the AC/DC converter.

2.2.3 GPS

The GPS will output National Maritime Electronics Association (NMEA) GPRMC data sentence, along with a 5V pulse each second. Both data will be inputs to the Single Board RIO.

2.2.4 Single Board RIO (sbRIO)

Single Board RIO will take GPS data, GPS pulse, and stepped down wall voltage to calculate RMS value, frequency, and phase with precise timestamp. The data will be output as a text file.

2.2.5 LED

An LED will show the status of the PMU. If data is correctly being output from the sbRIO, LED will be lit.

2.2.6 Web Server

Data generated from the sbRIO will be uploaded to a web server. This will allow for the data to be observed anywhere.

2.2.7 AC/DC/DC Converter

This block will convert $22V_{RMS}$ from a transformer to a $24V_{DC}$ and $5V_{DC}$ to power the sbRIO and the GPS.

2.3 AC/DC, DC/DC Converter, Preliminary Simulation Results

2.3.1 Schematics

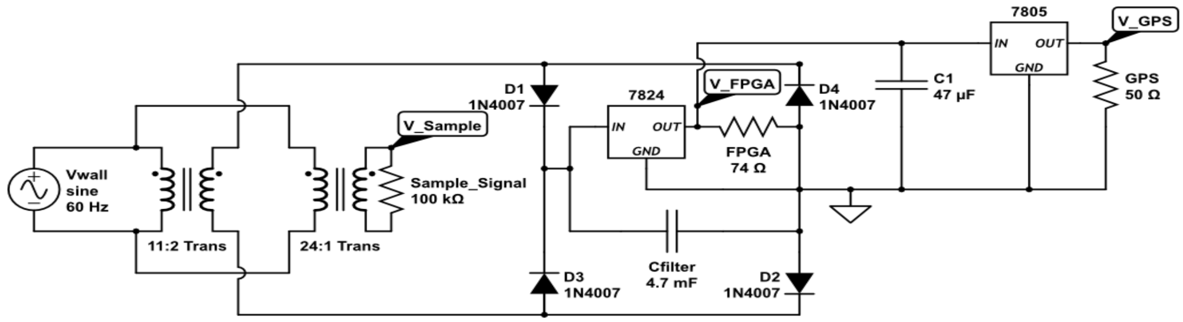

Figure 4. Power Supply

2.3.2 Calculations

There are three parts to the power supply. The V_Sample, V_FPGA, and V_GPS. Each component was calculated out with certain requirements.

First, the V_Sample which is used for sampling must be between -10 to 10 V in amplitude from the requirements. Since the Vwall is $120V_{RMS}$, a 24:1 transformer is used to step the voltage down to $5V_{RMS}$. Since the analog input of the converter is high impedance, in the schematic it is replaced by a 100kΩ resistor.

V_FPGA is the constraint for the main part of the design. Initially, the voltage at the FPGA was chosen as 24V. Since at 60Hz, capacitive filtering would require a very large capacitor for a true rippleless voltage, a 4.7mF capacitor was decided to be used alongside with the UA 7824 voltage regulator. By doing this, the V_ripple is found to be fairly large, as shown in (1), but small enough for this application. The linear regulator input can be found by (2) with the constraint of (3) and (4).

$$V_{ripple} = \frac{I_{load}}{2fC} = \frac{P}{2VfC} = \frac{7.75}{2*24*4700*10^{-6}} = .59V \tag{1}$$

$$V_{regin} = V_{secondary} - 1.2 \pm \frac{V_{ripple}}{2} \tag{2}$$

$$27V < V_{regin} < 37V \tag{3}$$

$$V_{regin} = V_{cap} < 35V \tag{4}$$

Using these properties, the V_secondary is solved for as a range in (5).

$$30.9V < V_{secondary} < 31.5V \tag{5}$$

From this calculated result, V_secondary is chosen as 31V to solve for the transformer turns ratio as 11:2.

From a stable 24V at the FPGA, a 5V output was necessary to power the GPS. To create this output, a linear regulator was used again. Using a 47uF capacitor to stabilize the input voltage, UA7805 was used to create the 5V supply.

2.3.3 Simulation

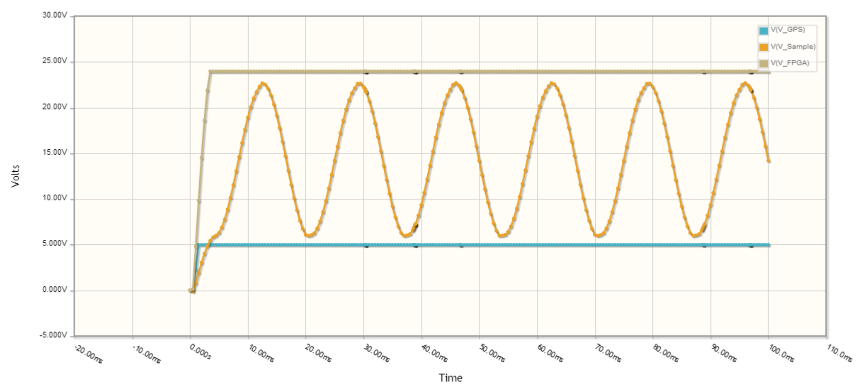

Figure 5. Simulation results

Figure 5 shows the simulation results. The results show that V_FPGA and V_GPS is stable at 24V and 5V, and V_Sample is an undistorted sine wave. This would power the board, gps, and allow sampling to be made.

2.4 GPS Simulation

The Garmin 18x LVC provides timing information that “enables” data synchronization for the project. A sample of the GPS 1 pulse per second signal is shown in the oscilloscope screen shot at Figure 6. The signal high is 5 V and low is 0 V. The distinct pulse leading edge marks the start of each second accurate up to 1µs. A sample of the National Maritime Electronics Association (NMEA) standard sentence “GPRMC” is shown in Figure 7, which provides the date and time stamp. The two together forms the time reference for the PMU.

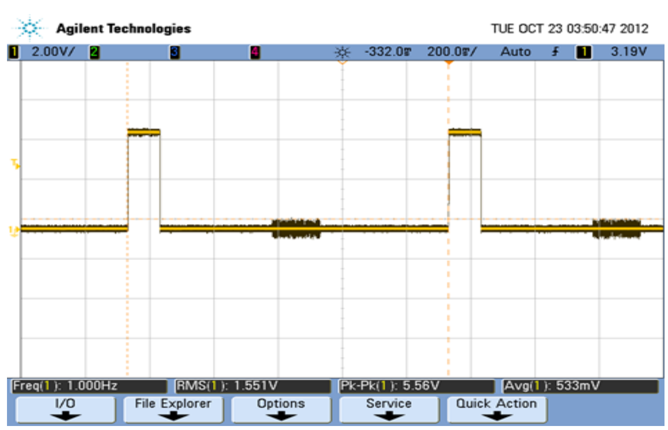

Figure 6. GPS Pulse Signal

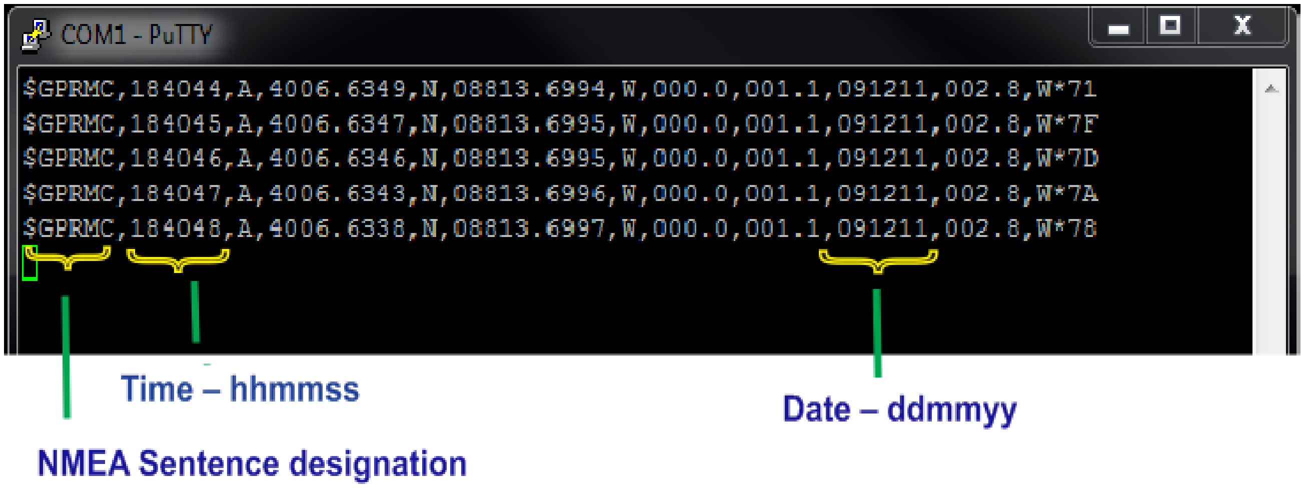

Figure 7. GPS Data Sentence for Date and Time

2.5 NI labVIEW Programming Simulation

2.5.1 Control VI

Figure 8 shows the code written for the sbRIO. This VI controls 2 subVIs: FPGA VI and GPS VI. Control VI controls the overall operation for the PMU. It takes data read by FPGA subVI along with GPS subVI to calculate frequency, RMS voltage, and phase of the waveform and outputs correct data with precise timestamp. Timestamp data collected every second is divided into 6 parts and are assigned to corresponding group of voltage measurements and calculations. In this simulation, calculated data is output as waveform each time the FIFO fills up, as shown in Figure 11. LED and web server control will be added to this main VI.

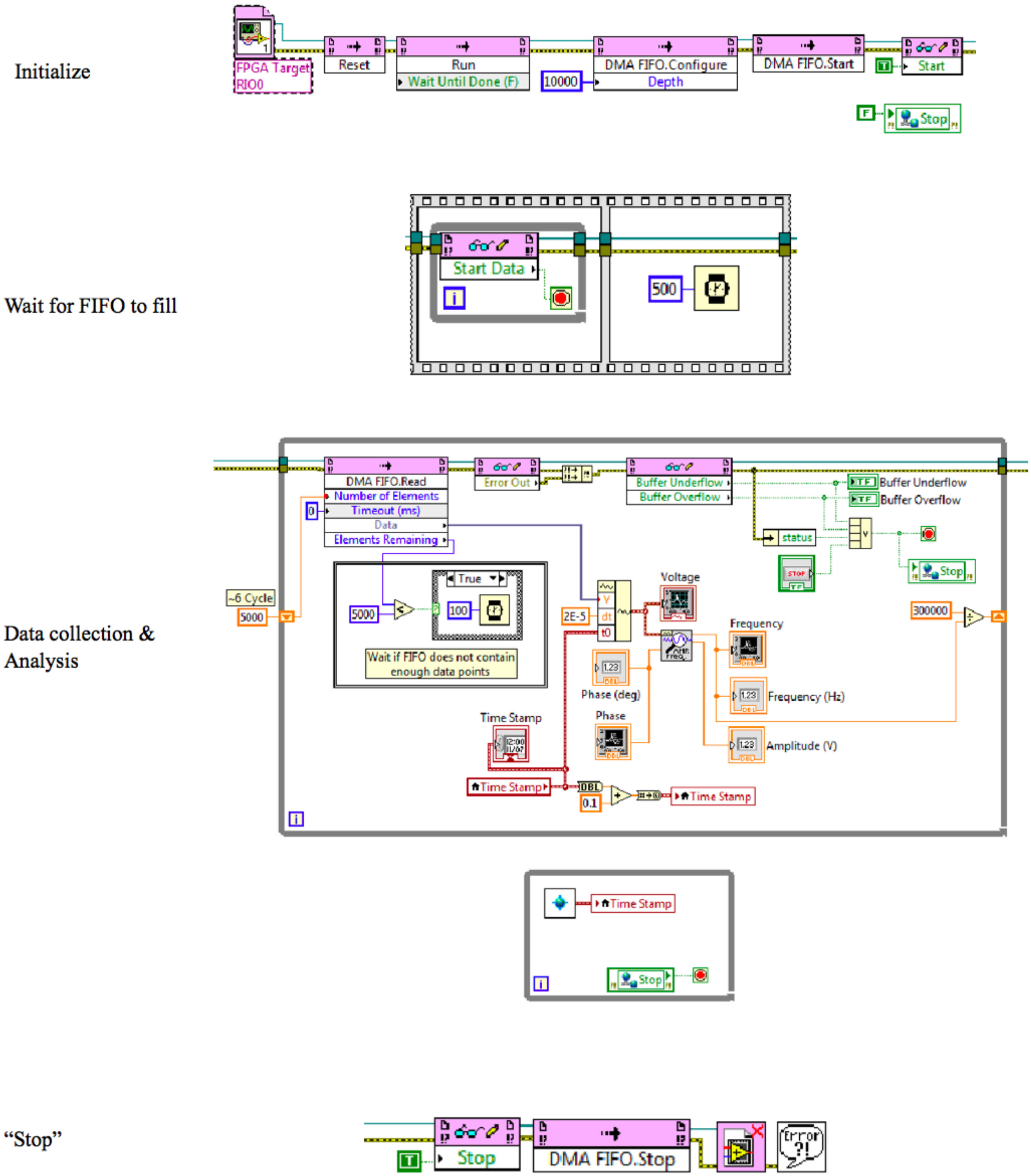

Figure 8. Control VI

2.5.2 FPGA subVI

FPGA subVI is operated by control VI to collect data at the start of pulse given by the GPS. Collected data points are put into a FIFO for control VI to utilize.

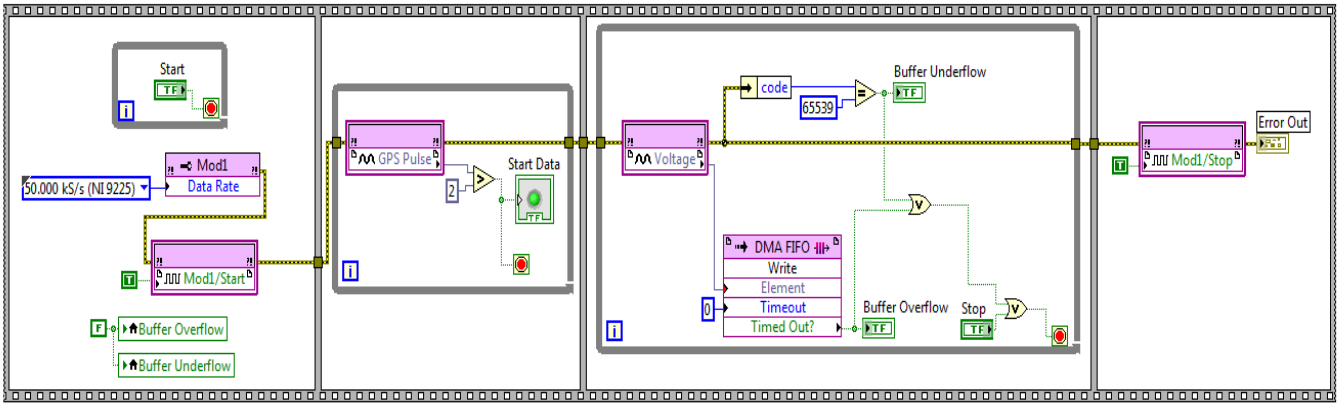

Figure 9. FPGA subVI

2.5.3 GPS subVI

This subVI collects GPS sentence in a string form and outputs year, month, date, and time exact to a second. The output is used by the control VI to stamp time to acquired voltage data.

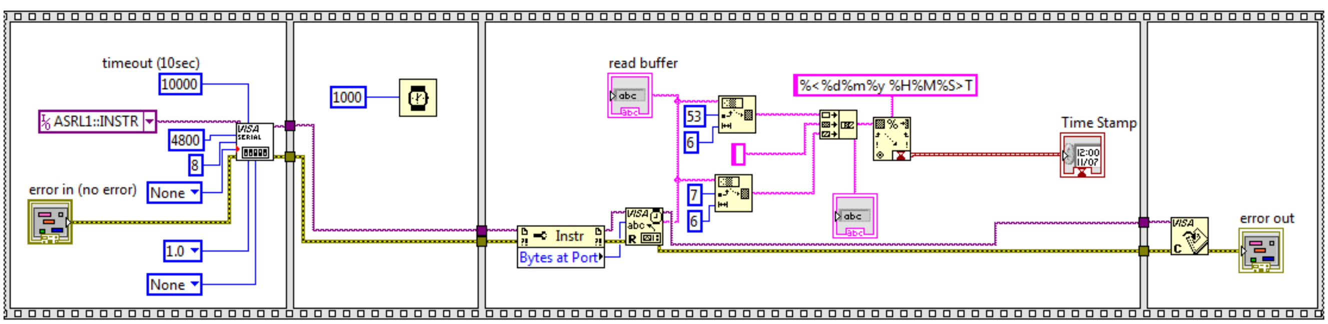

Figure 10. GPS subVI

2.5.4 Front Panel

Figure 11 shows the front panel of the main control VI. As seen in the figure, correct representation of the wall voltage is confirmed with frequency and phase. With a finalized product, the data will be output as a text file to a web server.

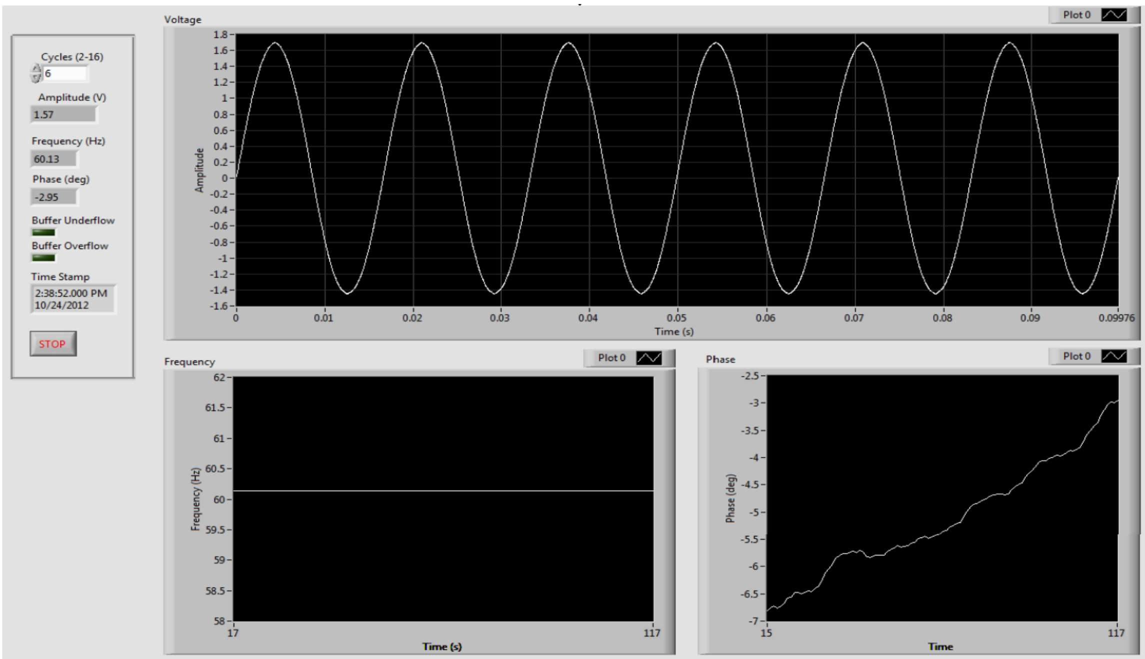

Figure 11. Front Panel

2.5.5 Web Server

The web server data storage of the PMU will be implemented using the sbRIO. As long as the sbRIO is connected to the internet via Ethernet cable, sbRIO can be programmed using LabVIEW FPGA code to store data on the server.

3 Requirements and Verification

3.1 Testing Procedures

Requirements	**Verification**
Wall Outlet 1. Sinusoidal voltage wave with 120V RMS ±6.667% provided by the utility company.	1. Tested using a voltage probe and an oscilloscope.

Transformer	
1. $120V_{RMS}$ ±6.667% on the primary, will give $5V_{RMS}$ ±6.667% on the secondary. This gives a stepped down voltage amplitude range of 6.60~7.54 V, which is within the 10 V maximum analog input of the sbRIO.	1. An oscilloscope will be used to ensure the stepped-down voltage is within the analog input range over the entire wall voltage allowed range: a. Connect 112 VRMS to the primary of the transformer. The amplitude on the secondary must not exceed 10V. b. Connect 128 VRMS to the primary of the transformer. The amplitude of the secondary must not exceed 10V
2. 2mV conversion error when stepping down wall voltage. This translates into a wall voltage error of 48mV giving an assumed range between 119.952~120.048 V RMS when the wall voltage is 120.000 V_{RMS}. Greater number of turns give a smaller conversion error.	2. The primary and secondary transformer RMS voltages will be measured with a multimeter for different input values: a. Put 112 VRMS on the primary of the transformer. Measure the RMS value on the secondary. Calculate the conversion factor by dividing the primary RMS to the secondary RMS value. b. Repeat for 1 VRMS increments until 128 VRMS c. If the range in the conversion factor is less than 0.0192 when the primary is varied from 112 VRMS to 128 VRMS, the transformer works as required and the next step can be ignored. d. If the error is bigger, increase the number of turns on each side of the transformer while keeping their ratio the same

	until the conversion factor error is within range.
<u>GPS</u> 1. It must accurately generate a square wave with a rising edge at the beginning of each second. The pulse has 5 +- 0.6 V DC.. 2. The rising edge represents the beginning of each second and is accurate to within 1 μs according to its specifications. The accuracy takes into account the effects of rise time.	1. The GPS signal will be verified using an oscilloscope 2. The accuracy will not be tested since the specifications are assumed to be true.
<u>Single Board RIO</u> 1. The FPGA inside the sbRIO multiplies the analog input by the transformer step down conversion factor. 2. Write code to calculate the frequency of the voltage wave. 3. The voltage wave will then be sampled and each point will be time-stamped using the GPS signal. 4. It transmits data to a web server	1. a. Programmatically multiply the analog signal by the transformer conversion factor b. Plot the resulting waveform in LabVIEW c. Calculate its RMS value d. It must be within 48 mV of the wall voltage. 2. The resulting frequency must be the same as the frequency of the wave displayed on the oscilloscope. 3. a. Display time-stamped data b. Compare timestamp with official time c. Check the accuracy to be within 1 us. 4. a. Write code to transmit data to

5. Signal to turn on the LED will be sent when there is no error in data being stored on the server	a server b. Test the code by giving it data to store online c. Check the web server to make sure data was successfully stored 5. a. Write code to turn LED off when error is present in the web server data storage application b. Introduce an error in the data storage code, such as removing the GPS signal while code is running c. Look at the LED d. Check that it turned off e. Remove the error from the code by reintroducing the GPS signal f. Watch the LED g. Check that is turned on and data is being stored on the server
<u>Web Server</u> 1. Continuously received data from the sbRIO, as long as sbRIO is powered on and no error in the code appear	1. a. Turn everything on b. Check the webserver to see if data is stored on the website c. Introduce an error by removing the GPS signal d. Check the webserver to make sure no data is stored with the GPS signal missing.
<u>LED</u> 1. LED is on when data is transmitted to the server; otherwise, LED is off.	1. a. Transmit data to the web

	server b. LED must be on c. Introduce an error in the data storage code d. Try to transmit data to the web server e. LED must turn OFF
<u>AC/DC/DC</u> 1. The AC/DC/DC converter uses wall voltage to power the sbRIO and GPS unit, therefore it must be designed to operate over the entire wall voltage range.	1. a. Power the converter using 112 VRMS b. Measure the converter DC voltage using an oscilloscope c. It must be 25 VDC +- 20 mV d. Increment the voltage into the converter by 1VRMS. e. Measure the converter DC voltage f. It must be 25 VDC +- 20 mV g. Repeat steps d. and e. until 128 VRMS is at the input of the converter h. A steady converter output over the entire input voltage range will verify its correct operation
2. sbRIO input voltage from converter must be 25V_{DC} with a ripple less than 20 mV and current of 0.31A with a ripple of 25 mA	2. a. Add a 70 ohm load at the output of the AC/DC converter. This will draw 0.36 A, which is over the required limit of 0.31 A. b. Measure the voltage and its ripple using an oscilloscope c. Check if voltage is within required limits d. Measure current into the load using an oscilloscope

	e. Check current to make sure it is 0.36 A f. Let it running for half an hour g. Voltage and current values and ripples must not change value over time h. Make sure components do not melt or become hot while operating for a long period of time
3. GPS must be powered by 5V DC with an allowed ripple between 4.0-5.5 V DV and 90 +- 2 mA	3. a. Add a 50 ohm load at the output of the DC/DC converter. b. This will draw 0.1 A c. Measure voltage and current at the load using an oscilloscope d. Check that these are the desired values with the corresponding desired ripples e. Leave it powered for half an hour f. Check that current and voltage values and ripple do not change over time g. DC/DC converter components must not get hot or melt during prolonged operation
4. The current provided by the converter is 0.4 A +- 25 mA. Since there will be a transformer in our converter with 0.4 A representing the current on the low side, the high side will have less current; therefore 0.4 A represents the maximum current in our converter.	4. This step verified implicitly by step 3 because the DC/DC converter current is supplied through the AC/DC converter

3.2 Tolerance Analysis

The National Electrical Code (NEC) says the standard for the wall voltage is 120V ±5%. This gives a range of 114 V to 126 V. However, in order to accommodate outliers, we will design our power converter to operate from a voltage source range of 112 V to 128 V. The sbRIO-9632 user guide dictates that the power supply ripple must be less than 20 mV.

Since there is a step down of voltage from the wall outlet to the analog input of the FPGA, an error factor naturally exist. The accuracy of the voltage measurement is essential. However, since the FPGA is accurate up to 6220 µV at the highest voltage range (-10V to 10V), this would mean that the FPGA can theoretically be accurate up to 0.06%. To bring the error factor to low as possible, an Agilent Technologies oscilloscope will be used to make sure that this voltage is accurate up to 0.1%.

4 Cost and Schedule

4.1 Cost

4.1.1 Labor

Name	Rate	Hours	Total	Total x 2.5
Andy Yoon	$40/hr	100	$4,000	$10,000
Bogdan Pinte	$40/hr	100	$4,00	$10,000
Kenta Kirihara	$40/hr	100	$4,000	$10,000

Total: $30,000

4.1.2 Parts

Description	Manufacturer	Vendor	Cost/Unit	#	Total Cost
Single Board RIO-9632	National Instruments	National Instruments	$940	1	$0 (Donated)
Linear Regulator UA7824	Texas Instruments	Digikey	$0.91	1	$0.91
Linear Regulator UA7805	Texas Instruments	Digikey	$0.99	1	$0 (University)
Capacitor UUD1V470MCL1GS	Nichicon	Digikey	$0.82	1	$0.82
Capacitor F931V475KCC	Nichicon	Digikey	$1.04	1	$0 (University)
Diode 1N4007	Vishay S.D.D.	Digikey	$0.43	4	$0 (University)
266M6-ND Transformer (For data)	Hammond Manufacturing	Digikey	$32.08	1	$32.08

PC-20-500 Transformer Core (for converters)	Signal Transformer	Digikey	$11.25	1	$11.25
11-00038 Cable (NEMA 5-15)	Tensility International Corp.	Digikey	$2.60	1	$2.60
GPS 18x LVC	Garmin	gpscity	$60.00	1	$0 (donated)

4.1.2 Total Project Cost

Total Labor Cost	**Total Parts Cost**	**Total Project Cost**
$30,000	$47.66	$30,047.66

*Total project cost is to be $ 31,051.41 (counting donated and existing parts)

4.2 Schedule

Week	Task Description	Leading Member
2/11	Finish converter calculation	Kenta
2/18	Simulate converter	Bogdan
	Acquire converter parts	Kenta
2/25	**Design Review**	
	sbRIO programming for data acquisition	Andy
	Build/test converter	Kenta
	Acquire/test transformers	Bogdan
3/4	sbRIO programming for signal processing	Andy
	Design PCB, send request	Kenta
3/11	**Individual progress report due**	
	sbRIO programming for LED/web server	Bogdan
	Solder pieces on acquired PCB	Andy
3/18	**Spring Break**	
	Test the sbRIO with PCB assembled	Kenta
3/25	**Mock up demos**	
	Assemble PMU	Bogdan
	Test and verify functionality	Andy
4/1	**Mock-up presentations**	
	Debug if any problems are seen	Kenta
4/8	**Last day to request PCB**	
	Prepare presentation	Bogdan
4/15	**Demo/Presentation sign-up**	
	Prepare demo	Kenta
4/22	**Demos**	
	Write final paper	Andy
4/29	**Presentations, final paper due**	

5 Ethical Issues

Our team agrees to adhere to the IEEE Code of Ethics included in Appendix [A]. Furthermore, the following portions of the IEEE Code of Ethics are directly pertinent to our project:

1. "to be honest and realistic in stating claims or estimates based on available data;"
   Our PMU must not operate outside of the claimed errors. Its data must be as reliable as we claim it to be.

2. "to improve the understanding of technology; its appropriate application, and potential consequences;"
   One main reason to build the PMU was to aid in academic research by improving the understanding of their operation.

6 Safety Considerations

Since the project deals with high voltage, several safety measures are deemed important.

- Make sure the converter circuit is wired correctly before turning on power
- Do not make circuit changes when power is on
- Do not wear loose-fitting clothing
- Be cautious when handling equipments after it has been operating, as they may be hot
- Make sure parts (especially capacitors) are wired correctly with correct polarity
- Do not test with wet hands

7 Reference

[1] "IEEE Code of Ethics." IEEE. Web. 25 Feb. 2013. <http://www.ieee.org/about/corporate/governance/p7-8.html>.

[2] "User Guide." *National Instruments*. Web. 25 Feb. 2013. <http://www.ni.com/pdf/manuals/375052c.pdf>.

[3] Fairchild Semiconductor, "General Purpose Rectifiers," 1N4001 datasheet, May 2009

[4] Sparkfun, "Positive-Voltage Regulators," LM7805 datasheet, May 1976 [Revised May 2003]

[5] Reinhard, Karl. "Final Project Report: Phasor Measurement Unit," Dec 9, 2011

7 Appendix

[A] Section 7.8 IEEE Code of Ethics

We, the members of the IEEE, in recognition of the importance of our technologies in affecting the quality of life throughout the world, and in accepting a personal obligation to our profession, its members and the communities we serve, do hereby commit ourselves to the highest ethical and professional conduct and agree:

1. to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;
2. to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;
3. to be honest and realistic in stating claims or estimates based on available data;
4. to reject bribery in all its forms;
5. to improve the understanding of technology; its appropriate application, and potential consequences;
6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;
7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;
8. to treat fairly all persons regardless of such factors as race, religion, gender, disability, age, or national origin;
9. to avoid injuring others, their property, reputation, or employment by false or malicious action;
10. to assist colleagues and co-workers in their professional development and to support them in following this code of ethics.

Changes to the IEEE Code of Ethics will be made only after the following conditions are met:

- Proposed changes shall have been published in THE INSTITUTE at least three (3) months in advance of final consideration by the Board of Directors, with a request for comment, and
- All IEEE Major Boards shall have the opportunity to discuss proposed changes prior to final action by the Board of Directors, and
- An affirmative vote of two-thirds of the votes of the members of the Board of Directors present at the time of the vote, provided a quorum is present, shall be required for changes to be made.