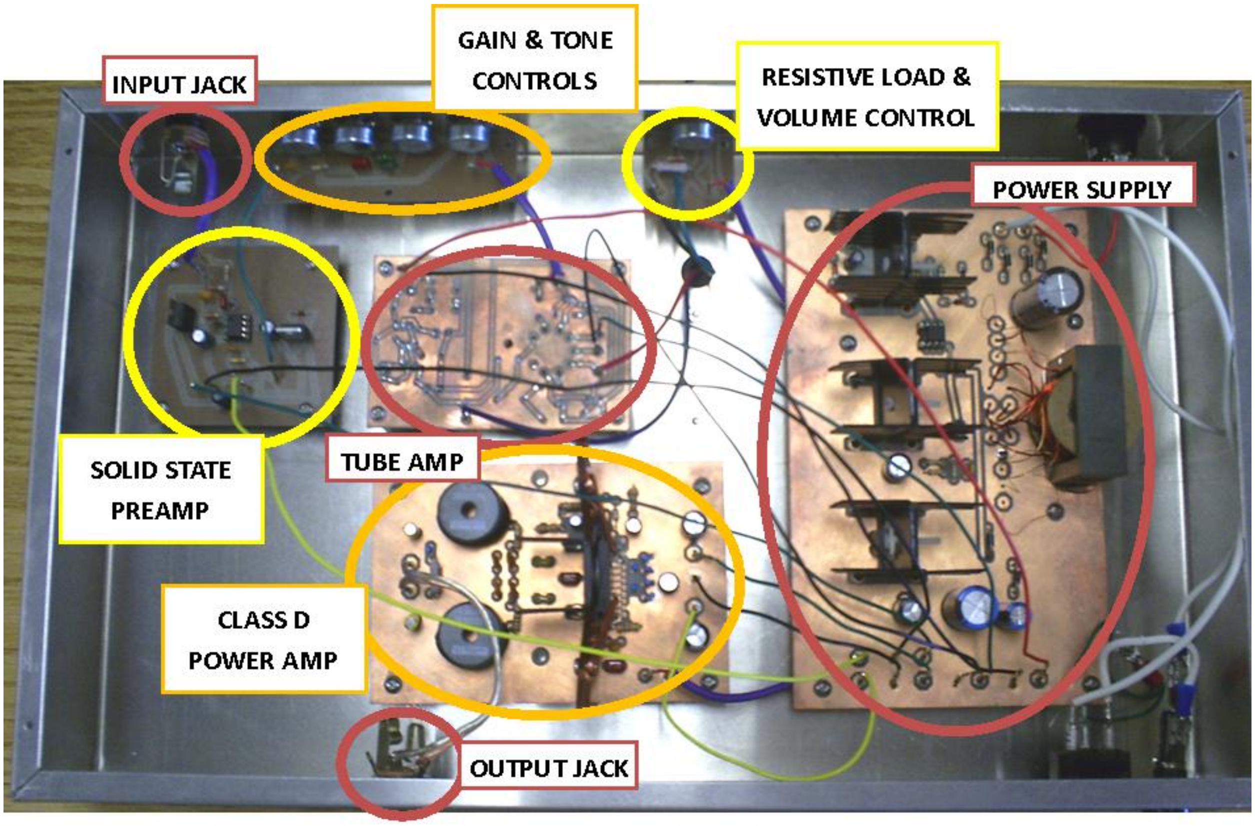
Appendix 2

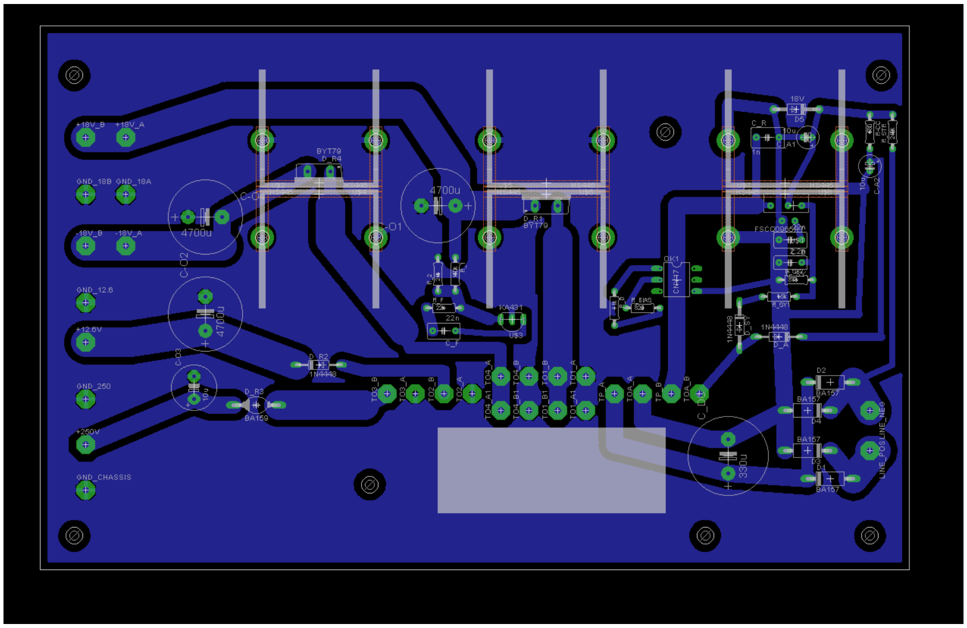
Final Construction of Amplifier Head



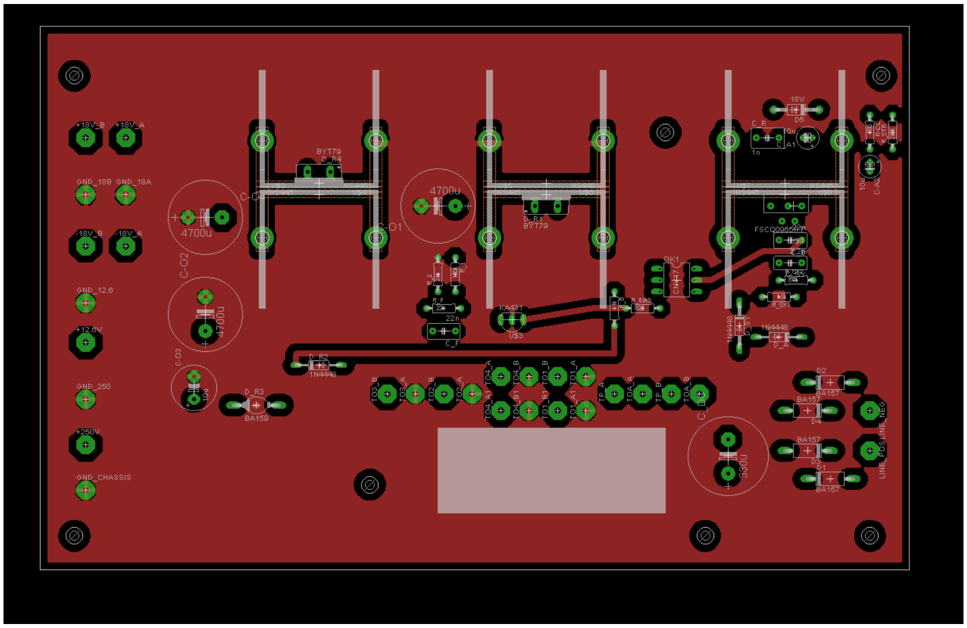
PCB Layouts

Power Supply Board

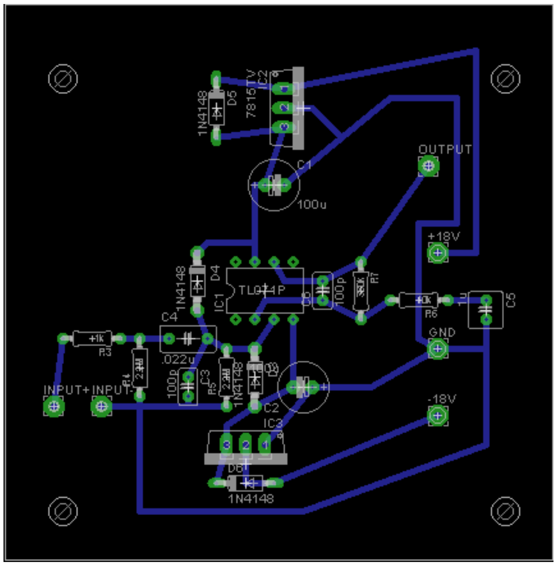
Bottom



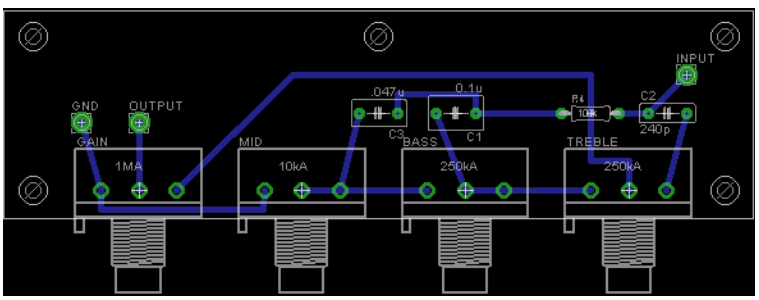
Top



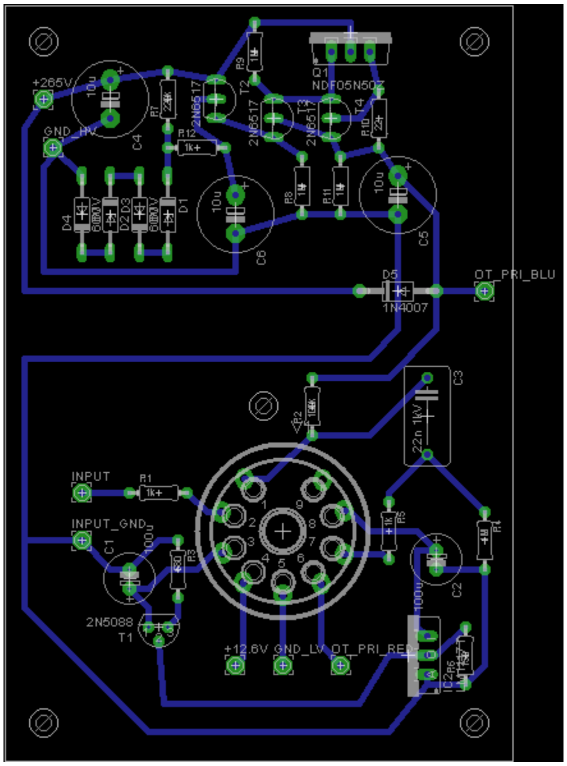
Solid-State Preamplifier



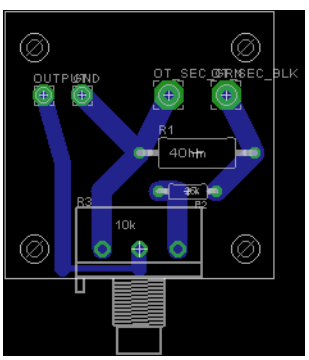
Gain & Tone Controls



Tube Amplifier

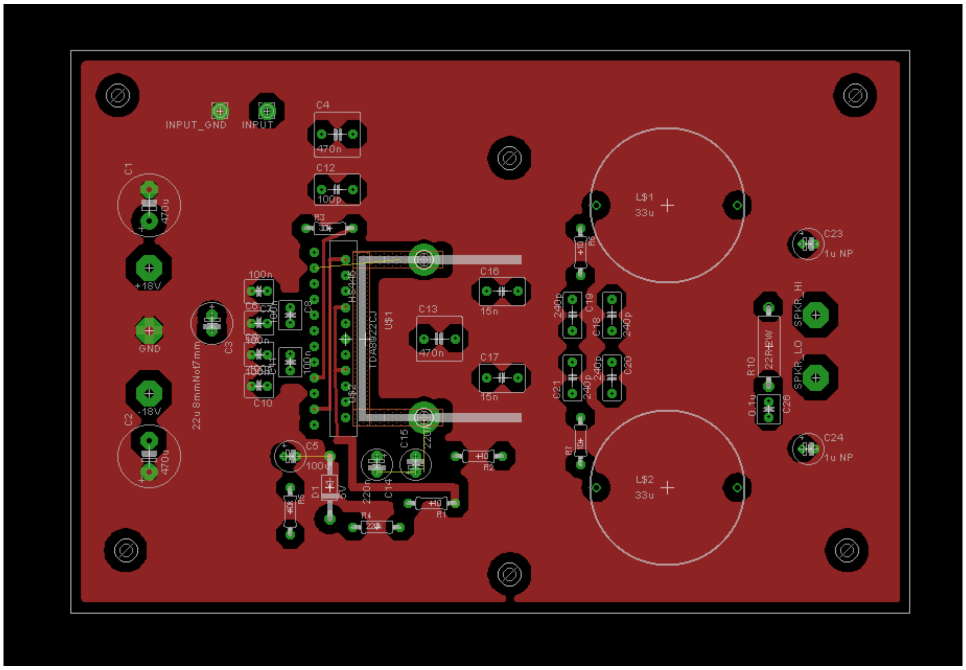


Resistive Load & Volume Control



Solid-State Power Amplifier

Top



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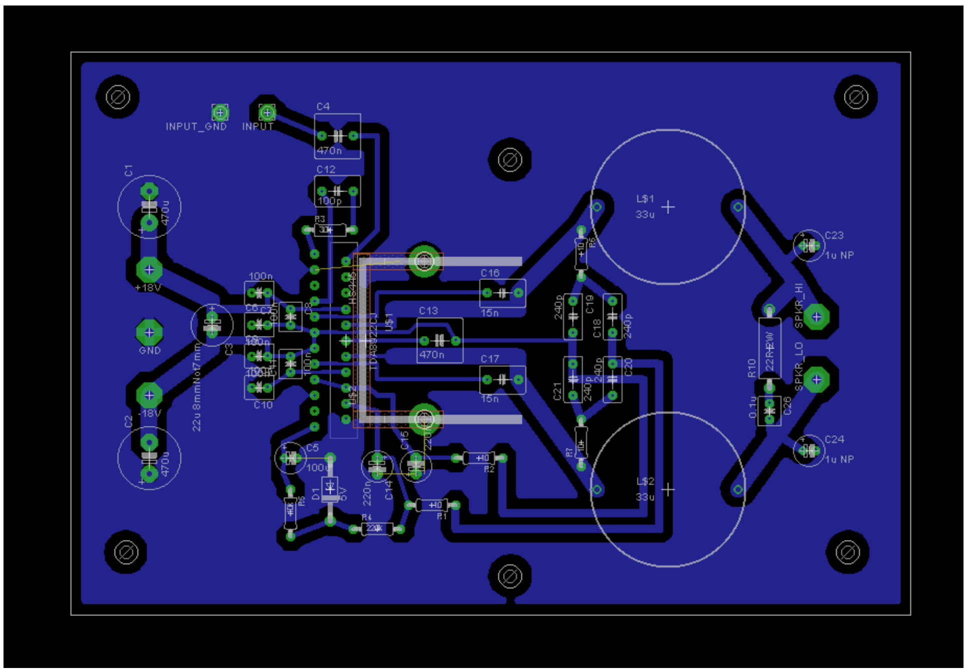


Power Supply Design Sheet

FAIRCHILD SEMICONDUCTOR™

FPS Design Assistant for AN4146
Ver 1.00 *by H.S. Choi*
Blue cells are the input parameters
Red cells are the output parameters

1. Define the system specifications

Minimum Line voltage (V_{line}^{min})	103.5	V.rms
Maximum Line voltage (V_{line}^{max})	137.5	V.rms
Line frequency (f_L)	60	Hz

	$V_{o(n)}$		$I_{o(n)}$		$P_{o(n)}$		$K_{L(n)}$
1st output (Vo1) ; regulated by feedback	18	V	2.50	A	45	W	46
2nd output (Vo2)	12.6	V	0.15	A	2	W	2
3rd output (Vo3)	260	V	0.03	A	7	W	7
4th output (Vo4)	18	V	2.50	A	45	W	46
5th output (Vo5)		V		A	0	W	0

Maximum output power (P_o) =	98.4	W
Estimated efficiency (E_{ff})	70	%
Maximum input power (P_{in}) =	140.6	W

2. Determine DC link capacitor and DC link voltage range

DC link capacitor (C_{DC})	330	uF
Minimum DC link voltage (V_{DC}^{min}) =	125	V
Maximum DC link voltage (V_{DC}^{max})=	194	V

3. Determine the reflected output (V_{RO})

Output voltage reflected to primary (V_{RO})	126	V
Maximum nominal Drain voltage (V_{ds}^{nom}) =	320	V

4. Determine transformer primary side inductance (Lm)

Drain voltage falling time (T_F)	2.3	us
Minimum Switching frequency of FPS (f_{s_min})	25	kHz
Maximum duty cycle (D_{max}) =	0.47	
Primary side inductance (L_m) =	500	uH
Maximum peak drain current (I_{ds}^{peak}) =	4.74	A
RMS drain current (I_{ds}^{rms}) =	1.88	A

5. Choose the proper FPS considering the input power and current limit

Typical current limit of FPS (I_{LIM})	6.00	A		
Minimum I_{LIM} considering tolerance	5.28	A	>	4.74 A
	->O.K.			

6. Determine the proper core and the minimum primary turns

Maximum flux density swing in normal mode (D	0.30	T	-->	N_p> 42.25 T
Maximum flux density in transient (B_{sat})	0.38	T	-->	N_p> 42.18 T
Cross sectional area of core (A_e)	187	mm^2		

Minimum primary turns (N_p^{min})=	42.2	T

7. Determine the number of turns for each output and Vcc drop circuit

Vo2 in standby mode (V_{o2}^{stby})	6.3	V	V_{o2}= 13 V in normal mode
Vcc auxiliary voltage drop ratio (K_{drop}) =	0.54		
Minimum V_a in standby mode (V_a^{stby})	13.0	V	
V_a in normal mode (V_a^{normal}) =	24.9	V	

	$V_{F(n)}$				# of turns	
Winding for Va (24.9V)	1.2	V	9.5	=>	10	T
Winding for Vo1 (18V)	1.2	V	7	=>	7	T
Winding for Vo2 (12.6V)	1.2	V	5.0	=>	5	T
Winding for Vo3 (260V)	1.2	V	95.2	=>	95	T
Winding for Vo4 (18V)	1.2	V	7.0	=>	7	T
Winding for Vo5 (V)		V	0.0	=>	0	T
Number of turns for primary winding (N_p)=	46	T	> 42.2 T			
	--->enough turns					

Ungapped AL value (AL)	4690	nH/T²			
Gap length (G) ; center pole gap =	0.94199	mm			
Maximum operating current of FPS (I_{op})	8	mA			
MOSFET input capacitance (C_{iss})	1750	pF			
Breakdown voltage of Vcc zener diode	18	V			
Current consummed by FPS (Icc) =	10.8	mA	at	90	kHz
Vcc drop resistor (Rcc)	0.7	kΩ	<	1	kΩ
Power dissipation of Rcc =	0.1	W			

8. Determine the startup resistor

Maximum Startup current of FPS (I_{start})	50	uA			
Startup resistor	240	kΩ	<	782	kΩ
Effective Vcc capacitor (Ce)	20	uF			
Maximum dissipation in startup resistor =	0.03	W	at	137.5 Vac	
Maximum startup time (T_{str}^{max}) =	2.66	s	at	103.5 Vac	

9. Determine the wire diameter for each winding

	Diameter		Parallel		$I_{D(n)}^{rms}$		(A/mm
Primary winding	0.7	mm	×	1	1.9	A	4.9
Winding for Vcc (24.9V)	0.3	mm	×	1	0.1	A	1.4
Winding for Vo1 (18V / 2.5A)	0.8	mm	×	2	6.0	A	5.9
Winding for Vo2 (12.6V / 0.15A)	0.4	mm	×	1	0.3	A	2.8
Winding for Vo3 (260V / 0.025A)	0.2	mm	×	1	0.1	A	2.0
Winding for Vo4 (18V / 2.5A)	0.8	mm	×	2	6.0	A	5.9
Winding for Vo5 (V / A)		mm	×		#####	A	####

Copper area (A_c) =	36.05	mm²
Fill factor (K_F)	0.2	

Required window area (A_{wr})	180.27	mm^2

10. Choose the rectifier diode in the secondary side

	$V_{D(n)}$			$I_{D(n)}^{rms}$	
Rectifier diode for Vcc	65	V		0.10	A
Rectifier diode for Vo1 (18V / 2.5A)	48	V		5.97	A
Rectifier diode for Vo2 (12.6V / 0.15A)	34	V		0.35	A
Rectifier diode for Vo3 (260V /0.025A)	663	V		0.06	A
Rectifier diode for Vo1 (18V /2.5A)	48	V		5.97	A
Rectifier diode for Vo5 (V /A)	0	V		#####	A

11. Determine the output capacitor

	$C_{o(n)}$		$R_{C(n)}$		$I_{cap(n)}$		$\Delta V_{o(n)}$
Output capacitor for Vo1 (18V / 2.5A)	470	uF	110	mΩ	5.4	A	1.7
Output capacitor for Vo2 (12.6V / 0.15A)	4700	uF	100	mΩ	0.3	A	0.1
Output capacitor for Vo3 (260V / 0.025A)	10	uF	100	mΩ	0.1	A	0.1
Output capacitor for Vo4 (18V / 2.5A)	470	uF	110	mΩ	5.4	A	1.7
Output capacitor for Vo5 (V / A)		uF		mΩ	#####	A	####

12. Design the synchronization network

Peak value of Sync voltage (V_{sync}^{pk})	9.0	V	$4.6 < V_{sync}^{pk} < 12V$ (V_{OVP})
Sync voltage divider resistor (R_{sy1})	1500	Ω	
Sync voltage divider resistor (R_{sy2})	848	Ω	
Effective output capacitance of MOSFET	1.1	nF	(Coss + Cr)
Sync capacitor (C_{sy})	2.2	nF	

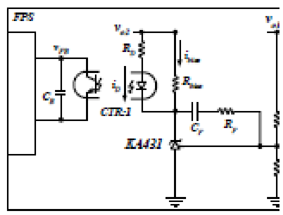
13. Design voltage drop circuit for the burst operation

Vo2 in standby mode (V_{o2}^{stby})	6.3	V
Breakdown voltage of zener diode, Dz	3.3	V

14. Design the feedback control circuit

Control-to-output DC gain =	9				
Control-to-output zero (w_z) =	19.3	krad/s =>	f_z=	3,080	Hz
Control-to-output RHP zero (w_{rz})=	167.4	krad/s =>	f_{rz}=	26,663	Hz
Control-to-output pole (w_p)=	951	rad/s =>	f_p=	151	Hz

Voltage divider resistor (R_1)	150	kΩ
Voltage divider resistor (R_2)=	24.2	kΩ
Opto coupler diode resistor (R_D)	1	kΩ
KA431 Bias resistor (R_{bias})	0.82	kΩ
Feeback pin capacitor (C_B) =	22	nF
Feedback Capacitor (C_F) =	22	nF
Feedback resistor (R_F) =	22	kΩ
Current transfer ratio of opto coupler (CTR)	80	%



Feedback integrator gain (w_i) =	679	rad/s =>	f_i=	108	Hz

Compensator zero (w_{zc})=	2066	rad/s =>	f_{zc}=	329	Hz
Compensator pole (w_{pc})=	16234	rad/s =>	f_{pc}=	2,585	Hz