USB 3.0 Outlet Conversion

Final Report

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May 2, 2012

ECE 445 Spring 2012

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Abstract

This paper showcases the final design and results of the USB 3.0 Outlet Conversion project. The purpose of this project was to address the growing need for efficient DC power used in household electronic devices. The project covered from the inception of the idea through to the implementation in hardware.

The final design involves a rectifier, flyback, and three dc/dc converters; each component was installed on a PCB. The entire assembled product was designed to fit within a standard wall outlet box. By performing the testing procedures, the electrical results were gathered for each of the design module under various loads. The electrical results were also discussed and compared to the verifications specification. In addition, there were discussions of design changes and the motivation behind it. The efficiency graphs are given over a variety of loads. A cost analysis shows individual parts, fabrication, and labor costs is also included.

Contents

1 Introduction

1.1 Purpose

The project aims to address the growth of external DC converters for consumer products. The objective of this project is to modify an AC wall outlet to include two DC ports. One of the DC ports will be a standard USB 3.0 port; the ratings of this port will be 5V/5A. The other one will be a high power, 12V/15A, output port. These additional outputs would eliminate the need for DC converters outside the wall outlet or in appliances.This product will promote the standardization of DC appliances. It will also further the transition to green technologies by removing the need for wasteful external converters and replacing them with higher efficiency permanent converters.

1.2 Project Functions

This project features a modified wall outlet that includes DC outlet. Although the standard wall outlet is modified it maintains a simple installation process for the users. The product will be designed to achieve a high efficiency during the conversion between AC to DC power and DC voltage levels. It will also provide a more ascetically pleasing environment for the user by eliminating bulky external DC converters. In addition by eliminating external DC converters, it reduces the pollutions due to the disposal of it.

1.3 Subprojects

We split the project into modules for an easier debugging process; the modules are shown in the block diagram in Figure 1.

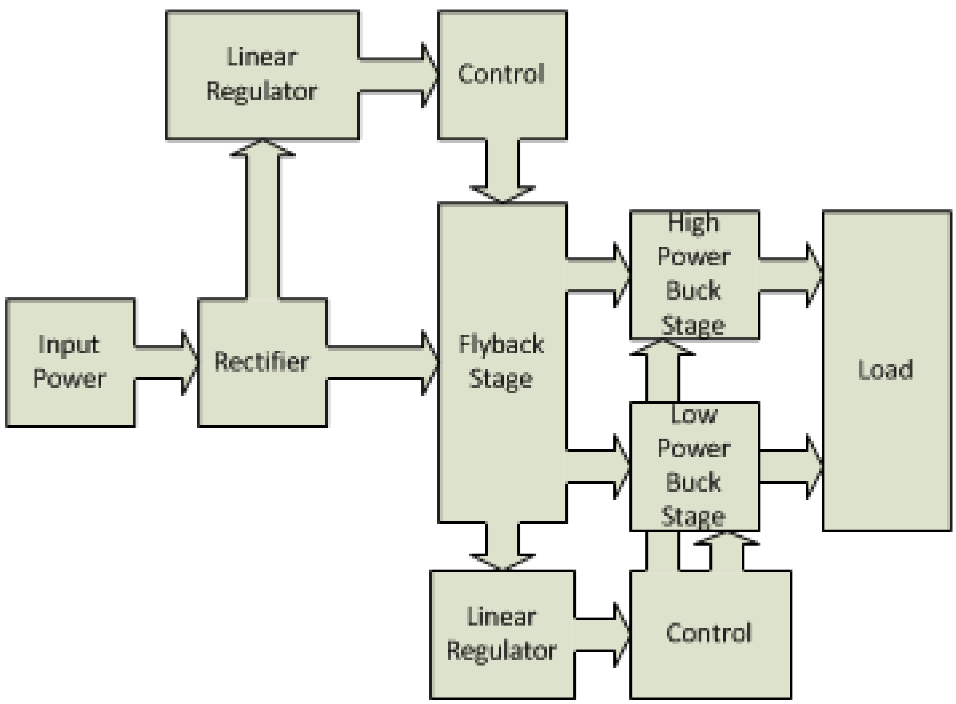


Figure 1: Block Diagram

1.3.1 Start-up Sequence

The start up sequence is power flows through the rectifier converting the AC to DC, which is smoothed out by a capacitor bank. This powers the two linear regulators which allows the PWM chip to switch. Then the MOSFET of the flyback begins switching which permits the power flow between the input and output of the flyback. A the output of the flyback a stable 25 V is established and sent to an other linear regulator to supply an enable voltage for the buck converter control chips. The outputs of the low buck and high buck are 5 V and 12 V respectively at the various loads.

1.3.2 Control

The original control block was designed to operate with a MSP430 chip. However, this was determined unnecessary and was replaced with an integrated circuit (IC) chip. Therefore the control system is divided into three components; one for each power converter. The TPS5450 was selected for the low power buck control because it contains internal control and the MOSFET needed for the circuit. The original design of the high buck converter was to utilize the TPS40200 as its control system. But there were many technical difficulties with this IC chip so another design approach was taken. The alternative approach was to use a PWM controller with a high side gate driver for the high buck converter control. The UCC3851, a power factor correction (PFC) controller, was selected for the flyback converter but for the commercial design of this product a decision was made to use the UC3843 controller, which is a simpler PWM controller. Using different control chips for each block allowed for features to be selected that benefited each subsystem.

1.3.3 Linear Regulators

The linear regulators were used to step down the voltage to 12 V and used to power the IC control chip. The linear regulators selected were the TI TL783s. These regulators allowed us to step down output from the rectifier to 75 V and then again to the 12 V required. Output capacitance to reduce ripple was used.

1.3.4 Rectifier

The rectifier was implemented using an H-bridge rectifier chip for reduced voltage drop and higher efficiency. The rectifier has to be outfitted with output capacitance to ensure stability for the linear regulators. This also reduced the ripple seen by the output of the flyback converter.

1.3.5 Flyback Stage

A useful property of the flyback topology is galvanic isolation between the output and input. Galvanic isolation means that no electrons pass from the input to the output. The energy is transferred via a magnetic field coupling in a coupled inductor. The topology estimates the properties of an ideal transformer and provides a turns ratio. The flyback stepped down the voltage before the input of the buck converter. By stepping the voltage in two stages, the circuit components can be sized down. In addition, a high power factor was achieved with this topology.

1.3.6 High Power Buck

The high power buck converter stepped down the voltage from 25V to 12V. The converter maintained line regulation and controlled ripple.

1.3.7 Low Power Buck

The low power buck converter stepped down the voltage from 25V to 5V. Similar to the high power buck converter, the lower power converter maintained line regulation and controlled ripple.

1.3.8 Load

The system load was a varying electronic load for testing purposes. The final demo load for the low power circuit was charging two different cell phones including an Android phone and an iPhone 4. The final demo load for the high power circuit was an electric drill.

2 Design Overview

2.1 Overall Circuit Schematics

The project overall circuit schematic is provided in Figure 2.

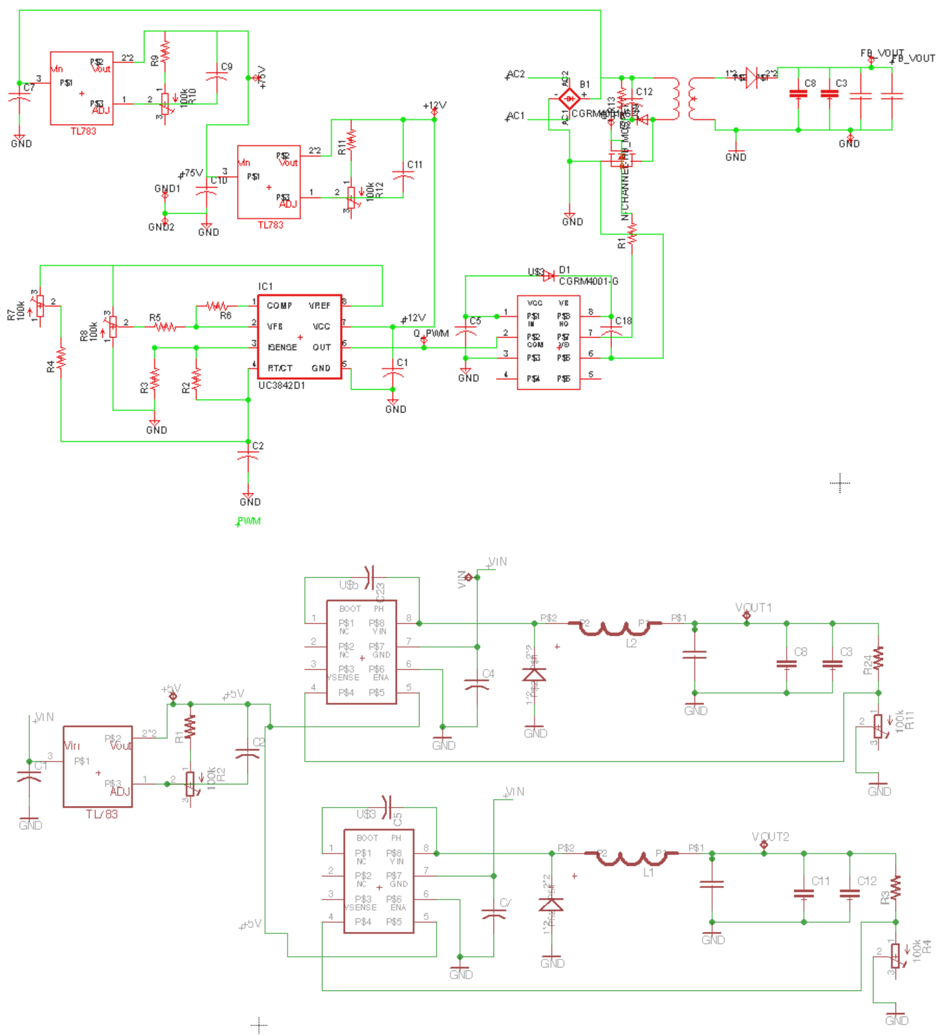
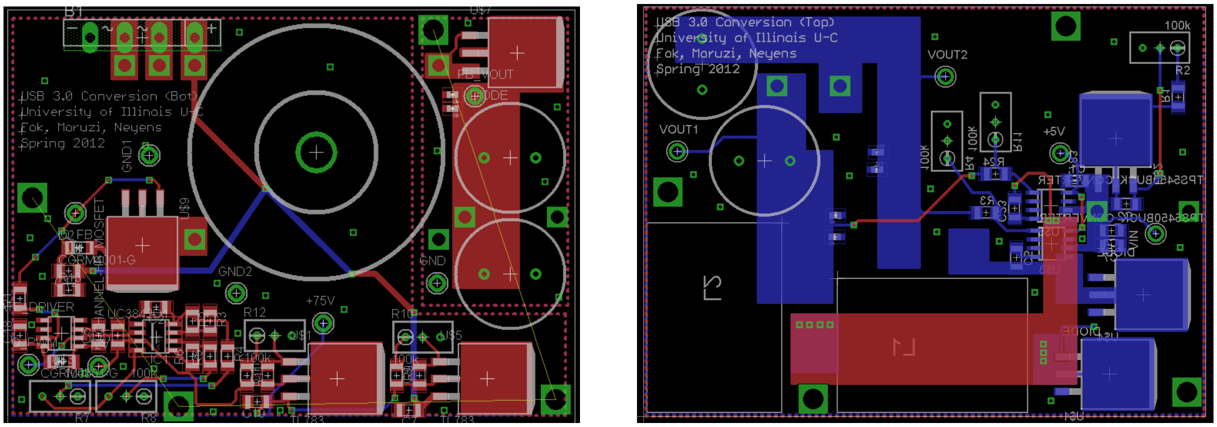


Figure 2: PCB Schematics
(Top) Rectifier, Flyback, Linear Regulators
(Bottom) Low Buck



(a) Bottom - Rectifier/Flyback

(b) Top - Two Buck Stages

Figure 3: Printed circuit boards

Figure 3 above shows the final PCB layout for this project. As mentioned before one of the requirements was circuit needed to fit inside a standard 4" x 4" wall outlet box. In order to accomplish this, we split the circuit onto two interlocking PCBs. The components were laid out in such a way that the tall ones were installed on opposite ends. This way the two boards could "interlock" like a sandwich and save space. We were concerned about thermal effects, but determined that the large ground plane installed on the boards was enough to dissipate the heat.

See Appendix C for all component schematics from data sheets.

2.2 Performance Specifications

Table 1: Performance Specifications

Specification	Value
Input Voltage (V ac rms)	120
Max Input Current (A)	15
Input Frequency (Hz)	60
Flyback Output Voltage (V)	25
Flyback Output Current (A)	10
Flyback Switching Frequency (kHz)	100
Low Buck Output Voltage (V)	5
Low Buck Output Current (A)	5
High Buck Output Voltage (V)	12
Low Buck Output Current (A)	15
Load Regulation (%)	0.5
Max Start-up Current (A)	10
Output Ripple (%)	± 1
Power Factor	0.85
Efficiency (%)	85

2.3 Rectifier

The GBU6D bridge rectifier chip was used. This chip was selected based on the ratings calculated below; it contains ratings of 140 V_{rms} and 6 A.

Voltage Rating:

$$V_{pk} = \sqrt{2} * V_{rms} = \sqrt{2} * 120 = 169.7V \quad (1)$$

$$V_{DC} = \frac{2 * V_{pk}}{\pi} = 108V \quad (2)$$

$$V_{diode}(max) = 170 - 108 = 62V \quad (3)$$

Current Rating: 3A

In order to supply a smoother DC voltage and reduce noise into other modules, a capacitor bank of 156 μF was added to the output of the rectifier.

2.4 Linear Regulator

In total there were three linear regulators used in the design. Two of which were used to provide power to the control system of the flyback. In order to provide this power, there was a need for a voltage drop from 108 V_{dc} to 12 V_{dc}. But to accomplish this voltage drop, it needed to be a two step process. The other linear regulator was used to drop the voltage from 25 V_{dc} to 5 V_{dc} enable the two buck stages.

In the two step linear regulator circuit is shown in Figure 4. The cicuit receives the 108 V output from the rectifier. With the added capacitance at the rectifier output, a smoother linear regulator output voltage was seen. But the TL783 was limited to a 125V difference between the input and output of it. Also as the input and output voltage difference increase, the TL 783 will operate at a higher temperature. Therefore in order to avoid over stressing and heating the component, a 75V bus was created to supply the second linear regulator.

To calculate the resistances required to set the output voltage of each regulator: R_1 was set to be 82Ω and (4) was used. The calculated value of R_2 was used to size a potentiometer. The potentiometer was used to change the output voltage on each linear regulator for different testing criteria. In the datasheet of TL783, it stated that V_{ref} is an internal voltage of 1.25 V.

$$V_0 = V_{ref}(1 + \frac{R_2}{R_1}) \quad (4)$$

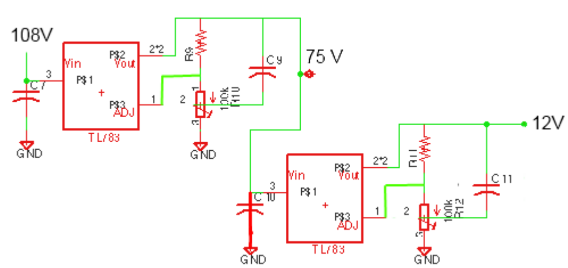


Figure 4: Linear Regulator Flyback board

2.5 Flyback Converter

2.5.1 Flyback Circuit Design

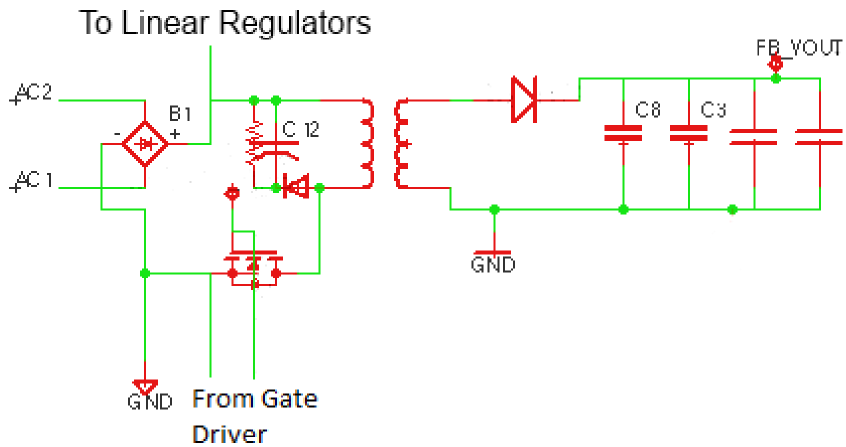


Figure 5: Flyback Stage Topology

2.5.2 Challenges

A design challenge for the flyback was the ringing noised caused by operating the MOSFET at high frequency. The solution to this was to incorporate a snubber circuit into the design topology. Another challenge was to balance the operation frequency with the inductor component size and system loss. Operating the circuit at higher frequency would lower the inductance and the size of the inductor. The higher frequency would also increase the system losses that are caused by the switching components.

2.5.3 Operation Mode

To avoid saturation, the converter has been designed to operate in discontinuous conduction mode (DCM). The DCM design requires a smaller inductor.

2.5.4 Gate Driver

The power factor correction IC will send a switching signal through a gate driver to the MOSFET. The gate driver is needed for two reasons. The first reason is to provide isolation between the grounded PFC chip and the MOSFET gate. The source of the MOSFET will not be at ground, thus a low side gate driver would not work.

The second reason is to supply the current needed to charge the gate capacitance of the MOSFET. The MOSFET gate current can be considerable, see [1], and must be supported by a dedicated gate driver.

2.6 Buck Converter Stages

2.6.1 Challenges

The design of a buck converter depends on three main factors, input voltage, output voltage, and switching frequency. The input and output voltages determine the power ratings for the components. The switching frequency determines the physical size of the inductor and capacitor. The switching frequency posed a design challenge in balancing switching losses, explained above, and the size of the components. The project design is centered around being small and its ability to fit into a standard wall outlet, so a large switching frequency is favored. Efficiency is also a major design criteria for the project, and favors a lower switching frequency. The selected switching frequency was chosen with these two factors in mind.

The buck converters are the final stages in the circuit and are responsible for the quality of the output voltage. The amount of voltage ripple was taken into account when the capacitance of the buck converters was determined. A small capacitance has a large voltage ripple at the output, but saves space. A large capacitance reduces the output voltage ripple, but consumes a larger space.

2.6.2 Buck Converter Topology

Both low and high power buck converter topologies are derived from the circuit shown in Figure 6. For a clearer visual of the switching operation the MOSFET is displayed as a ideal switch. The buck converter has two stages: on stage and off stage. During the on stage the MOSFET is on and the diode is in reverse bias, which allows current to flow in to and store energy in the inductor. Then during the off stage the diode is in forward bias mode and the MOSFET is off. This allows the stored energy in the inductor and capacitor to maintain the output voltage.

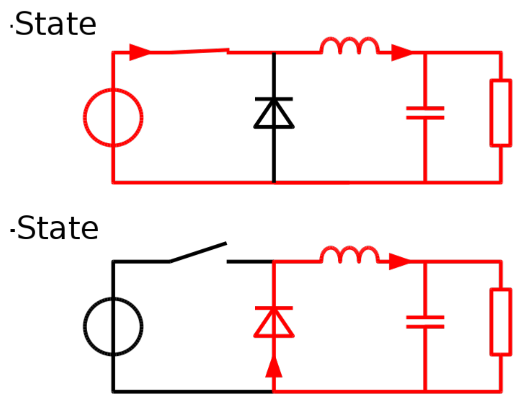


Figure 6: Buck Converter (Top) On State (Bottom) Off State [3]

From Figure 6, (5) to (9) was derived and the component ratings can be computed.

$$D_1 * V_{in} = V_{out} \tag{5}$$

$$V_{diode} = V_{in} \tag{6}$$

$$I_{diode} = (1 - D_1) * I_{out} \tag{7}$$

$$V_{mosfet} = V_{in} \tag{8}$$

$$I_{mosfet} = D_1 I_{out} \tag{9}$$

2.6.3 Low Power Buck

Shown in Figure 7is the final design schematic of the low buck module.

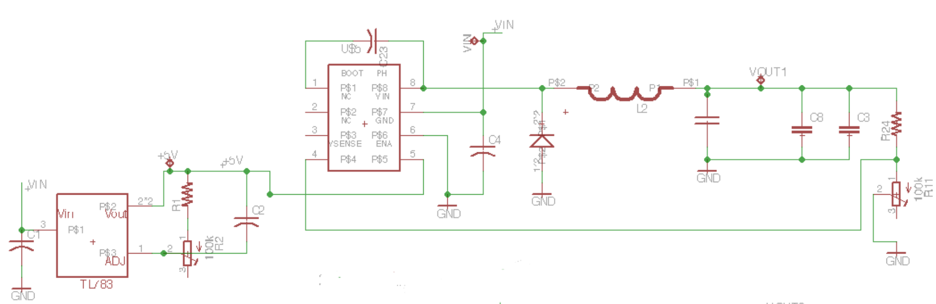


Figure 7: Low buck Converter [3]

The low power buck was implemented using TPS5450, an IC chip. This chip meet all required voltage and current ratings as the discrete components. With (5) to (9) the rating for discrete components was calculated and the values are displayed in Table 2.

Table 2: Low Power Buck Ratings

D_1	V_d (V)	I_d (A)	V_{fet} (V)	I_{fet} (A)	I_o (A)	V_o (V)	I_i (A)	V_i (V)	I_{chip} (A)	V_{chip} (V)
.2	25	4	25	1	5	5	1	25	6	36

The TPS5450 had the capability to handle the required current and voltage ratings safely. The TPS5450 also included the MOSFET and controls for linear regulation. Along with the TPS5450, there is an external diode, capacitor and inductor for the low power buck converter.

2.6.4 High Power Buck

Unlike the low power buck converter, the high buck module was built using discrete components and a controller. The component was selected based on individual calculated ratings. With (8) and (9), the high power buck MOSFET ratings was computed and the values are tabulated in Table 3. The high power buck diode ratings was calculated from (6) and (7), values shown in Table 3. Along with the calculated ratings for the high power buck converter, the selected component ratings are also listed in Table 3. In order to protect the circuit against noise and ripple that occurs in non-ideal components, the select components have higher ratings than calculated. Also over-sizing the components helps improve the reliability of the circuit. This approach was chosen in order to handle the current requirements.

Table 3: High Power Buck Ratings

	D_1	V_d (V)	I_d (A)	V_{fet} (V)	I_{fet} (A)	I_o (A)	V_o (V)	I_i (A)	V_i (V)
Theoretical Ratings	.48	25	7.8	25	7.2	15	12	7.2	25
Actual Component Ratings	-	30	10	40	15	-	-	-	-

2.7 Design Changes

The largest change of the design since the design review was the move to PCBs. We initially thought we would build a single PCB. After considering our form factor needs we decided to go to a double PCB design. This required some forethought and mechanical design. All of the larger components had to fit within the space between the PCBs. In the end, we were able to complete PCBs that accomplished the desired space requirements.

Due to time we were unable to make a PCB for the high buck stage. We resorted to a vector board design. In compensation we added a second low buck to the bottom PCB. One of the challenges that we encountered with this was high ESR capacitors. At the higher current loads we noticed that the decoupling capacitors were heating up. This was due to the high ESR. We mitigated this problem by using several capacitors in parallel which increased our capacitance and decreased the ESR. With surface mount components we believe we would be able to push this design even further with lower ESR capacitors.

Another design change was the addition of capacitance to the output of the rectifier. This was to ensure a steady output for the linear regulators. To achieve the appropriate voltage rating we used several capacitors in parallel. A capacitance of 260 μF was used. This provided enough stability for the linear regulators to operate reliably.

During testing of our original coupled inductor we encountered problems with saturation and wire resistance. On the second revision we moved to a larger core and larger wire size. We developed a winding method that allowed us to use the large wire and to wind it neatly.

3 Simulations

Figure 8 below shows the schematic of the simulation. A rectifier, flyback converter with a turns ratio, and two buck converters are realized. All components are modeled with realistic parasitics such as on-state losses and magnetizing inductance.

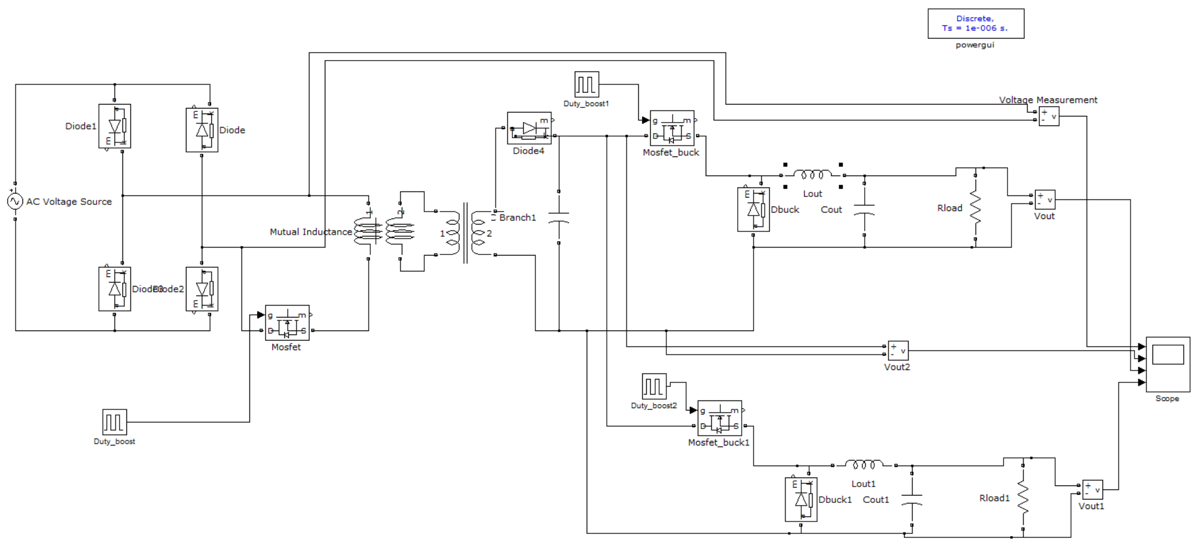


Figure 8: Simulation Schematic

3.1 Simulation Results

Figure 9 below shows the simulation results. Axis one shows the output of the rectifier bridge. The peak is 169 V and the frequency is 60 Hz. Axis two displays the output of the flyback converter with an output capacitance of 10 mF. This is still a large capacitance and will require more design thought. Axis three displays the output of the high power buck converter with a duty ratio of 82%. This is well within the achievable range for duty ratio. Axis four shows the output of the low power buck converter with a duty ratio of 25%.

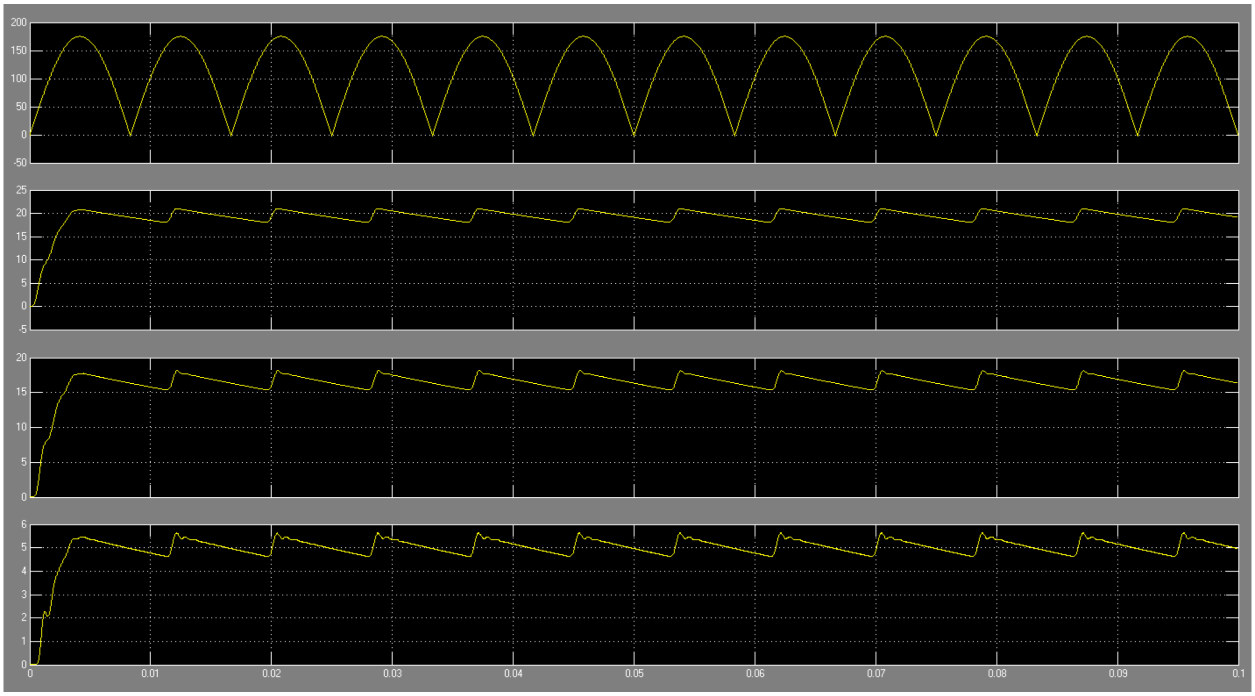


Figure 9: Simulation Results

The simulation exercise were used to confirm rough estimates of our design values. Moving forward the design will be optimized through lab testing.

4 Design Verification

The circuit was built in modules and each module was tested individually. After separate testing the modules were placed together to test the overall circuit. The testing and verification procedure table can be found in Appendix F.

4.1 Rectifier Circuit

The rectifier circuit was used to convert 120 V AC to 108 V DC. For safety reasons, we utilized a Variac to adjust the input AC voltage when testing the rectifier circuit. Figure 10 is the rectifier input (Channel 2) and output (Channel 1) voltage waveform.

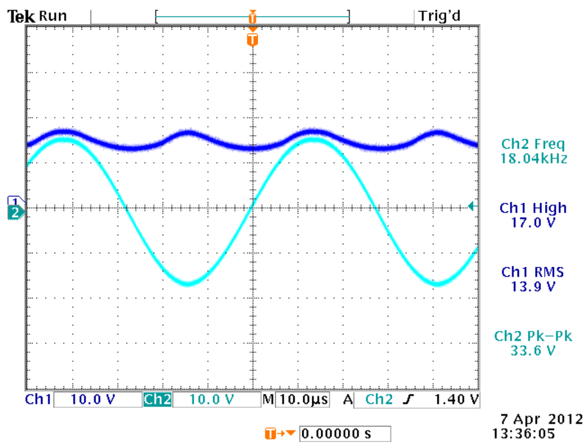


Figure 10: Rectifier Circuit Testing Waveform

During testing a capacitor bank of 156 μF was added to the design to improve the voltage ripple to meet the specified requirement of ±2.16V. This capacitor bank also stabilized the output for the linear regulators. The additional capacitors resulted in a output voltage ripple of ±1.7V .

After the adjustments to the circuit design, the rectifier circuit was able to maintain an efficiency of 97.37%.

4.2 Linear Regulators

The linear regulators were used to provide 12V and 5V to the IC control chips. In order to test the linear regulators, a DC voltage input and a load was provided. Figure 11 shows the waveform gathered during testing of the linear regulators.

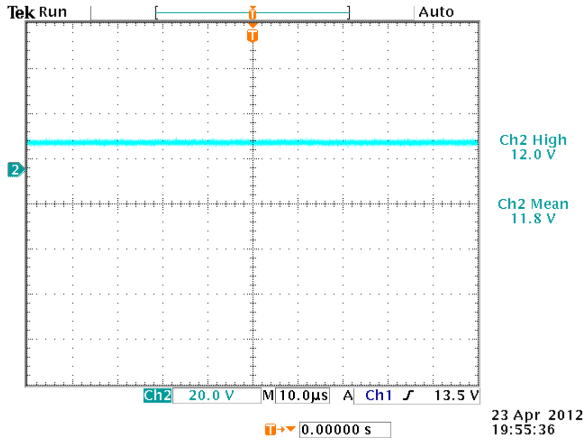


Figure 11: Linear Regulator Circuit Testing Waveform

From the waveform, it shows that the linear regulator is able to maintain a 12V output to power the IC chips.

4.3 Flyback Stage

The PFC controller was replaced with a PWM controller. Figure 12 is the waveform of the PWM control signal for the Flyback stage without the bridge rectifier as the input.

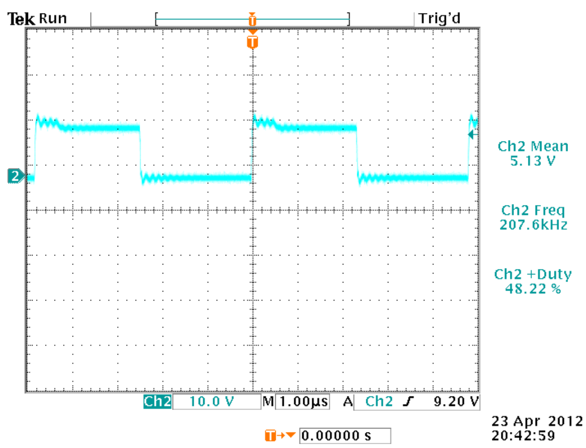


Figure 12: Flyback PWM Controller Waveform

The flyback PWM controller was able to maintain a variable duty ratio and a nominal ratio of 48.22%. This meets the requirements specified for the flyback PWM controller.

Figure 13 shows the noise from the switching signal when the flyback input is provided from the output of the rectifier. Also in Figure 13, channel 1 was the output of the second voltage regulator, channel 2 was the output of the first voltage regulator, channel 3 was the output of the bridge rectifier and channel 4 was the switching signal from the controller.

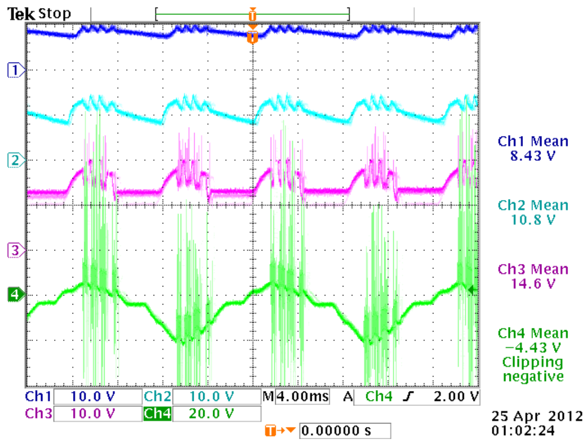


Figure 13: Noise on the Switching Signal of Flyback Circuit Waveform

Another challenge with the flyback converter was the floating ground. In Figure 14 the switching signal referenced to grown is shown. It can be seen that the switching signal is imposed on top of the "ac" input waveform. Also it has the same channel arrangements as Figure 14.

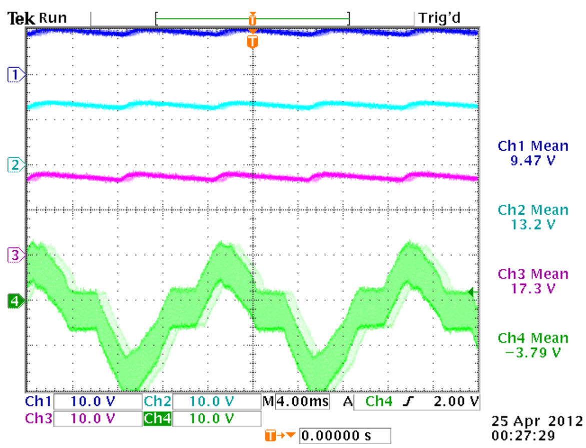


Figure 14: Flyback Issues with Floating Ground

4.4 Low Buck Stage

The low buck stage should provide a 5V/5A output. In Figure 15, it shows the low buck converter with an electronic load. The electronic load was set to draw 4.75A current. In this Figure, channel 1 was the input voltage; channel 2 was the output voltage, and channel 3 was the output current of the low buck converter.

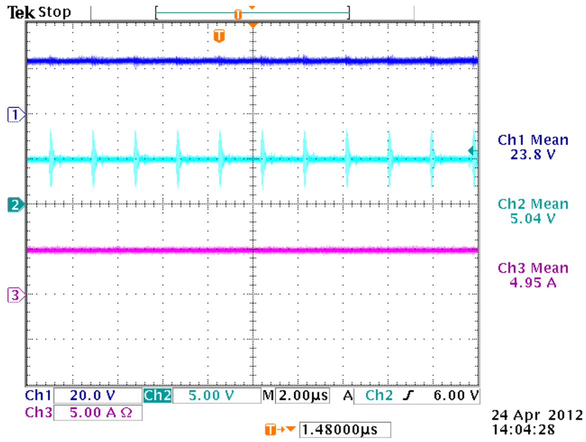


Figure 15: Low Buck Stage Waveform

The low buck converter was able to maintain an average output voltage of 5V. It was also able to maintain a ripple of ±100mV, which is much better than the specified requirements. In addition the low buck stage had an average efficiency of 80.3% and can be seen in Figure 16.

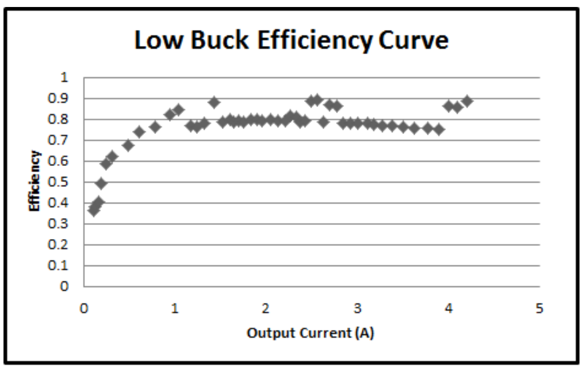


Figure 16: Low Buck Efficiency vs Load

4.5 High Buck Stage

Figure 17 shows the High Buck stage loaded with the drill. Channel 1 shows the 25V input from the DC power supply. Channel 2 shows the gate signal of the MOSFET. Channel 3 shows the PWM controller output. Channel 4 shows the output voltage with a load drawing 3.5A

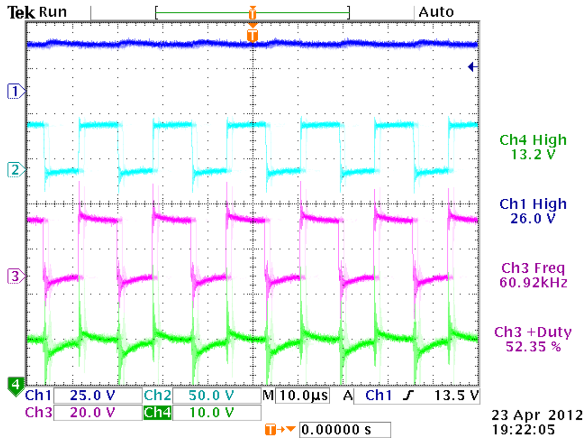


Figure 17: High Buck Stage under drill load

Figure 18 below shows the efficiency of the High Buck converter at various loads. We were impressed with the high efficiency of this converter given that it was made on a vector board. We were able to reach our goal efficiency across most of the load range except at very low loads.

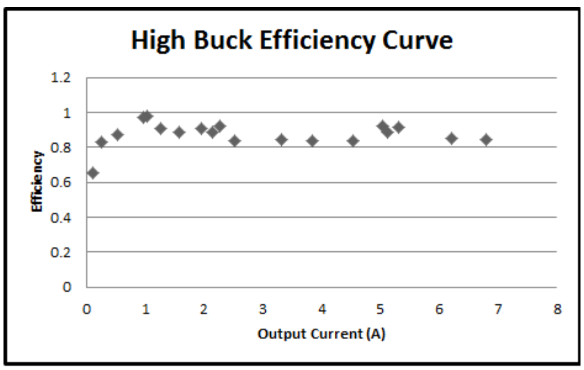


Figure 18: High Buck Stage efficiency

5 Cost

5.1 Labor

Table 4 describes the amount of time and salary of each member of the team is estimated to earn if the product were manufactured in a business setting.

Table 4: Labor Cost

Name	Rate	Hour	Total = Rate * Hour * 2.5
Cindy Fok	\$50/hr	180	\$22,500
Andrew Moruzi	\$50/hr	180	\$22,500
Tyler Neyens	\$50/hr	180	\$22,500
		Total	\$67,500

5.2 Bill of Materials

The parts selected are bases on the specifications of the wall outlet converter design. Some components are slightly oversize to protect the circuit from potential damage during testing. In Appendix B, there are tables that describe the cost of each module of the circuit. The total cost of materials for this project was \$ 197.28. The cost summary is each module is shown in Table B.8 in the Appendix.

Total Project Cost = \$67,600 + \$197.28 = \$ 67,797.28

6 Conclusion

6.1 Accomplishments

A fully functional project was obtained during this semester. The project met the size requirement which was the main goal of the group. We wanted to show that our product could be functional, practical, and hidden from view in a wall. This was done through multiple design revisions and creativity. The sandwich configuration of the PCBs is the highlight of our project. It involved careful consideration of component placement and a detailed understanding of the main power path through the circuit. It was through this design that the project can easily be placed inside a common household electrical box.
Each PCB was tested separately, but due to an over site in the testing procedure were never tested together. The output of the flyback PCB was maintaining a constant DC voltage that simply needed to be connected via wire to the buck PCB. The buck PCB had been tested by supply a DC voltage, and worked flawlessly.

6.2 Uncertainties

The major challenge for this project was the high buck converter. The challenge in this module was the high current rating that we insisted on. This rating was decided upon based on the standard of 120 Vac current for the US household. Our assumption was that this product will need to compete with the AC appliances. Most DC appliances, such as computers, do not require a current anywhere near our 15A design specification. A laptop charger requires 3-5A.

6.3 Future Work

The prototype of this product fully complies with the requirements for the project. However, like all products there is still room for improvement. The first improvement for the circuit would be the use of low ESR (Equivalent Series Resistance) capacitors being used throughout the circuit, but specifically in the high buck circuitry. The capacitors were found to be the limiting factor for the current in this component. Using low ESR capacitors would allow for the capacitors to dissipate less energy, which would increase the efficiency in the module. It would also cause less energy to be dissipated as heat. Heat is a real concern during this project because our circuit would be encased in a wall with little to no ventilation.
Another improvement on the circuit would be the size of the overall circuit and the components. The PCB for the circuit was built in an interlocking sandwich. There were two PCBs which where designed so that the tall components on one, mainly the inductors and capacitors, would be placed over the surface mount components of the other. This design allowed for minimum space. This same design would be used, but it is the consensus of the team that both PCBs could be designed with tighter component placement in order to reduce the size of the board. This goes hand in hand with the increase in switching frequency. By increase the switching frequency of all the modules, smaller inductors and capacitors can be used. This would not only conserve board space, but also allow for a smaller vertical separation of the two PCBs. The reason higher switching frequencies were not used during this stage is because of the heat concern. With higher frequencies comes higher switching loss, which results in more heat being created by the circuit. There would have to be extensive analysis on the proper switching range to maintain safety.
With the final circuit design, all of the potentiometers, will be replaced with resistors. The reason potentiometers were used in this design in order to change the values to match certain testing and debugging procedures. The removal and replacement of the potentiometers would decrease the board space by a considerable amount.

6.4 Ethical Considerations

The main ethical issue of the USB 3.0 Outlet is user safety; which correlates with IEEE Code of Ethics #9: "to avoid injuring others, their property, reputation, or employment by false or malicious action" [2]. As a consumer product there are several safety concerns associated with a power outlet. Therefore the goal is to developed the safest product possible to ensure user safety. To accomplish this, there is a need for short circuit protection. This would avoid damage to the equipment and act as a protection precaution for the user. Along with the short circuit, it is necessary to design a high power safe connector to create a more durable product. This connector would allow the user to disconnect from the outlet abruptly or harshly without damaging the internal circuit or harming the user.

References

[1] Hussain, Abid. "Driving Power MOSFETs in High-Current, Switch Mode Regulators." www.microchip.com. 2002. Web. 18 Feb. 2012. <http://ww1.microchip.com/downloads/en/appnotes/00786a.pdf>.

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Appendix A

Coupled Inductance Design Calculations

Appendix B

Complete List of Bill of Material

Appendix C

Data Sheet Schematics

Appendix D

PCB Layout

Appendix E

Each Modular Circuit Design

Appendix F

Testing and Verification Table