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# USB 3.0 Outlet

## Design Review

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# Contents

# 1 Introduction

## 1.1 Motivation

The project aims to address the growth of external DC converters for consumer products. The objective of this project is to modify an AC wall outlet to include two DC ports. One of the DC ports will be a standard USB 3.0 port; the ratings of this port will be 5V/5A. The other one will be a high power, 12V/15A, output port. These additional outputs would eliminate the need for DC converters outside the wall outlet or in appliances. This project was selected because of the group's common interest in power electronics. It is also commercially viable and the implementation of this product to an existing wall outlet would be simple. This product will promote the standardization of DC appliances. It will also further the transition to green technologies by removing the need for wasteful external converters and replacing them with higher efficiency permanent converters.

## 1.2 Objectives

The modified wall outlet intends to include USB compatibility and maintain a simple installation process for the users. The product will be designed to achieve a high efficiency during the conversion between AC to DC power and DC voltage levels. It will also provide a more ascetically pleasing environment for the user by eliminating bulky external DC converters.

### 1.2.1 Consumer Benefits

- Increased efficiency; save money on power bill
- Quieter appliances
- User-friendly; easy to install
- Fewer "wall warts" (external DC converters)
- Reduce pollution due to disposed converters
- Continued use of AC wall outlet; added feature of two DC outlets

### 1.2.2 Product Features

- Two DC outputs with two power levels options
- In-wall installation
- High efficiency
- Two 120V/15A AC outlets
- Eliminated need of additional power converter
- Simple installation process
- High power factor and low harmonic distortion

# 2 Design

## 2.1 Block Diagram

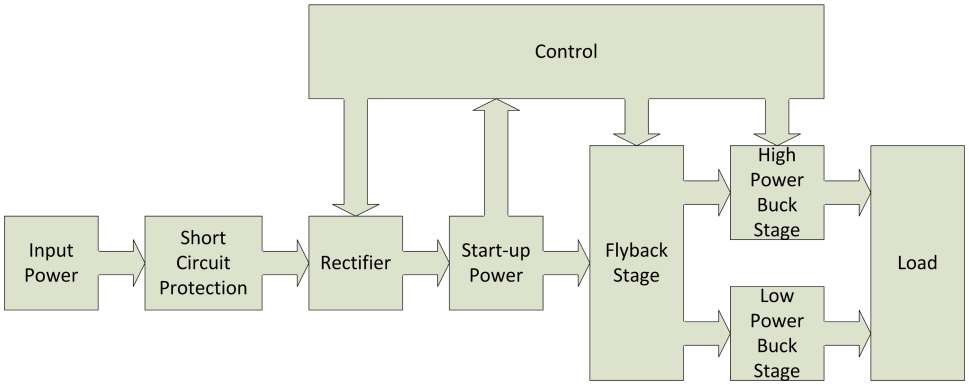


Figure 1: Block Diagram

### 2.1.1 Block Descriptions

**Control** The original control block was designed to operate with a MSP430 chip. However, this was determined unnecessary and was replaced with an integrated circuit (IC) chip. The TPS5450 was selected for the low power buck control because it contains internal control and the MOSFET needed for the circuit. The TPS40200 was chosen for the high power buck. And the UCC3851, a power factor correction (PFC) controller, was selected for the flyback converter. Using different control chips for each block allows for features to be selected that benefit the circuit.

**Rectifier** The rectifier will be implemented using an H-bridge rectifier chip for reduced voltage drop and higher efficiency.

**Start-up Power** The start-up sequence will be implemented using the soft start capabilities of the controller ICs. The on-state set point can be established using RC circuits and the controller can operate at a lower voltage until the main power supply stabilizes its output. A consideration to supply the controller IC power is to add a third winding to the flyback coupled inductor. This output would serve as power supply the IC once the steady state voltage has been achieved. The buck converter chips also have a soft start capability which would limit the stress induced on the system during the initial start of the system.

**Short Circuit Protection** The short circuit protection circuit will limit the amount of output current during short circuit conditions. The circuit will detect a short circuit and power down the outlet. This added protection will increase the safety of the outlet.

**Flyback Stage** A useful property of the flyback topology is galvanic isolation between the output and input. Galvanic isolation means that no electrons pass from the input to the output. The energy is transferred via a magnetic field coupling in a coupled inductor. The topology estimates the properties of an ideal transformer and provides a turns ratio. The flyback will step down the voltage before the it is input into the buck converter. By stepping the voltage in two stages, the circuit components can be sized down. In addition, a high power factor is achievable with this topology.

**High Power Buck** The high power buck converter will step down the voltage from 25V to 12V. The converter will maintain line regulation and control ripple.

**Low Power Buck** The low power buck converter will step down the voltage from 25V to 5V. Similar to the high power buck converter, the lower power converter maintain line regulation and control ripple.

**Load** The system load will be a varying electronic load for testing purposes. The final demo load for the low power circuit will be charging three different cell phones including an Android phone and an iPhone 4. The final demo load for the high power circuit will be an electric drill.

# 3 Component Design

## 3.1 Schematic

The project overall circuit is shown in Figure 2. In order to simplify the design process of a PCB board later, this schematic was drawn with Eagle CAD software. The schematic, like the circuit, is designed in a modular fashion for easy debugging. Each module of the design is explained in the following sections.

Standard packages were chosen for each type of component. This will ease the board layout and testing process. The 1206 package was used for all of the small resistors and capacitors. The D2PAK package was chosen for MOSFETs and diodes. The SOIC-8 and SOIC-16 packages were chosen for control IC chips. These standard surface mount packages were already in the Eagle library. The PFC, gate driver, low buck converter, and high buck controller were all drawn using the Eagle CAD software. The symbol for these components are labeled with pin numbers and names to assist in the wiring on the breadboard for testing.

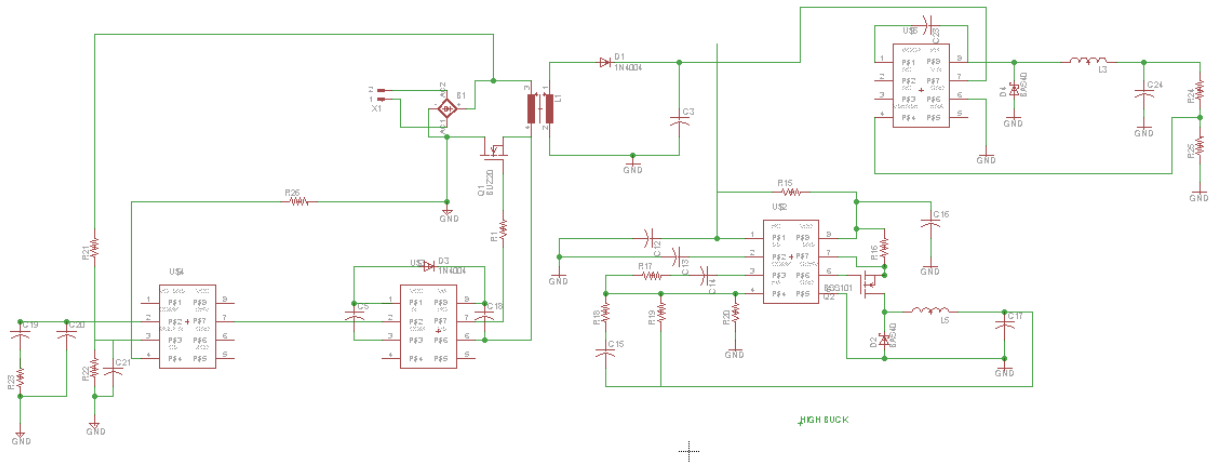


Figure 2: Eagle Schematic

See Appendix C for all component schematics from data sheets.

## 3.2 Performance Specifications

Table 1: Performance Specifications

| Specification | Value |
|---|---|
| Input Voltage (V ac rms) | 120 |
| Max Input Current (A) | 15 |
| Input Frequency (Hz) | 60 |
| Flyback Output Voltage (V) | 25 |
| Flyback Output Current (A) | 10 |
| Flyback Switching Frequency (kHz) | 100 |
| Low Buck Output Voltage (V) | 5 |
| Low Buck Output Current (A) | 5 |
| High Buck Output Voltage (V) | 12 |
| Low Buck Output Current (A) | 15 |
| Load Regulation (%) | 0.5 |
| Max Start-up Current (A) | 10 |
| Output Ripple (%) | $\pm 1$ |
| Power Factor | 0.85 |
| Efficiency (%) | 85 |

## 3.3 General Design Considerations

### 3.3.1 Switching Frequency

The selection of switching frequency is a careful balance between size of the components and switching losses. Since the critical inductance is inversely proportional to the switching frequency; the increased frequency would allow a smaller inductance to meet the circuitry requirements. This relationship is shown in (1). A smaller critical inductance values signifies that the inductor is physically smaller, which would allows the product to become more compact. But the increase in frequency would cause an increased system loss.

$$v = L\frac{\Delta i}{DT} \tag{1}$$

Through research and personal experience, a switching frequency of 100 kHz was selected for the flyback converter and 300kHz was selected for the low and high power buck converters. These frequencies provide balance between the properties that affect the circuit.

### 3.3.2 Snubber Circuit

A snubber circuit is key for the flyback topology. The flyback MOSFET is in series with the primary coupled inductor coil. During turn-off state, the MOSFET must counter the inductor's tendency to keep current flowing. This results in a large voltage build up across the MOSFET, which can lead to overheating and damage. The parasitic effects in the transformer and the switch determine the magnitude of the voltage spike [6].

The purpose of the snubber circuit is to absorb the extra current during a turn-off transient. It is also used to prevent excessive ringing [4, 5]. In a traditional Resistor Capacitor Diode (RCD) snubber, the energy from the extra current is stored in a capacitor. During the turn on time, the capacitor is discharged across the resistor. This leads to additional loss in the system but the MOSFET is protected from damage. The capacitor is chosen to have a small equivalent series resistor (ESR) value to handle the high peak currents.

### 3.3.3 Thermal Effects

Thermal effects must be taken into account throughout the project. A thermal analysis will be done on the MOSFETs, diodes, and buck converter ICs to assess the need for heat dissipation. Various temperature

measurements will be taken with in-lab equipment at different load levels.

### 3.3.4 Capacitors

The capacitor selection process is critical for the design of the control schemes. There are several types of capacitors; the main three options were ceramic, tantalum, and electrolytic.

The first type explored was the ceramic capacitor. The physical size of the component is small which fits the size constraint of the standard wall outlet housing. This type of capacitor also has excellent high frequency characteristics and has a linear capacitance change with operating temperature. One of the drawbacks is that the capacitance changes with applied voltage. Another drawback is the degrading of ceramic material over time. The strengths of ceramic capacitors are low cost, low ESR, and low power loss.

Then next type of capacitor examined was tantalum. They are small in size and have a wide range of operating temperatures. Tantalum capacitors have long operating life and constant capacitance despite voltage changes. The disadvantages of this capacitor type are higher cost and limited voltage range. Tantalum capacitors also have the potential of exploding when the voltage or current rating is exceeded or when the polarity of the applied voltage is reversed.

The final type of capacitor researched was electrolytic. These capacitors have a large capacitance to volume ratio and they smooth voltage ripple. Electrolytic capacitors have a large ESR and equivalent series inductance (ESL) which limit the potential of high frequency operation. They also have poor low temperature stability and loose tolerances. Similar to tantalum capacitors, they can burst when overloaded or overheated or if the applied voltage is exceeded [1].

After comparing the benefits and drawbacks of each type of capacitor, the ceramic type was the clear selection choice. With the capacitor type determined, the different ceramic dielectric material options need to be address. From previous experience and data sheet recommendation, the XR7 was selected. The XR7 contains the properties of -55°C minimum temperature , 125°C maximum temperature, and ±15% capacitor value tolerance [3]. These properties correspond well with the circuit requirements.

## 3.4 Rectifier

The first stage of the topology is an H-Bridge rectifier to convert the input ac power to dc. There are several configuration options for the H-Bridge rectifier: such as using four diodes, four Schottky diodes, a bridge rectifier chip, or four MOSFETs.

Table 2: Comparison of Rectifier Component Options

| Component | Voltage Drop (V) | Power Loss (W) | Percent of Total Power (%) |
|---|---|---|---|
| Diode | 1 | 15 | 3 |
| Schottky Diode | 0.4 | 6 | 1.2 |
| H-Bridge Rectifier Chip | 0.5 | 7.5 | 1.5 |
| MOSFET with $R_{DS(on)}$ of 0.038 Ω | 0.57 | 8.55 | 1.7 |

Table 2 shows the characteristics of each configuration option under consideration during the design process. Even though the design with the MOSFETs contained the lowest amount of power loss; it required additional control circuitry which increased the complexity of the design. The power savings did not outweigh the additional control complexity. The final component chosen was the H-Bridge chip because it's implementation was simple and it has low power loss. The H-Bridge also cost less than the other configuration options; it can lower the overall cost and make the final product more marketable.

### 3.4.1 Power Ratings

Voltage Rating:

$$V_{pk} = \sqrt{2} * V_{rms} = \sqrt{2} * 120 = 169.7V \quad (2)$$

$$V_{DC} = \frac{2 * V_{pk}}{\pi} = 108V \tag{3}$$

$$V_{diode}(max) = 170 - 108 = 62V \tag{4}$$

Current Rating: 15A

## 3.5 Flyback Converter

### 3.5.1 Challenges

A design challenge for a flyback is the ringing noised caused by operating the MOSFET at high frequency. The solution to this was to incorporate a snubber circuit into the design topology. For more details on the snubber circuit refer to Section 3.3.2. Another challenge was to balance the operation frequency with the inductor component size and system loss. Operating the circuit at higher frequency would lower the inductance and the size of the inductor. The higher frequency would also increase the system losses that are caused by the switching components.

### 3.5.2 Operation Mode

The flyback converter can be run in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). To avoid saturation, the converter has been designed to operate in DCM mode. The DCM mode design also requires a smaller inductor.

### 3.5.3 Coupled Inductor Design

When designing the coupled inductor there are several considerations that need to be taken into account, such as the core size, air gap length, and conductor type. The following calculations demonstrate the process used to choose the inductor core that is necessary for the flyback converter.

The size of the air gap was the first design criteria under consideration because it effected the inductor performance. An air gap in the inductor core could improve its performance and make it more accurate. From the relationship of (5), it shows that as the air gap increases the reluctance increase, this is shown from the relationship of (5). But the increased reluctance would decrease the effective permeability; and the permeability is inversely proportional to the saturation limit. Therefore the increased air gap would prevent the core from reaching saturation. The increased reluctance also causes both the inductance and power storage per unit volume to decrease. This correlation is revealed through the equation given in (6), (10), (11). After careful consideration, a core with an air gap was selected to increase the inductance and power storage per unit volume.

$$\mathbb{R} = \frac{g}{\mu A_e} \tag{5}$$

$$W = \frac{1}{2} L i^2 \tag{6}$$

The given properties for the inductor calculation are provided in Table (3).

Table 3: Constant Values for Inductor Design

| Description | Symbol | Value | Units |
|---|---|---|---|
| Frequency | f | 100 | kHz |
| Duty Ratio | D | 50 | % |
| Input Voltage | $V_{in}$ | 108 | V |
| Output Voltage | $V_{out}$ | 25 | V |
| Input Current | $I_{in}$ | 3 | A |
| Output Current | $I_{out}$ | 10 | A |
| Permeability of Free Space | $\mu_0$ | $4\pi * 10^{-7}$ | H/m |

The following calculation is for one of the cores under consideration for the inductor design. From the data sheet of 36/22 FerroxCube core [2], the core characteristics is displayed in Table 4 below.

Table 4: Core Characteristics

| Description | Symbol | Value | Units |
|---|---|---|---|
| Core Material | - | Ferrite | - |
| Core Size | - | 36/22 | - |
| Magnetic Field Saturation | $B_{sat}$ | 0.3 | T |
| Effective permeability | $\mu_e$ | 66 | - |
| Effective length | $l_e$ | 0.0532 | m |
| Effective Area | $A_e$ | 0.000202 | $m^2$ |
| Inductance/turn | $A_l$ | $3.15 * 10^{-7}$ | H/turn |

With the core characteristics and the given values, the number of turns, permeability, reluctance, and inductance for the coupled inductor were calculated from the following equations; the values are shown in Table 5.

$$\mu = \mu_e * \mu_o \tag{7}$$

$$\mathbb{R} = \frac{l_e}{\mu A_e} \tag{8}$$

$$\frac{N_1}{N_2} = \frac{108}{25} \tag{9}$$

$$L_1 = \frac{N_1^2}{\mathbb{R}} \tag{10}$$

$$L_2 = \frac{N_2^2}{\mathbb{R}} \tag{11}$$

Core permeability was found using (7). With the computed permeability value, the core reluctance was determined by (8). The turns ratios also needed to be established before computing the inductance values. The secondary number of turns were assumed to be 10 turns. With the value of $N_2$ and (9), the primary number of turns was calculated to be 44 turns. After the turn ratio was determined, the primary and secondary inductance can be computed with (10) and (11).

Table 5: Sample Calculated Coupled Inductor Values

| Description | Symbol | Value | Units |
|---|---|---|---|
| Primary Turns | $N_1$ | 44 | turns |
| Secondary Turns | $N_2$ | 10 | turns |
| Core Permeability | $\mu$ | $8.29 * 10^{-5}$ | H/m |
| Core Reluctance | $\mathbb{R}$ | $3.17 * 10^{6}$ | 1/H |
| Primary Inductance | $L_1$ | $6.09 * 10^{-4}$ | H |
| Secondary Inductance | $L_2$ | $3.14 * 10^{-5}$ | H |

In addition to the calculation process, the calculated values need to be tested to determine whether the core met the requirements. There were three different test calculations done for each core under consideration. The first test was for energy balance which used the correlation of (12). Then with relationship provided in (13), the amp-turns was examined. Also the Volt-sec rating test is performed on core by utilizing (14).

$$\frac{1}{2}V_{in}I_{in}T \quad < \quad \frac{1}{2}L * I_{in}^2 \tag{12}$$

$$N_1 I_{in} \quad < \quad B_{sat}A_e\mathbb{R} \tag{13}$$

$$V_{dc}DT \quad < \quad B_{sat}N_1 A_e \tag{14}$$

The calculation and testing process was done for multiple core sizes to find the most suitable core for the design topology. All inductor calculations performed can be reviewed in Appendix A.

#### 3.5.4 Output Capacitance

A capacitor is added to the output of the flyback converter. It acts as a filter to maintain a ripple of 1%. One of the requirements that this capacitor needs is a low ESR because a high ESR would add losses to the system.

$$C \quad = \quad I_{out}\frac{D}{f * V_{ripple}} \tag{15}$$

(15) shows the relationship governing the capacitor value of a flyback converter. The calculated minimum value for the output capacitor given the design specifications is 200 $\mu F$.

#### 3.5.5 Power Factor Correction Control/Harmonics

One of the design goals for the project is to achieve a high power factor. Power factor is a ratio of the real power flow to the total complex power. The indirect goal of achieving a high power factor is to reduce the reactive power to zero. Reactive power is power that flows between the load and source without being consumed [9]. Reactive components such as capacitors and inductors store energy and then lose it throughout the switching states. Sources that draw reactive power still require real current to flow on power lines [8]. This forces utilities to increase line size for current that does no real work.

Minimizing the reactive power draw and maximizing power factor is a growing concern. In 2001 the European Union signed the IEC/EN61000-3-2 proposal into law [10]. This law requires that all equipment above 75 W limit input AC harmonics up to the 40th and implement power factor correcting pre-stages. This project will use a power factor correcting IC which meets the IEC1000−3−2 harmonic reduction requirements.

#### 3.5.6 Gate Driver

The power factor correction IC will send a switching signal through a gate driver to the MOSFET. The gate driver is needed for two reasons. The first reason is to provide isolation between the grounded PFC chip and the MOSFET gate. The source of the MOSFET will not be at ground, thus a low side gate driver would not work.

The second reason is to supply the current needed to charge the gate capacitance of the MOSFET. The MOSFET gate current can be considerable, see [7], and must be supported by a dedicated gate driver.

### 3.6 Buck Converter Stages

#### 3.6.1 Benefits

The final stage of AC/DC conversion happens in one of two buck converters. A buck converter is a DC/DC step-down converter, in this circuit the voltages are stepped down from a 25V DC bus supplied by the flyback to either 5 V or 12 V DC. Each buck was built using a different approach, the low power buck utilizes an IC

chip in order to maintain efficiency, while the high power buck uses discrete components that can be sized to handle the voltage and current.

At first linear regulators were considered; these are simple devices that reduce Voltage by dissipating energy. Linear regulators are simply voltage dividers that continuously adjust a variable resistor in order to maintain the desired output. But buck converters are more efficient than linear regulators and offer efficient line regulation. In a buck converter, the output voltage is maintained by changing the switching function instead of a variable resistor. The switch in a buck converter is ideally a loss-less component, and thus maintains the efficiency.

A buck converter has two stages, an on stage and an off stage as shown in Figure 3. During the on stage, the switch, usually a MOSFET, is closed; the current flows into the inductor; and the diode is in reverse bias which acts as an open switch. The current from the input charges the inductor and capacitor. When the MOSFET opens, the diode acts as a closed switch and provides a path for the current to flow through. So the stored energy in the inductor and capacitor maintain the output voltage.

Both buck converters used voltage mode control in order to regulate the output voltage. Voltage mode control senses the change in output voltage and corrects the switching frequency accordingly to maintain the desired output. This type of control can be defined as "cause and then react"[17]. Therefore the voltage mode control is slower than current mode control, however, for a power application the slower speed is offset by the simplicity of implementation as well as the increased noise tolerance.

Buck converters are simple in design and can be modified to handle any input voltage and output voltage. Their input/output relation, (16), can be changed to provide a constant output as long as the input voltage remains higher. The size of a buck converter is dependent on the voltage and current ratings of its components and the switching frequency.

### 3.6.2 Challenges

The design of a buck converter depends on three main factors, input voltage, output voltage, and switching frequency. The input and output voltages determine the power ratings for the components. The switching frequency determines the physical size of the inductor and capacitor. The switching frequency posed a design challenge in balancing switching losses, explained above, and the size of the components. The project design is centered around being small and its ability to fit into a standard wall outlet, so a large switching frequency is favored. Efficiency is also a major design criteria for the project, and favors a lower switching frequency. The selected switching frequency was chosen with these two factors in mind.

The buck converters are the final stages in the circuit and are responsible for the quality of the output voltage. The amount of voltage ripple was taken into account when the capacitance of the buck converters was determined. A small capacitance has a large voltage ripple at the output, but saves space. A large capacitance reduces the output voltage ripple, but consumes a larger space.

### 3.6.3 Buck Converter Topology

Both low and high power buck converter topologies are derived from the circuit shown in Figure 3. For a clearer visual of the switching operation the MOSFET is displayed as a ideal switch. As mentioned before the buck converter has two stages: on stage and off stage. During the on stage the MOSFET is on and the diode is in reverse bias, which allows current to flow in to and store energy in the inductor. Then during the off stage the diode is in forward bias mode and the MOSFET is off. This allows the stored energy in the inductor and capacitor to maintain the output voltage.

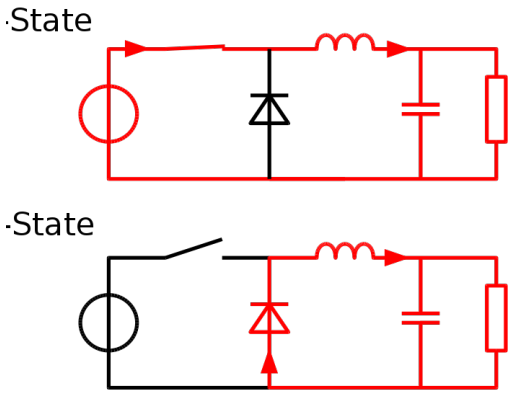


Figure 3: Buck Converter (Top) On State (Bottom) Off State [18]

From Figure 3, (16) to (20) was derived. With these equations, the component ratings can be computed.

$$D_1 * V_{in} = V_{out} \tag{16}$$

$$V_{diode} = V_{in} \tag{17}$$

$$I_{diode} = (1 - D_1) * I_{out} \tag{18}$$

$$V_{mosfet} = V_{in} \tag{19}$$

$$I_{mosfet} = D_1 I_{out} \tag{20}$$

Since the functionality of each converter is different, the rating of the components will also vary. More details are provided in 3.6.4 and 3.6.5.

### 3.6.4 Low Power Buck

The low power buck is implemented using an IC chip. This chip must meet all required voltage and current ratings as the discrete components. With (16) to (20) the rating for discrete components is calculated and the values are displayed in Table (6). Through research the TPS5450 was found to be able to handle current and voltage ratings safely. The TPS5450 includes the MOSFET and controls for linear regulation. Along with the TPS5450, there is an external diode, capacitor and inductor for the low power buck converter.

Table 6: Low Power Buck Ratings

| $D_1$ | $V_d$ (V) | $I_d$ (A) | $V_{fet}$ (V) | $I_{fet}$ (A) | $I_o$ (A) | $V_o$ (V) | $I_i$ (A) | $V_i$ (V) | $I_{chip}$ (A) | $V_{chip}$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|
| .2 | 25 | 4 | 25 | 1 | 5 | 5 | 1 | 25 | 6 | 36 |

### 3.6.5 High Power Buck

Unlike the low power buck converter, the high power buck converter will be build using discrete components and a controller. This allows the components to be selected based on individual calculated ratings. With (19) and (20), the high power buck MOSFET ratings can be determine and the values are included in Table 7. The high power buck diode ratings can be calculated from (17) and (18), values shown in Table 7. Along with the calculated ratings for the high power buck converter, the selected component ratings are also listed in Table 7. In order to protect the circuit against noise and ripple that occurs in non-ideal components, the select components have higher ratings than calculated. Over-sizing the components also helps improve the

reliability of the circuit. The high power buck converter will be realized using a buck controller IC. This approach was chosen in order to handle the current requirements.

Table 7: High Power Buck Ratings

| | $D_1$ | $V_d$ (V) | $I_d$ (A) | $V_{fet}$ (V) | $I_{fet}$ (A) | $I_o$ (A) | $V_o$ (V) | $I_i$ (A) | $V_i$ (V) |
|---|---|---|---|---|---|---|---|---|---|
| Theoretical Ratings | .48 | 25 | 7.8 | 25 | 7.2 | 15 | 12 | 7.2 | 25 |
| Actual Component Ratings | - | 30 | 10 | 40 | 15 | - | - | - | - |

## 3.7 Losses

The MOSFET loss calculations

$$P_l = P_c + P_{sw} + P_b \tag{21}$$

$P_l$: total MOSFET power losses, $P_c$: on-state conduction losses, $P_{sw}$: switching losses, $P_b$: body diode blocking losses

**Conduction Losses**

$$P_c = R_{DSon} * I^2_{D(rms)} \tag{22}$$

$R_{DSon}$: On-state drain source resistance, $I_{D(rms)}$: Rms drain current

**Switching Losses**

$$P_{sw} = \frac{V_r I_r}{2} t_r f_{sw} + \frac{V_f I_f}{2} t_f f_{sw} \tag{23}$$

$P_{sw}$: MOSFET switching power losses, $V_r$: voltage across the MOSFET during switch on, $I_{out}$: current through the MOSFET during switch on, $t_r$: rise time, $f_{sw}$: switching frequency, $V_f$: voltage across the MOSFET during switch off, $I_f$: current through the MOSFET during switch off, $t_r$: fall time

## 3.8 Design Changes

The project has evolved through the design process. After discussing the project with colleagues feedback has been incorporated to improve usability, performance, and other concerns.

To increase efficiency and scalability buck converter ICs will be used. The team was unaware of the existence of such ICs before the beginning of the project. Some of the team members have experience building converters from discrete components, but building a converter from and IC will be a new experience. The team is excited about exploring this new technology.

The control scheme has undergone several design iterations. The original design called for a micro controller, an MSP430 to be exact. After considering the needed capabilities and complexity a simpler Pulse Width Modulation (PWM) controller was chosen. This controller was smaller, easier to use, and was made specifically for this job. The next design change occurred when the team discovered PFC controllers. One of the design goals is to achieve a high power factor. After online research of the capabilities of PFC controllers, the control scheme was modified to include one.

The original design called for two types of USB output. After receiving confused feedback from some friends the team decided to change the high powered outlet to a different standard. The USB standard is meant for lower power applications and people could not see running an appliance using this type of connector. The new connector will be more secure and able to handle the power levels more safely.

# 4 Simulations

Figure 4 below shows the schematic of the simulation. A rectifier, flyback converter with a turns ratio, and two buck converters are realized. All components are modeled with realistic parasitics such as on-state losses and magnetizing inductance.

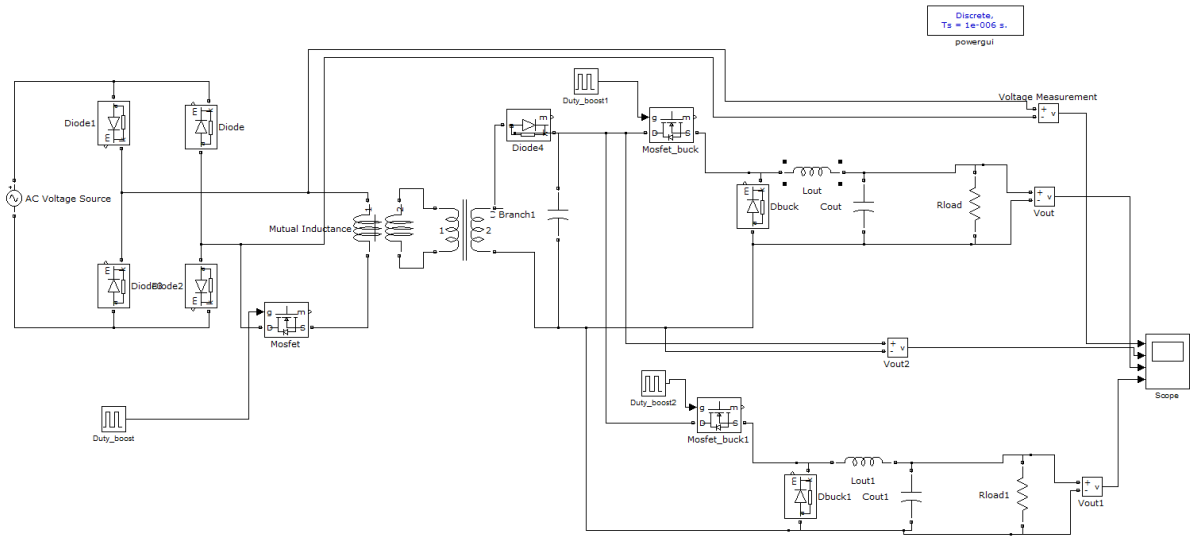


Figure 4: Simulation Schematic

## 4.1 Simulation Results

Figure 5 below shows the simulation results. Axis one shows the output of the rectifier bridge. The peak is 169 V and the frequency is 60 Hz. Axis two displays the output of the flyback converter with an output capacitance of 10 mF. This is still a large capacitance and will require more design thought. Axis three displays the output of the high power buck converter with a duty ratio of 82%. This is well within the achievable range for duty ratio. Axis four shows the output of the low power buck converter with a duty ratio of 25%.

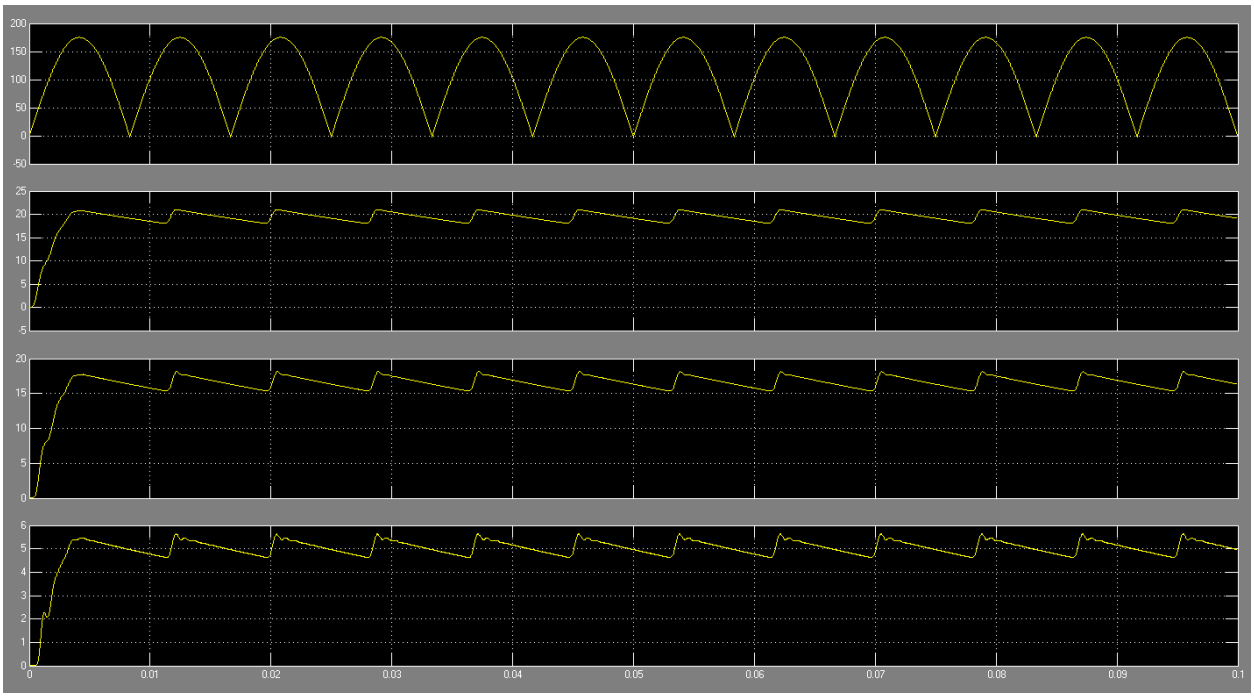


Figure 5: Simulation Results

The simulation exercise were used to confirm rough estimates of our design values. Moving forward the design will be optimized through lab testing.

# 5 Verification

## 5.1 Testing Procedures

Prerequisite: The circuit need to be build in modules. Each module need to be tested individually.

Load regulation defined in (24).

$$\%Load\ Regulation \quad = \quad \frac{V_{out(minload)} - V_{out(fullload)}}{V_{out(nom)}} \tag{24}$$

See Appendix D for Testing and Verification Procedures Table.

## 5.2 Tolerance Analysis

The functionality of the circuitry is dependent on the switching frequency of the flyback converter. The switching frequency is also inversely proportion to the size of the inductor in the flyback circuit. If the frequency is too small, the inductor will saturate and act as a short circuit. If the frequency is too large, the losses due to heat will increase dramatically. The current components are selected to function at the nominal switching frequency of 100 kHz. In order to analyze the system responsiveness, the frequency will be varied from 10 Hz to 1 MHz.

In addition to the frequency tolerance analysis, the gate drive circuitry will contain various pot resistors to determine the output current to gain optimal control of the MOSFET for the flyback converter. The initial stage of the gate driver circuit will be based on the information given on the data sheet. Afterward, a potentiometer will be used to determine the optimal response from the driver.

# 6 Cost and Schedule

## 6.1 Labor

Table 8: Labor Cost

| Name | Rate | Hour | Total = Rate * Hour * 2.5 |
|---|---|---|---|
| Cindy Fok | $50/hr | 180 | $22,500 |
| Andrew Moruzi | $50/hr | 180 | $22,500 |
| Tyler Neyens | $50/hr | 180 | $22,500 |
| | | Total | $67,500 |

## 6.2 Bill of Materials

See Appendix B for a complete list of materials.

**Total Project Cost** = $67,600 + $56.71 = $ 67,656.71

## 6.3 Schedule

| Week | Description of Task | Group Member |
|---|---|---|
| 1/16 | **Initial Posts** | **Class Dates** |
| | Find partner and brainstorm ideas | Cindy Fok |
| | Find partner and brainstorm ideas | Andrew Moruzi |
| | Find partner and brainstorm ideas | Tyler Neyens |
| 1/23 | **None** | **Class Dates** |
| | Email Prof. Carney about addition to project | Cindy Fok |
| | Topology research | Andrew Moruzi |
| | Initial simulations | Tyler Neyens |
| 1/30 | **RFA Due, Project Page Update, Schedule Submitted** | **Class Dates** |
| | Research section/design, Learn USB | Cindy Fok |
| | Power ratings, proposal | Andrew Moruzi |
| | Inductor calculation, part selection | Tyler Neyens |
| 2/6 | **Proposals Due, TA Meeting** | **Class Dates** |
| | Rectifier, Finalize BOM, Cont. USB/connectors | Cindy Fok |
| | Start Flyback on breadboard, Gate drivers | Andrew Moruzi |
| | Final simulation, Start Design Review | Tyler Neyens |
| 2/13 | **TA Meeting** | **Class Dates** |
| | Design Review final, Controls | Cindy Fok |
| | PCB Schematic Design | Andrew Moruzi |
| | Finish Flyback, Start Buck on Breadboard, Gate drivers | Tyler Neyens |
| 2/20 | **Design Reviews, TA Meeting** | **Class Dates** |
| | Finish Buck on Breadboard | Cindy Fok |
| | Eagle Part Design/Library | Andrew Moruzi |
| | Final Breadboard Testing | Tyler Neyens |
| 2/27 | **TA Meeting** | **Class Dates** |
| | Order PCB 1.0 from 4PCB | Cindy Fok |
| | Start SC Protection | Andrew Moruzi |
| | Finalize PCB Board Layout | Tyler Neyens |
| 3/5 | **TA Meeting** | **Class Dates** |
| | IPR, Finish SC Protection | Cindy Fok |
| | IPR, Start up power | Andrew Moruzi |
| | IPR, Test SC Protection | Tyler Neyens |

| | | |
|---|---|---|
| 3/12 | **Individual Progress Reports, TA Meeting** | **Class Dates** |
| | Order PCB 2.0 from 4PCB | Cindy Fok |
| | Test PCB 1.0 | Andrew Moruzi |
| | Finalize PCB 2.0, Test Start up power | Tyler Neyens |
| 3/19 | **Spring Break** | **Class Dates** |
| 3/26 | **Mock-up Demos, TA Meeting** | **Class Dates** |
| | Control slides | Cindy Fok |
| | Test slides | Andrew Moruzi |
| | Design slides | Tyler Neyens |
| 4/2 | **Mock-up Presentations, TA Meeting** | **Class Dates** |
| | Modify USB cord | Cindy Fok |
| | Circuit Housing | Andrew Moruzi |
| | Custom Load | Tyler Neyens |
| 4/9 | **Last Day for Final PCB, TA Meeting** | **Class Dates** |
| | Presentation | Cindy Fok |
| | Load | Andrew Moruzi |
| | Demo | Tyler Neyens |
| 4/16 | **Demo and Presentation Sign-up Closes, TA Meeting** | **Class Dates** |
| | Final Paper - Intro, cost, conclusion | Cindy Fok |
| | Final Paper - design procedure, details | Andrew Moruzi |
| | Final Paper- testing, verification | Tyler Neyens |
| 4/23 | **Demos, Presentations, TA Meeting** | **Class Dates** |
| | Final Paper Review - Intro, cost, conclusion | Cindy Fok |
| | Final Paper Review - design procedure, details | Andrew Moruzi |
| | Final Paper Review - testing, verification | Tyler Neyens |
| 4/30 | **Presentations, Final Paper, Checkout, Lab Notebooks** | **Class Dates** |

# 7 Ethical Considerations

The main ethical issue of the USB 3.0 Outlet is user safety; which correlates with IEEE Code of Ethics #9: "to avoid injuring others, their property, reputation, or employment by false or malicious action" [14]. As a consumer product there are several safety concerns associated with a power outlet. Therefore the goal is to developed the safest product possible to ensure user safety. To accomplish this, there is a need for short circuit protection. This would avoid damage to the equipment and act as a protection precaution for the user. Along with the short circuit, it is necessary to design a high power safe connector to create a more durable product. This connector would allow the user to disconnect from the outlet abruptly or harshly without damaging the internal circuit or harming the user.

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# Appendix A

Coupled Inductance Design Calculations

# Appendix B

Complete List of Bill of Material

# Appendix C

Data Sheet Schematics

# Appendix D

Testing and Verification Table