ECE 445: Senior Design Laboratory

M.E.L.O.D.I.C Design Document

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1 Introduction

1.1 Problem

A common problem associated with live performing is the 'rat's nest' of audio and control cables required to run front-of-house (FOH) equipment, digital effects, and instruments. However, in recent times UHF, VHF, and ISM systems have taken mainstay in the industry. For a large performance, having a $10,000+ rack dedicated to wireless audio systems makes sense. However, for the performing musician on a budget, such as a small house band or coffee shop artist, professional UHF, VHF, and ISM systems are not feasible to operate. Although low-cost or used legacy systems are popular amongst amateur musicians, they often suffer from problems such as data packet collisions from co-existing network protocols, interference from existing UHF and VHF television bands, and/or lack of scalability or configurability.

1.2 Solution

In order to combat this, we are developing M.E.L.O.D.I.C., a low-cost, scalable, configurable, and high-fidelity wireless audio link compatible with commonly used audio equipment in the live audio industry. We intend to use a commercial off-the-shelf Radio Frequency System-on-Chip (RF SOC), specifically the TI CC8531, commonly found in wireless headphones and karaoke systems. This chip is an attractive choice due to its operation in the ISM band, use of adaptive frequency hopping techniques for co-existence with other ISM devices, and configurable to either be an audio transmitter or receiver. Due to the configurability and low cost of the chip, our transmitter and receiver will have very similar circuit schematics, which will make it cheaper to manufacture multiple sets of transmitter and receivers.

1.3 High-level Requirements

- The system must transmit audio that meets or exceeds lossless CD audio standards, with a specific sampling rate of 44.1 kHz and a bit depth of 16 bits. This ensures high-fidelity sound reproduction suitable for professional live performance contexts.

- The system must co-exist with other 2.4 GHz wireless protocols (such as Wi-Fi and Bluetooth) without causing or suffering from interference that degrades performance. This will be quantitatively measured by maintaining a packet error rate (PER) below 1% in environments populated with at least three active 2.4 GHz sources.

- The device must feature a human-friendly user interface, equipped with an LCD that displays essential information including but not limited to battery status (with at least 10% granularity), network statistics (such as signal strength and PER), and unique device identification. This information must be easily readable under typical indoor lighting conditions from a distance of at least one meter.

2 Design

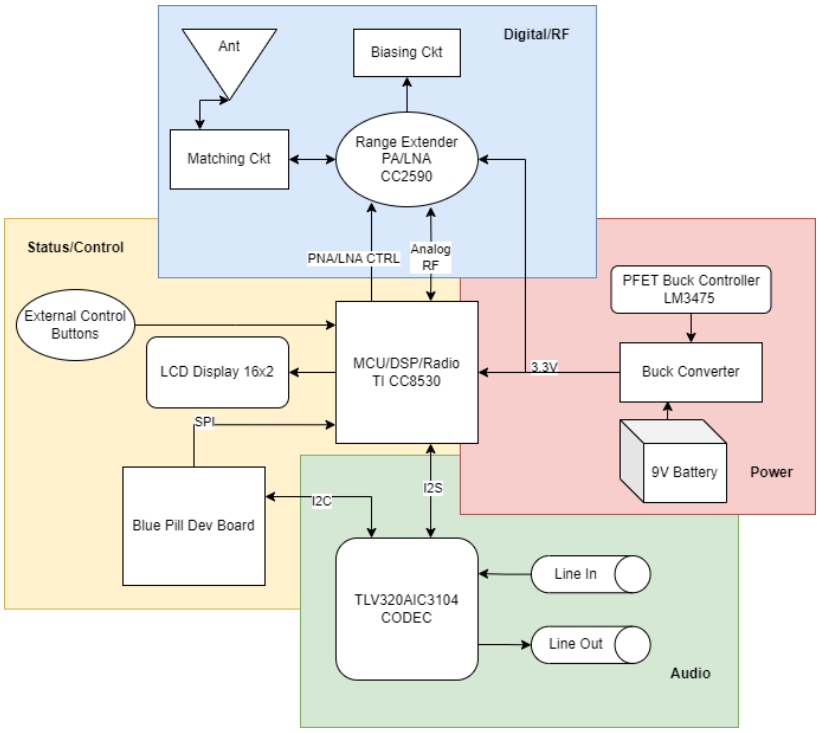

Figure 1: Block Diagram

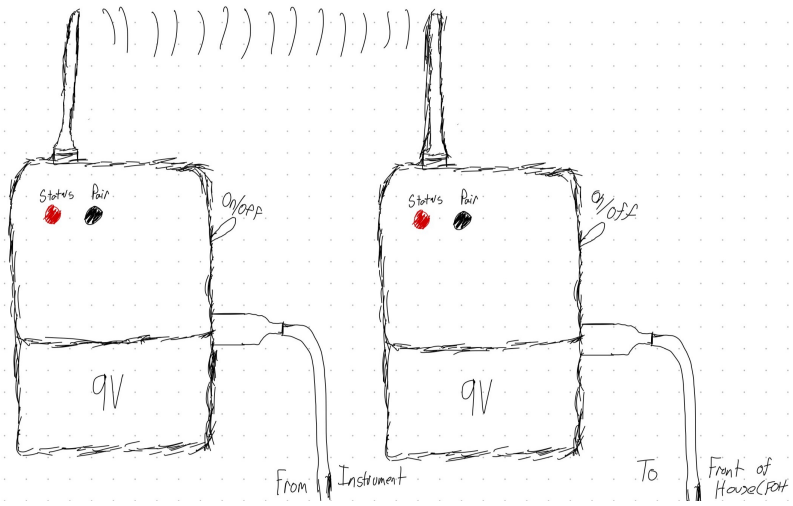

Figure 2: Sketch of M.E.L.O.D.I.C. Device (Initial Concept)

2.1 Status/Control

We will use the STM32F103 microcontroller to program our CC8531 SOC and audio codec. We will also be using this to connect to a display in order to meet our third high-level requirement. We will be operating the CC8531 in host-controlled mode, meaning each configuration must be manually programmed on the CC8531. We will be using the STM32F103C8T6 development board to accomplish this. For our initial prototyping, we will be using a pre-made development board called the "Blue Pill".

Once we have successfully completed a prototype of the device, we will replicate this board using our own design. We plan on using SPI for programming the chip as well as for getting the info for the display. We will use SPI for programming the RF SOC and I2C will be used for programming the display and codec. The reason I2C is used is the fact that we can simply operate on one bus for the codec and display. I2C programming simplifies the required amount of pins to two and with the PCF8574 I2C adapter we can connect the LCD to the STM32F103 over I2C. We will be using an SPI programmer to program the CC8531 and an I2C programmer for the codec. Both of these will be interfaced by the MCU. Note that the SPI wires that aren't connected to either programmer are connected to the CC8531.

The flowchart in 4 shows how the GUI will be implemented. Note that the only interfacing will be done by the use of three buttons: power, enter and scroll. Additionally, two bits are needed to

determine whether the device is a transmitter or receiver for the range extender. This is handled by ENABLE and PAENABLE on the micro-controller.

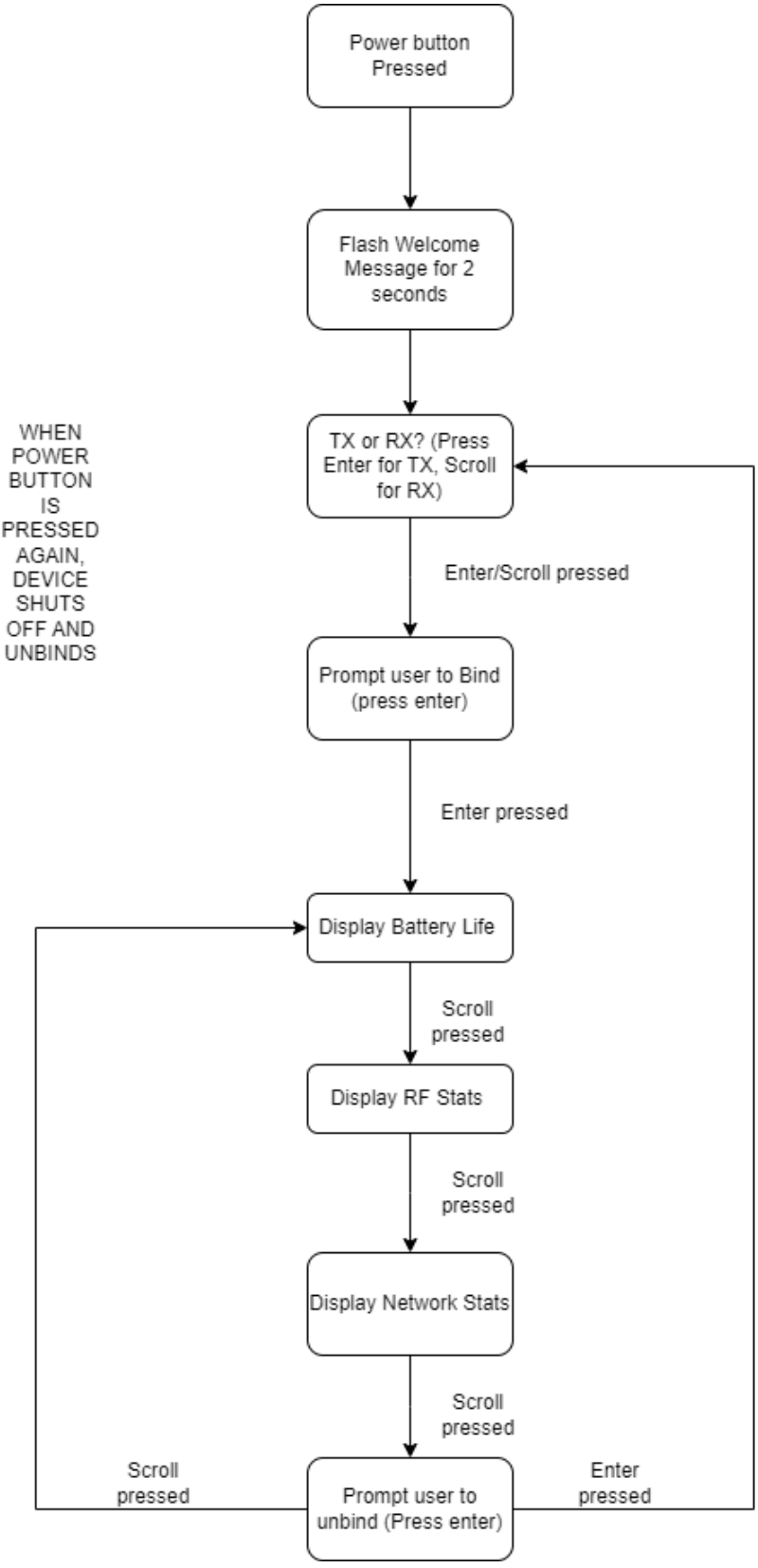

Figure 3: GUI Flowchart

Feature	Verification Actions
Micro-controller successfully programs and controls the codec and digital radio SOC's.	1. Use static code analysis tools to ensure that the micro-controller code is error-free and adheres to coding standards. 2. Develop test cases to verify individual functions of the micro-controller related to codec and digital radio control. 3. Measure and verify the data transfer rate and integrity of communication between the micro-controller and the codec and digital radio SOC using a logic analyzer.
LCD shows all necessary info.	1. Conduct usability tests to ensure all necessary information is displayed clearly and is easily readable. 2. Verify the LCD refresh rate and response time to ensure real-time updates without lag.
Buttons handle GUI navigation in the user interface.	1. Perform end-to-end testing to ensure buttons navigate to the correct screens or perform the correct actions. 2. Test for button durability and responsiveness under various conditions.

Table 1: System Verification Table

2.2 Power

The main power supply for our device will be a 9V battery. This will then be brought down to the 3.3V that the CC8531 RF SoC needs, using a variable duty ratio buck converter. The buck will operate using TI's 10-V hysteretic PFET buck controller, LM3475. This design will enable the system to operate consistently for an extended period, even as the 9V battery's charge diminishes. The LM3475 internally contains noise suppression circuitry but to ensure no noise propagates through the ground plane or interferes in the rest of the circuit we will be implementing external noise-dampening circuitry. In order to counteract noise spikes created by trace parasitic inductances there are several measures that can be taken. Slowing the rise and fall times of the switch can greatly reduce these spikes [1]. This is simply accomplished by placing a small resistor, $R_{PGATE} = 2\Omega$, between the gate and PGATE of the LM3475. In addition to this a small RC snub circuit will be implemented in parallel to the schottky diode to further reduce the noise. The PCB layout the circuit is another critical aspect. Adequate placement needs to be verified to ensure EMI problems and excess switching noise.

Requirement	Verification Method
The buck converter must provide stable 3.3V from the 9V battery.	Tested by voltmeter to ensure voltage stability under various load conditions.
Ripple and noise on 3.3V line must be less than 50 mV p-p.	Use an oscilloscope to measure ripple and noise on the power line.
Power conversion efficiency must be at least 85% under full load.	Measure efficiency under various loads using a power analyzer.
The battery must be able to last a minimum of 5 hours with adequate charge.	Tested by operating the device from a full charge under normal conditions until the battery is depleted, ensuring a minimum operational time of 5 hours.

Table 2: Power Management Verification Table

2.3 Audio

In order for compatibility with standards of the music industry, M.E.L.O.D.I.C will act as a wireless audio cable with line-level inputs and outputs.

We will be using Texas Instruments' TLV320AIC3204 Ultra Low Power Stereo Audio Codec to convert our analog audio into digital audio. This is done through the use of the codec's built-in DAC. The stereo audio DAC provided by the codec supports data rates ranging from 9khz to 198khz [2]. We choose to use PCM-16 at a sampling rate of 44.1 kHz to ensure that we reach the standards of CD-quality audio.

The host, whether it is the CC8531 in autonomous mode or the MCU will configure the needed codec registers for operation. These registers control things such as input bias, audio format, sampling frequency, and power consumption, to name a few. [2] In order to ensure it is configurable and usable with any type of device, we will have 2 different pin-outs for the digital transmission protocols.

- I2C: To configure the codec registers, an I2C protocol is used. (SCL, SDA)
- I2S: To send and recieve the digital audio samples. (MCLK,WCLK,BCLK,DIN,DOUT)

Requirement	Verification Method
Audio output should be CD quality (44.1khz/16-bit)	1.We will measure the frequency of the output using an oscilliscope to make sure it is within our tolerance range (5khz) 2. By Nyquist-Sampling criterion, the analog output should measure about 22.05khz 3. Tolerance was chosen based on average adult perception of 17khz frequency. If it is below this, then quality loss will be noticeable.

Table 3: Audio Verification Table

Requirement	Verification Method
Codec must support 44.1 kHz sampling rate and 16-bit depth.	Verify using technical documentation and testing with signal analyzer for compliance.
Input and output impedance must be 10 kÎ© and 600 Î©, respectively.	Measure impedance using an impedance meter to confirm values.
End-to-end latency must not exceed 20 milliseconds.	Measure latency from input to output using a digital oscilloscope.

Table 4: Audio Subsystem Requirements Verification Table

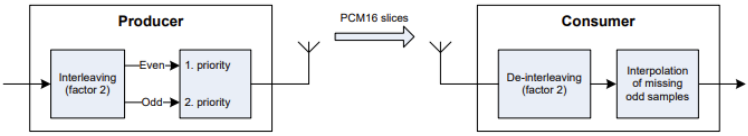

Figure 4: PCM16 Processing Diagram

- Convert line in analog audio into digital audio that can be transmitted by the RF subsystem.
- Convert digital audio provided by the RF subsystem into an analog CD-quality audio stream.

2.4 RF

The RF subsystem mainly comprises of the CC8531RHAT Pure-Path Wireless SOC and the CC2590 BLE range extender. We will connect these components using a differential micro-strip transmission line rated for 2.4 GHz with a 4 MHz bandwidth, utilizing Rogers RO4003C board laminate. [3] The subsystem will be comprised of two smaller sub-sub-systems. The digital back-end, and the analog RF front end.

The digital back-end will feature pin-outs that are designed to mate with the other board

sub-systems through jumper cables. This design choice was made so that the CC8531RHAT can work in autonomous mode, host-controlled mode and in production test mode [3] without needing significant board redesigns for prototyping, characterization and final production of the device. The chosen digital protocols that we will pin-out are:

- I2C: Used for control of the codec when in autonomous operation. The I2C lines will have the internal pull-up resistors required for I2C operation. (SCL, SDA)
- I2S: Used for digital audio transmission between the codec and the RF transceiver. (MCLK, WCLK, BCLK, DIN, DOUT)
- SPI: Used to flash the transceiver when in autonomous operation, configure and read registers when in host-controlled operation, and run included production code in production test. When the device operates in host controlled mode, and additional interrupt request pin is needed to interrupt SPI requests to and from the MCU [3]. (SCK,MOSI,MISO,CSn,IRQ)

The analog front end will feature the needed circuitry to bias the PA/LNA and to match the SMA coaxial port to the impedance of CC2590 BLE range extender. In order to match the antenna to the range extender, we will utilize a T-matching network to ensure that we have maximum power throughput at 2.4GHz for a 4MHz bandwidth matched to 50Ω [4]. We also choose component values to bias the PA to reach +14dBm [4], to ensure we do not exceed the FCC regulations for transmit power. Similar to the digital back-end, we will also utilize two pin-outs for the 2-bit parallel digital control to program the configuration of the internal microwave switch and enable operation of the device [4]. The digital signaling will be recieved via the MCU, similar to the digital front-end.

Feature	**Verification Actions**
AFH successfully negates the effects of frequency dependent interference from co-existing ISM protocols.	1. Setup a single link in an enviroment with other co-existing ISM protocols. 2. Using the PS_RF_STATS register, calculate the ratio between packets failed and packets attempted 3. If the ratio is greater than 25%, then AFH has failed.

Table 5: System Verification Table

Requirement	Verification Method
RF output power configurable up to +10 dBm.	Measure output power across operational range using an RF power meter.

Table 6: RF Subsystem Requirements Verification Table

We will validate these requirements by taking two sets of connected devices and deciding whether or not the RF interference from both co-existing protocols and the M.E.L.O.D.I.C protocol create any perceivable artifacts in audio. We will further quantify the amount of artifacts by capturing and recording the transmitted and received audio samples from both links, and comparing each links transmitted and received samples with each other. If the SNR between transmitting and receiving are greater than 0.5, then we will deem the audio link to suffer from considerable amount of interference and packet collision.

3 Tolerance Analysis

3.1 RF Subsystem

In order for M.E.L.O.D.I.C to solve the issue of frequency dependent interference with FSK, we must use AFH to spread the spectrum to decrease the probability of frequency dependent interference. The AFH technique still uses FSK as the main form of modulation, however, it varies the carrier frequency as function of time as opposed to fixing the carrier frequency to a single channel. Our chosen metric for proving that AFH has successfully decreased frequency dependent interference compared to using FSK is decreasing the probability of interference by a factor of two.

3.1.1 Justification for AFH

Typical systems in the UHF and VHF range utilize M-Ary frequency shift keying or M-FSK to modulate the digital signal in the base-band. Our motivation to use AFH, a subset of FHSS, is the high probability of frequency dependent interference from other devices in the ISM band. Our choice of using the ISM band for this device is solely based on working around FCC licensing for the device, as the ISM band is 'open waters' in the FCC band plan [5].

In order to formulate the devices band-plan, we must find the minimum amount of channels

needed for each stream to hop around the band plan. The Pure-Path Wireless protocol specifies 18 channels over a 4 MHz bandwidth, with each time slot taking up 222.2 KHz of bandwidth. [3].

Within each time-slot, 198 KHz of bandwidth is used for the FSK modulation, with the remaining side-bands around the frequency used as guard frequencies. However, we must specify how many channels we would like available for all time-slots to take up.

3.1.2 Mathematical background of FHSS/AFH and FSK

For our calculation of the minimum amount of channels needed for the band plan, we will consider two different time domain signals using FSK as the form of modulation.

$$x_1(t) = A * Re\{e^{j2\pi f_c t} e^{j2\pi \Delta f_m \int_0^t m(\tau)\, d\tau}\} \tag{1}$$

and

$$x_2(t) = A * Re\{e^{j2\pi f_{hop} t} e^{j2\pi \Delta f_m \int_0^t m(\tau)\, d\tau}\} \tag{2}$$

Where A is the maximum amplitude of the carrier signal, f_m is the max frequency deviation of the frequency modulated message, $m(t)$ is an arbitrary continous message and f_{hop} and f_c is the carrier frequency for the FSK and FHSS signals respectively.

For f_{hop} in equation 4, the relationship between carrier frequency f_c and f_{hop} is

$$f_{hop+1} = (f_{hop} + hop) mod(x) \tag{3}$$

Where *hop* is some psuedo-random sequence and x is the number of total channels we could choose.

Using this intuition, we can formulate a frequency domain simulation of each of these signals and calculate the probability of frequency dependent interference.

3.1.3 Simulation of AFH/FHSS and FSK co-existing with WLAN

Since the AFH algorithm uses extra processing outside of traditional FHSS systems to dynamically change the bands, we will not be modeling true AFH. Instead, we will use FHSS as a place holder to prove that it is better than using just FSK and calculate the minimum amount of channel bands needed to reach our performance metrics.

Using the equations in section 3.1.2, we can quantatively justify that FHSS is better than FSK and empiracally calculate the minimum amount of channels needed to avoid frequency dependent interference by creating a simple MATLAB simulation of the spectra.

For the simulation, we chose f_c and the initial f_{hop} to be centered around the same center frequency of some random WLAN spectra. We set $A = 1$ and $\Delta f_m = 222.222$ KHz for both $x_1(t)$ and $x_2(t)$. In order to calculate the frequency dependent probability given different values of SNR, we treat the WLAN spectra as both artificial noise and another co-existing protocol and increase it for every five sets of FHSS hop in the simulation. This simulation considers SNR to be the ratio between the transmit power of the WLAN spectra and the FSK or FHSS spectra. We set $m(t) = u(t)$ where $u(t)$ is the Heaviside step function. For five steps of f_{hop} within each step of WLAN transmit amplitude, we calculate the frequency dependent interference by taking the $\mathrm{P}(|x_2(t)| < |WLAN|)$ and plotting the average of each probability over the different values of WLAN transmit amplitude. Similarly, for five different instances of FHSS, we calculate the $\mathrm{P}(|x_1(t)| < |WLAN|)$ and plot those values over WLAN transmit amplitude.

In order to figure out how many channels out of the 18 possible channels we should use, we start with one channel and keep adding more channels until we are confident that the probability of interference with FHSS is half that of probability of interference with FSK.

Figure 5 shows the results from the simulation given the amount of channels is six. This result

was the first result where the probability of interference with FHSS is half that of FSK for 20 dB of relative WLAN transmit power. This validates that our simulation is correct, since the device needs a minimum of 6 channel bands to operate properly. [3] Therefore, in order to reach our tolerance of decreasing the probability of interference by a factor of two, we must have at least six channel bands used out of the 18 we could possibly use.

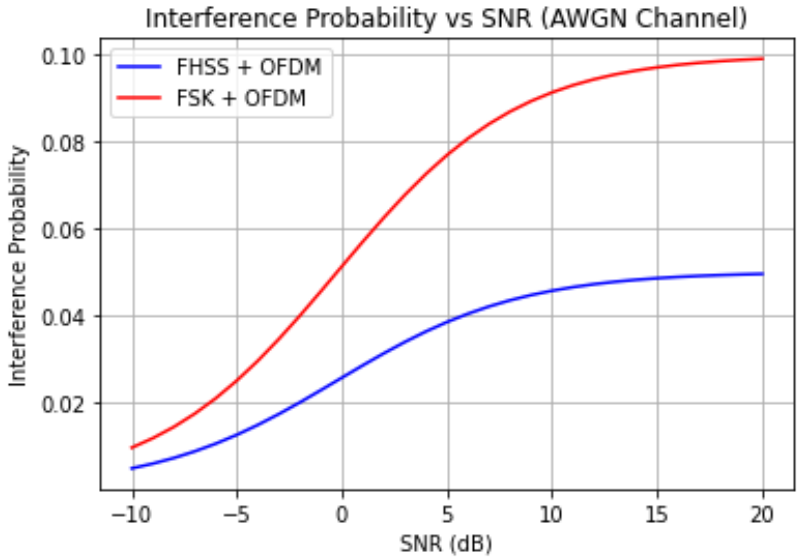

Figure 5: Probability of Frequency Dependent Interference versus SNR

3.2 Power Sub-System

In the design of the buck converter numerous capacitors, resistors, and other components needed to be sized & selected for optimal operation. The LM3475 controller is hysteretic so the frequency isn't set by resistors as in many other controllers but by the internal components of the circuit. Switching Frequency f_{sw} is defined by *eq. 4* [1].

$$f_{sw} = \frac{V_o}{V_i} \cdot \frac{(V_i - V_o) \cdot ESR}{(V_{HYST} \cdot \alpha \cdot L) + (V_i \cdot delay \cdot ESR)} \tag{4}$$

Where α is the feedback resistor relation $\frac{R_1+R_2}{R_2}$, V_{HYST} is the hysteresis voltage given as 21mV [1], delay is the propagation delay (90ns) [1]+ PFET on and off delay (26ns) [6], V_i is the 9V input, & V_o is the 3.3V output. The values of the inductor L and the capacitor ESR must be selected in regard to other criteria. In order to avoid a 90Â° phase shift of the output voltage ripple

and have greater control over the switching frequency a small 1Ω resistor is placed in series with the output capacitor.

Inductor L Selection:

The inductor is sized by its maximum allowable ripple shown in *eq. 5*

$$\Delta i_{Lmax} = I_{out,avg} \cdot 0.3 = 510mA \cdot 0.3 = 153mA \tag{5}$$

This can then be used in a derived equation for the minimum inductance for a buck converter shown in *eq. 6*

$$L \geq \frac{D(1-D)V_i}{f_{sw} \cdot \Delta i_L} \tag{6}$$

One other important factor to consider is the maximum switching frequency calculated in *eq. 7*. [1] Where $t_{off,min}$ is the sum of the blanking time (180ns [1]), propagation delay, and on and off delay of the PFET [6].

$$f_{sw,max} = \frac{(1-D)}{t_{off,min}} = \frac{1-D}{180ns + 90ns + 18ns + 8ns} = 2.16MHz \tag{7}$$

Using this along with eq. 4 & eq. 6 L can be selected. To stay well within the bounds an inductor of $27\mu H$ was chosen which gives a switching frequency of 850kHz.

Output Capacitor C_{out} Selection

The output capacitor is selected on the previously calculated switching frequency as well as the desired output voltage ripple, Δv_c. To minimize output ripple an amply-sized capacitor should be used while keeping the capacitor reasonably small. Using *eq. 8* an output capacitor of 100uF which leads to a 0.22mV ripple.

$$C_{out} \geq \frac{1}{8f_{sw}} \cdot \frac{L}{\Delta v_C} \tag{8}$$

4 Ethics and Safety Considerations

4.1 FCC Regulations

One concern with designing a digital wireless communication system was aligning with FCC regulations and the FCC band plan. If we were to design our system around the same frequencies as existing systems, we would need to license our device to work in that band. Specifically, UHF and VHF equipment used in the live audio industry either have privately licensed bands with the FCC or are licensed around the same bands as terrestrial television [5]. Since we are using an RF SOC specifically made for wireless digital audio streaming, and it has already been tested and approved for use in the ISM band, we do not need to worry about FCC licensing.

4.2 Environmental Concerns

One concern with using a 9V battery is the potential environmental damage that it might cause when it is thrown away. We plan on using Alkaline 9V batteries which are a safer alternative to lithium ion batteries, which are known to have a greater negative impact on the environment when thrown away.

4.3 Safety Concerns

We will ensure that the device itself is safe to use before we demo the project through thorough analysis of the device's power consumption. Mainly, all components (resistors, capacitors, SOCs, etc.) should be within their allowed power consumption tolerance. Most of the devices we are using do not draw a substantial amount of current except for the STM32, which varies based on the programs it is running. We will do thorough electrical analysis to determine how much current the device is drawing when we run the programs.

5 Bill Of Materials

5.1 Labor Costs

Based on the average salary of an ECE graduate from the University of Illinois, we are assuming a wage of $45/hr. We plan on working for 15 hours per week per person. The project design phase

will last for about 10 weeks. Calculating the total labor cost: $45 * 15 * 10 * 3 = \$20250$.

Table 7: Bill of Materials

Component	Part Number	Unit Price ($)	Quantity	Package	Total Cost ($)
		Audio			
Capacitors 10u	C1, C2, C8, C10, C12	0.49	25	0402	12.25
Capacitors 1.0u	C3, C4	0.49	10	0402	4.9
Capacitors 47n	C5, C6	0.49	10	0402	4.9
Capacitor 2.2u	C7	0.49	5	0402	2.45
Capacitor 1u	C9	0.49	5	0402	2.45
Audio Jacks	J2, J3	Free	10	AudioJack3	0
Resistors 100	R1, R2	0.80	10	0402	8.0
Audio Codec	U1	6.29	5	TLV320AIC3204IRHBR	31.45
		RF			
Capacitors 12p	C1, C2	0.49	10	0402	4.9
Capacitor 1u	C3	0.49	5	0402	2.45
Capacitor 1.2p	C4	0.49	5	0402	2.45
Capacitor 6.8p	C5	0.49	5	0402	2.45
Capacitor 1.8p	C6	0.49	5	0402	2.45
Capacitors 2.2u	C7, C8	0.49	10	0402	4.9

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Table 7 – *Continued from previous page*

Component	Part Number	Unit Price ($)	Quantity	Package	Total Cost ($)
Capacitor 220p	C9	0.49	5	0402	2.45
Capacitors 100n	C10-C18	0.49	45	0402	22.05
Capacitors 1n	C19, C22, C23	0.49	15	0402	7.35
Capacitors 18p	C20, C21	0.49	10	0402	4.9
Ferrite Beads	FB1, FB2	0.94	10	Ferrite	9.4
SMA Connector	J1	5.71	5	SMA	28.55
Inductors 2.2n	L1	0.68	5	0402	3.4
Inductor 3.9n	L2	0.68	5	0402	3.4
Inductor 1.5n	L3	0.68	5	0402	3.4
Inductors 6.8n	L4-L8	0.68	25	0402	17.0
Resistor 56k	R1	0.80	5	01005	4.0
Resistors 2.2k	R2, R3	0.80	10	01005	8.0
RF SOC	U1	8.24	5	CC8531RHAT	41.2
Range Extender	U2	3.20	5	CC2590RGVR	16.0
Crystal 48MHz	X1	0.32	5	SMD 0603	1.6
		Power			
Schottky Diode D1	DO-214AC	0.296	10	SMD/SMT	2.96

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Table 7 – *Continued from previous page*

Component	Part Number	Unit Price ($)	Quantity	Package	Total Cost ($)
PFET	SI2343CDS-T1-GE3	0.365	10	SMD/SMT	3.65
Capacitor 100uF	GRM153R61A105ME95D	0.075	10	0402	0.75
Capacitor 22uF	C0402C220J8HACTU	0.1	10	0402	1.0
Capacitor 1uF	80-C0402C105K9PAC	0.016	10	0402	0.16
Capacitor 1nF	CL05B102KB5NFNC	0.013	10	0402	0.13
Resistor 1 Ohm	CRM1206-FW-1R00ELF	0.077	10	SMD/SMT	0.77
Resistor 30 Ohm	ESR10EZPJ300	0.077	10	SMD/SMT	0.77
Resistor 5k Ohm	RT0603BRE075KL	0.094	10	SMD/SMT	0.94
Resistor 1.6k Ohm	ERJ-UP3F1601V	0.082	10	SMD/SMT	0.82
Inductor 27uH	CR54NP-270MC	0.674	10	SMD/SMT	6.74
Buck Controller	LM3475	0.61	10	SMD/SMT	6.1
Battery Clip	546-BS61	2.31	5	THT	11.55
		Control			
Buttons	474-COM-00097	0.35	15	THT	5.25
Switches	R13112ABB	2.56	5	THT	12.80
μC	STM32F103 Blue Pill Dev Boards	6.99	1	THT	6.99
LCD	HY1602E	5.33	2	THT	10.66

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Table 7 – *Continued from previous page*

Component	Part Number	Unit Price ($)	Quantity	Package	Total Cost ($)
LCD I2C Driver	PCF8574	.74	2	SMT	1.48
				Total Cost ($)	**318.26**

6 Schedule

Date	Tasks	Responsible
Week of February 26th	Complete Design Review with Professor Schuh on 2/26	Everyone
	Begin designing PCB and ordering all parts	Everyone
	Research libraries for SPI and I2C programming on the STM32 Microcontroller	Colin
	Research best PCB design choice for RF circuits	Ryan and Macrae
	Meet with Koushik for our weekly team meeting	Everyone
Week of March 4th	Place first PCB order and pass audit	Everyone
	Begin working with Blue Pill development board to get familiar with SPI and I2C programming	Colin and Ryan
	Complete Teamwork Evaluation 1	Everyone
	Meet with Koushik for our weekly team meeting	Everyone
Week of March 11th (Spring Break)	Continue to research SPI and I2C commands and reading all chip datasheets for necessary info	Everyone
Week of March 18th	Work on soldering components of PCB for the power, audio, and RF subsystems	Macrae
	Begin programming the codec and CC8531 using the Blue pill dev board	Colin and Ryan
	Test power system for verification and measure results	Macrae
	Continue to revise PCB design as necessary and place next order	Everyone
	Meet with Koushik for our weekly team meeting	Everyone

Table 8: Schedule

Date	**Tasks**	**Responsible**
Week of March 25th	Verify successful programming of the codec and CC8531 and begin to work on GUI	Colin and Ryan
	Order next round of PCB if necessary, this time including the Blue Pill clone design	Everyone
	Complete Individual Progress Report	Everyone
	Begin drafting final paper	Everyone
Week of April 1st	Work on programming the codec, CC8531, and GUI with the cloned development board	Colin and Ryan
	Order new PCB if necessary	Everyone
	Start testing out design with keyboard and digital audio	Ryan and Macrae
	Continue drafting final paper	Everyone
Week of April 8th	Fully test design and ensure requirements are met	Everyone
	Work on final paper	Everyone
Week of April 15th	Complete Mock Demo with TA	Everyone
	Make any possible changes to the final design as necessary	Everyone
Week of April 22nd	Prepare for final presentation	Everyone
Week of April 29th	Complete Final presentation	Everyone

Table 9: Continuation of the Schedule

References

[1] *LM3475 Hysteretic PFET Buck Controller*, Texas Instruments, Oct. 2015, sNVS239C â October 2004 â Revised October 2015. [Online]. Available: https://www.ti.com/lit/ds/symlink/lm3475.pdf

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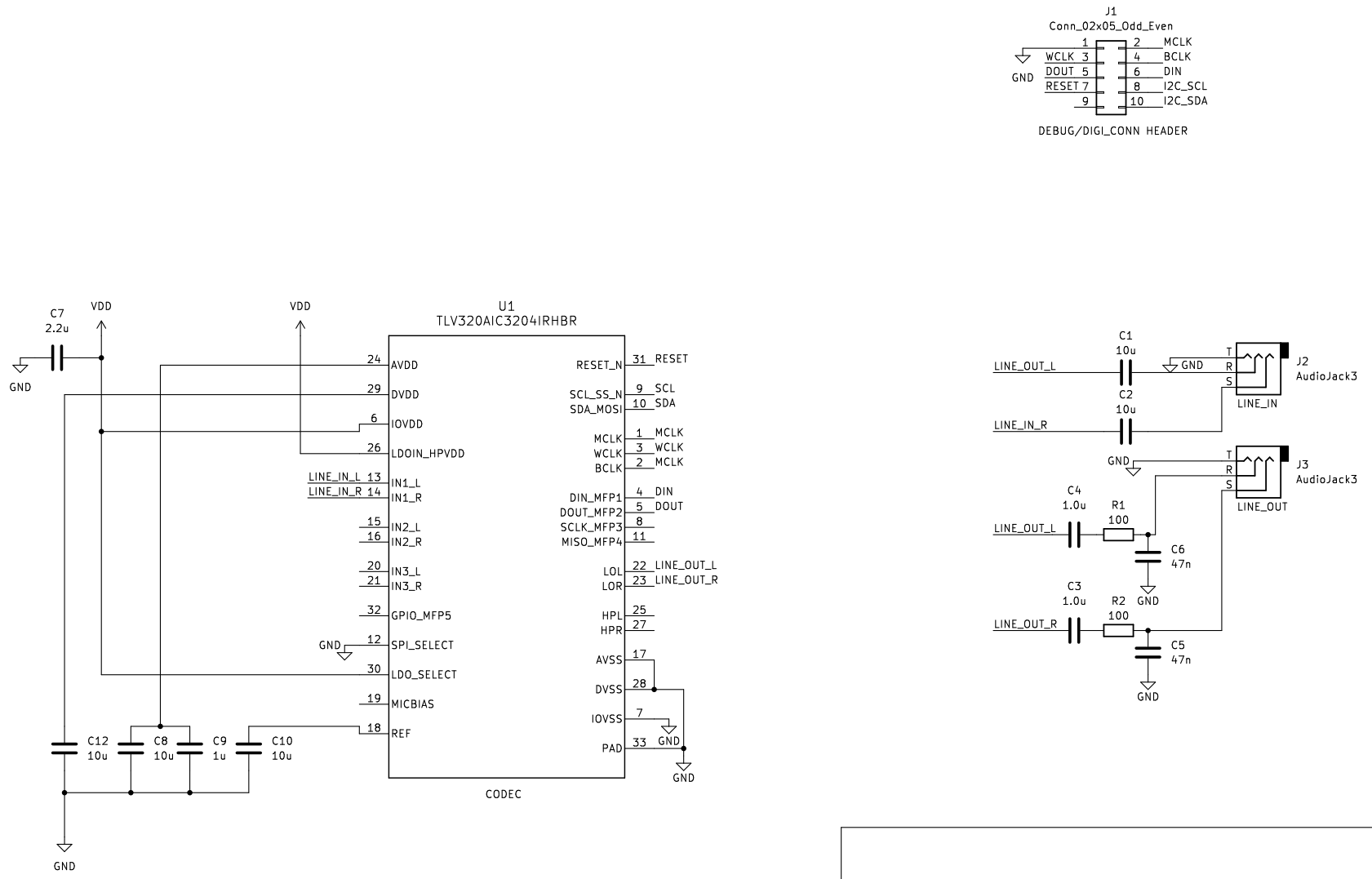
[3] *CC85xx Family User's Guide: RF SoC for Wireless Audio Streaming*, Texas Instruments, 2013, sWRU250M â June 2013, Revised. [Online]. Available: https://www.ti.com/lit/ug/swru250m/swru250m.pdf

[4] *CC2590 2.4 GHz RF Front End*, Texas Instruments, 2008, available: Texas Instruments. [Online]. Available: https://www.ti.com/lit/ds/symlink/cc2590.pdf

[5] Federal Communications Commission, "Title 47 CFR Part 15.247 - Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz," Online, 2013. [Online]. Available: https://www.govinfo.gov/content/pkg/CFR-2013-title47-vol1/pdf/CFR-2013-title47-vol1-sec15-247.pdf

[6] *Si2343CDS P-Channel 30-V (D-S) MOSFET*, Vishay Siliconix, 2009, document Number: 65474, S09-2270-Rev. A, 02-Nov-09. [Online]. Available: https://www.vishay.com/docs/65474/si2343cd.pdf



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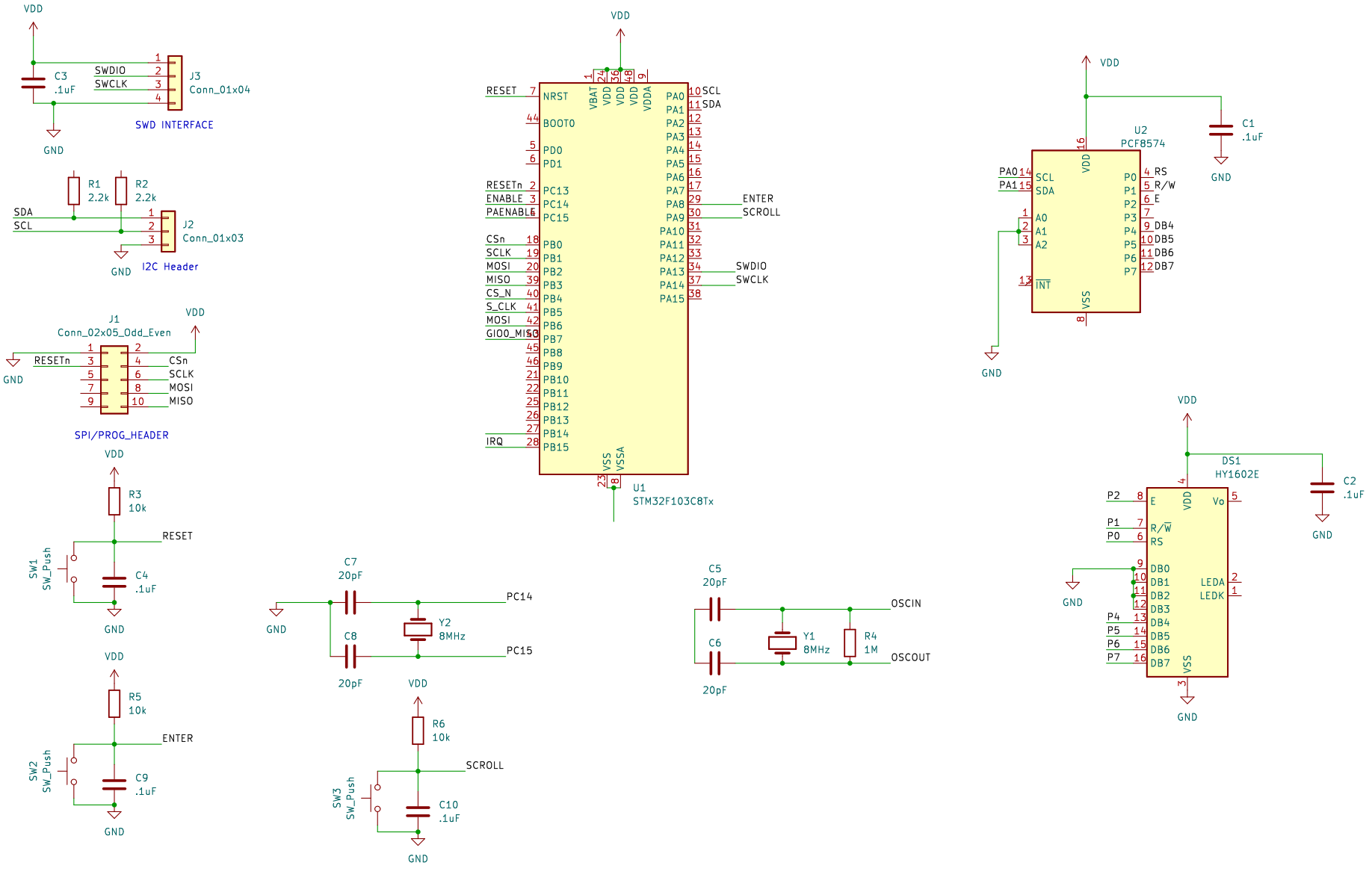
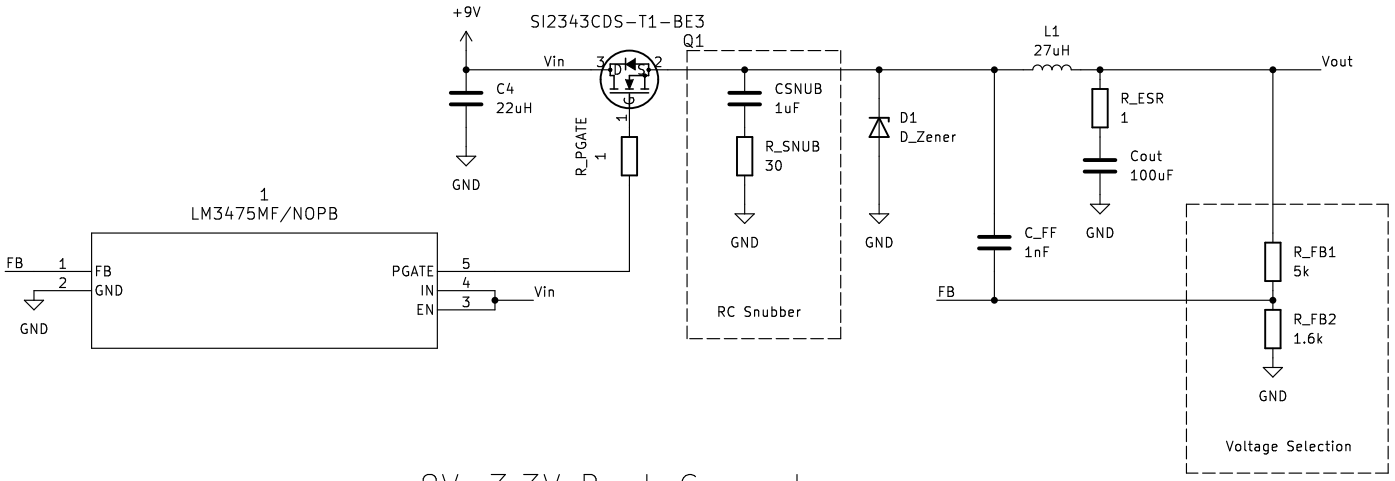


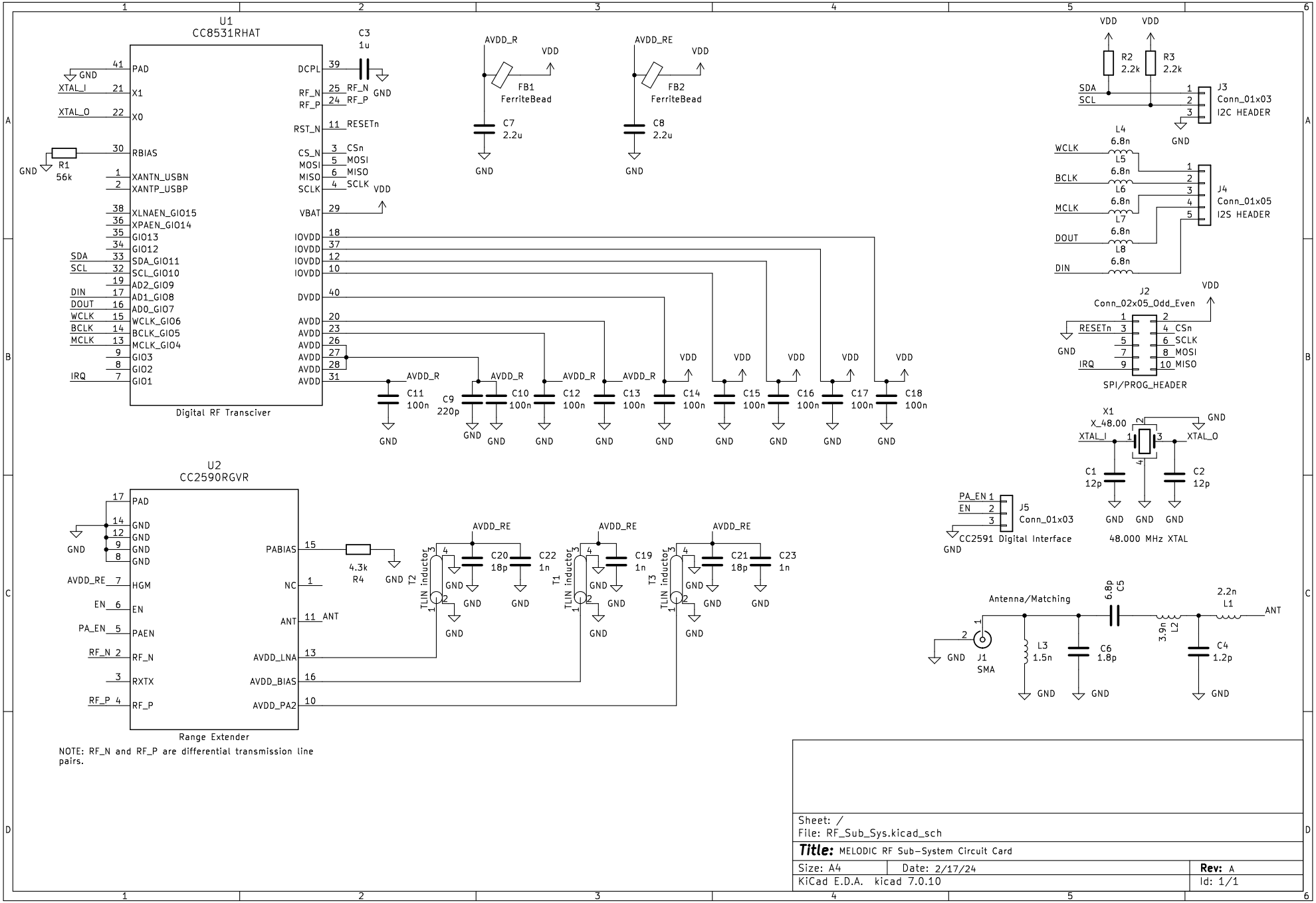
CONTROL SUBSYSTEM SCHEMATIC

COLIN DEVENNEY

A



9V-3.3V Buck Converter


U1
CC8531RHAT
Digital RF Transciver
U2
CC2590RGVR
Range Extender
NOTE: RF_N and RF_P are differential transmission line pairs.
J2
Conn_02x05_Odd_Even
SPI/PROG_HEADER
J3
Conn_01x03
I2C HEADER
J4
Conn_01x05
I2S HEADER
J5
Conn_01x03
CC2591 Digital Interface
X1
X_48.00
48.000 MHz XTAL
Antenna/Matching
J1
SMA
FB1
FerriteBead
FB2
FerriteBead
TLIN inductor
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Rev: A
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