

# LINE OPERATED VARIABLE VOLTAGE POWER SUPPLY

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## **Abstract**

This report presents the design and implementation of a line operated variable voltage power supply that is relatively low cost, accurate, and safe. The power supply utilizes switched-mode conversion for high efficiency and power factor correction, and includes subsystems for isolated input rectification, DC-DC conversion, microcontroller unit, and hardware. The output voltage should be adjustable from 5V to 25V at 50W, with less than 1% total deviation under full load and a power factor greater than 0.9. The design meets IEC 61000-3-2 standards for harmonic current and addresses common issues with low-cost bench power supplies such as drift, inaccurate readings, and lack of basic protection.

**Contents**

- 1. Introduction ..... 5
  - 1.1 Problem ..... 5
  - 1.2 Solution ..... 5
  - 1.3 Visual Aid ..... 5
  - 1.4 High Level Requirements ..... 5
  - 1.5 Block Diagram ..... 6
- 2 Design ..... 7
  - 2.1 Design Procedures ..... 7
    - 2.1.1 Isolated Input Rectification & Power Factor Correction ..... 7
    - 2.1.2 DC-DC Converter ..... 7
    - 2.1.3 Microcontroller Unit ..... 8
    - 2.1.4 Case and Hardware ..... 9
  - 2.2 Design Details ..... 9
    - 2.2.1 Isolated Input Rectification & Power Factor Correction ..... 9
    - 2.2.2 DC-DC Converter ..... 10
    - 2.2.3 Microcontroller Unit ..... 12
    - 2.2.4 Case and Hardware ..... 13
- 3. Design Verification ..... 14
  - 3.1 Isolated Input Rectification & Power Factor Correction ..... 14
  - 3.2 DC-DC Converter ..... 15
  - 3.3 Microcontroller Unit ..... 15
- 4. Costs and Schedule ..... 17
  - 4.1 Parts ..... 17
  - 4.2 Labor ..... 18
  - 4.3 Schedule ..... 19
- 5. Conclusion ..... 20
  - 5.1 Accomplishments ..... 20
  - 5.2 Uncertainties ..... 20
  - 5.3 Ethical considerations ..... 20
  - 5.4 Future work ..... 20
- References ..... 21

Appendix A Requirement and Verification Table .....	23
Appendix B Schedule .....	1

# 1. Introduction

## 1.1 Problem

Many low-cost bench power supplies are noisy with bad accuracy and are sometimes unsafe. Even the top positive reviews of Amazon's best-selling bench power supply (Kungber 30V 10A) [1] have serious complaints about its performance, such as drift, inaccurate display readings, excessive voltage error, and outright failure. Low-cost bench supplies with poor power factors inject harmonics into the power lines, and their switching noise and other distortions can disrupt precision circuits. Additionally, basic protections are sometimes lacking, leading to unsafe conditions that could damage the supply, the circuit, or the user.

## 1.2 Solution

We intend to build a line operated variable voltage power supply that is relatively low cost. To provide for low cost, isolation, and high efficiency, switched mode conversion will be used to correct the power factor, as well as to ultimately transform the voltage from line levels down to the selected voltages while providing for the output error specifications. Its subsystems will include isolated input rectification & power factor correction, DC-DC conversion, microcontroller unit, and case & hardware. Its output should be adjustable from 5V to 25V at 50W, at less than 1% total deviation under a static full load, with  $PF > 0.9$  while meeting IEC 61000-3-2 standards for harmonic current.

## 1.3 Visual Aid

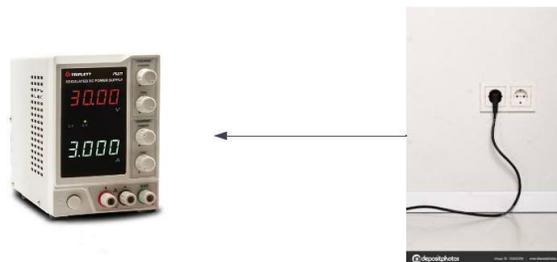


Figure 1-Power Supply

## 1.4 High Level Requirements

To consider our project successful, our power supply must fulfill the following requirements:

1. The power factor for the device will be greater than 0.9.
2. The device will meet or exceed IEC 61000-3-2 standards for harmonic current.
3. The device will deliver 5V - 25V at 50W with 1% accuracy to a static load across the whole voltage range.

# 1.5 Block Diagram

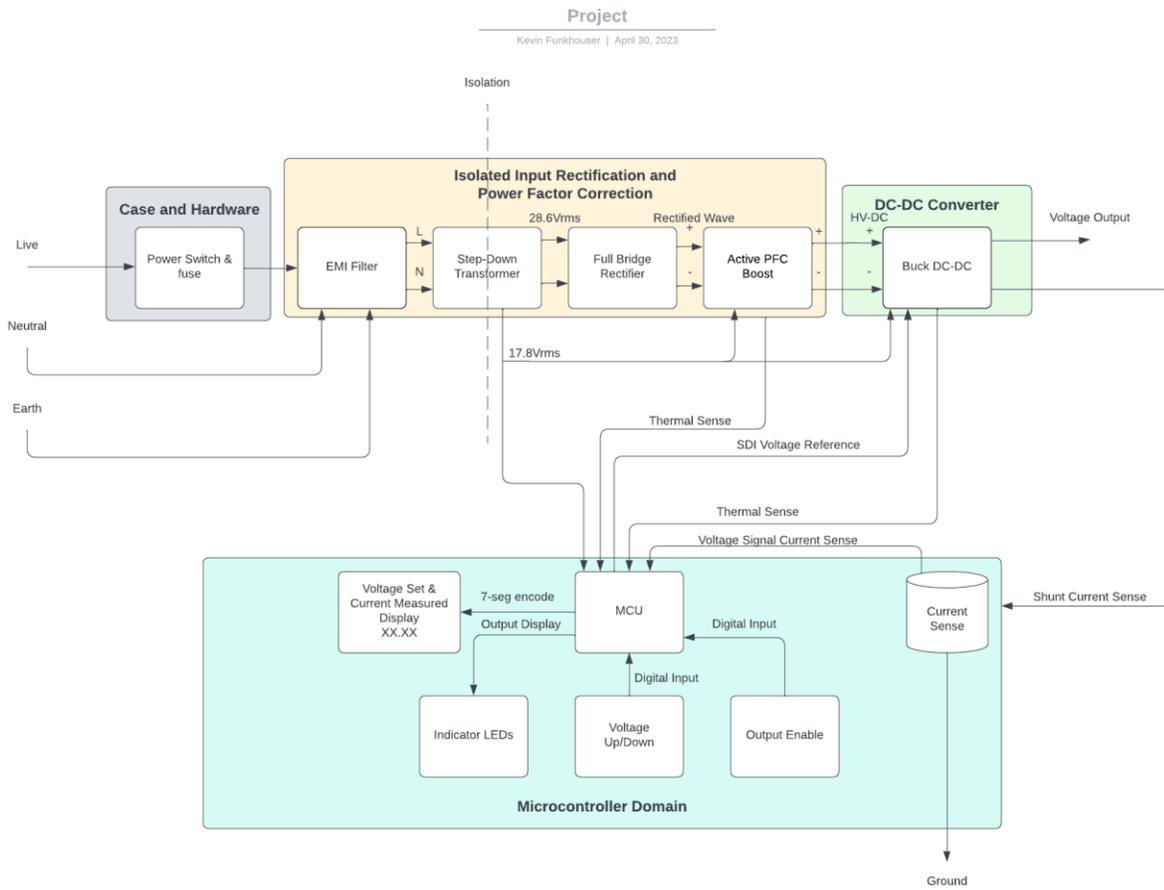


Figure 2-System Block Diagram

## 2 Design

### 2.1 Design Procedures

#### 2.1.1 Isolated Input Rectification & Power Factor Correction

The current proposed system entails an EMI filter followed by a line voltage step down transformer, which feeds a full bridge rectifier followed by a boost power factor corrector. The rectified output is then boosted to a high voltage DC (HVDC) intermediate bus at 55Vdc, which is later switched down to output levels. There are a variety of chips that can control a boost converter for PFC use, such as the UCC28180. The full bridge can be a simple packaged component or individual general-purpose diodes. The step-down transformer, while inelegant, provides us with immediate galvanic isolation while lowering the HVDC rail voltage. This allows us to avoid isolated DC-DC switching topologies, which have degraded performance generally due to optocoupler limitations. Additionally, inductors are much more varied and cheaper off the shelf, whereas transformer choice is more particular - this could save us from having to use a custom transformer or winding our own. It is of note that there is a power switch and fuse “upstream” of this subsystem. This circuit should meet IEC 61000-3-2 standards for line harmonic current. This subsystem will have a chip regulator to deliver power to control circuitry. When looking at the circuitry of this subsystem we will be using Fig. 3 taken from Texas Instrument [2]. We will of course make sure to have a transformer between the EMI filter and the four-bridge circuit to isolate the system.

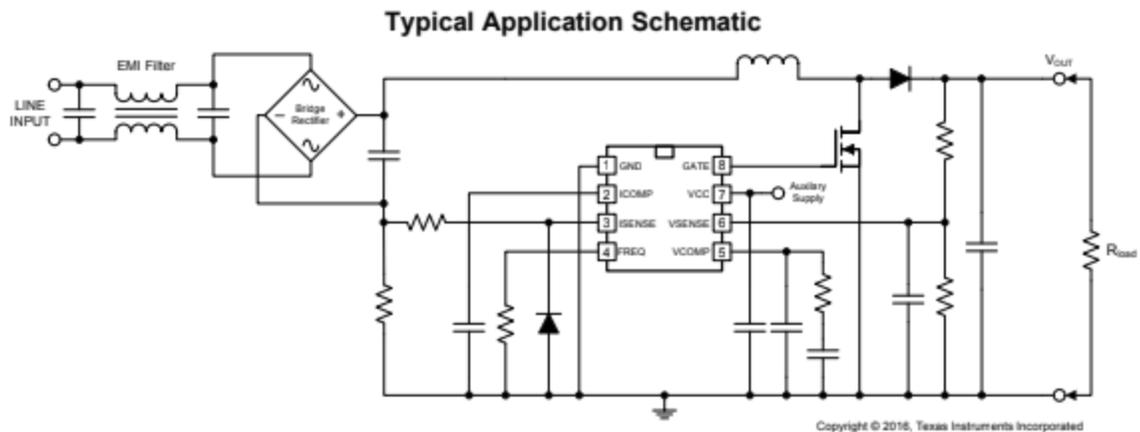


Figure 3-Boost Power Factor Correction Controller

#### 2.1.2 DC-DC Converter

This regulated converter will transform from 55Vdc down to the desired voltage. The proposed topology is a single phase synchronous buck converter due to its simplicity and efficiency. Control circuitry will entail a PWM controller and compensation system. The system is compensated with a Type III compensation according to [8], yielding a 10kHz error amplifier



purpose because of its familiarity, ease of use, and generous GPIO and ADC inputs. This subsystem will have a chip regulator to deliver power to the MCU.

#### **2.1.4 Case and Hardware**

This instrument will need to be operable. It will need to have a case with adequate venting and heatsink capabilities, a three prong plug with strain relief, a fused input, and a power switch. Shielding will be investigated. It will also need to have simple displays to tell real time voltage and current conditions. There must be a dial or buttons to select voltage and output enable, and banana plugs or other connectors for power, ground, and earth. There must be LED indications for 'output active' and 'fault condition' signals. The case must be adequately grounded if applicable.

## **2.2 Design Details**

### **2.2.1 Isolated Input Rectification & Power Factor Correction**

The isolated input rectification consists of a double tapped center transformer at the input that steps down the 120 VAC down to 28.6 Vrms. It is then rectified using a full bridge rectifier and boosted to a high voltage at 55V. The boosting is controlled by a UCC28180 TI chip that is also provided for power factor compensation. The UCC28180 chip has 8 pins and provides active power factor correction, low current distortion and excellent high voltage regulation of boost pre-regulators in AC-Dc applications. The controller can operate in 100-W to few kw range which in our use is boosting to 55V at 100W. The programmable frequency is operable between 18 KHz to 250KHz in our case we operate at 117KHz. Our boost inductor is rated at 56uH and can provide a duty cycle of 0.331 with a current ripple of 2.09A and can withstand a peak current of 6.94A. Our switching element is a standard n-transistor with a gate to source voltage of 15.2V provided by the UCC28180. Our total FET loss is 2.56W and an appropriate heat sink was provided. A current sense resistor of 0.02 ohms is provided to compensate for when the inductor current is at soft over-current threshold. Our output capacitor is 6800uf and rated for 80V and provides an output voltage peak-peak ripple of less than 5%. The following schematic below is our circuit schematic in KiCad.

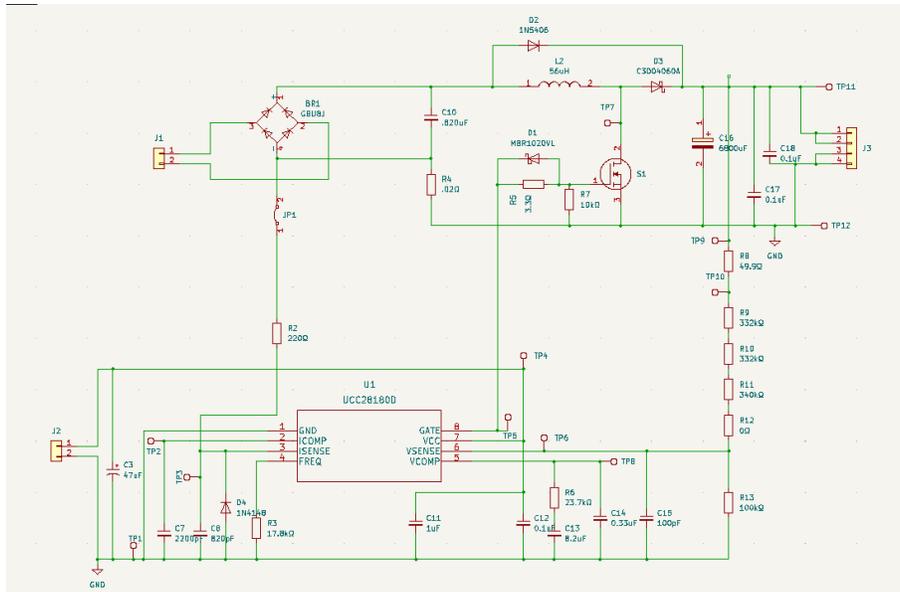


Figure 5-Boost PFC Controller Schematic

### 2.2.2 DC-DC Converter

The DC-DC Converter must meet specifications in both ripple, DC offset, and stability to be able to deliver proper amounts of current at the specified output voltages. To maintain continuous conduction mode under heavy loads, a large power inductor retrieved from scrap was arbitrarily chosen, tested for physical parameters and current handling capabilities, and tested in simulations to ensure proper ripple specifications. A 178uH, 15A toroidal inductor was chosen. Once this was done, a capacitor was determined in simulation to be the closest 10% preferred value to that which would yield 0.1% voltage ripple at 5V, 10A. A 47uF, 100V electrolytic capacitor was chosen for this purpose. Ripple current on the capacitor is limited to below 250 mArms, meeting ripple specifications. Simulations indicated no more that 0.2% voltage ripple across the output range. Stability was suggested based upon dominant pole compensation simulations, though the actual proposed topology was not fully simulated – we expected experimental verification through use of vector analyzers and reference material in figures 6 and 7 to be fruitful.

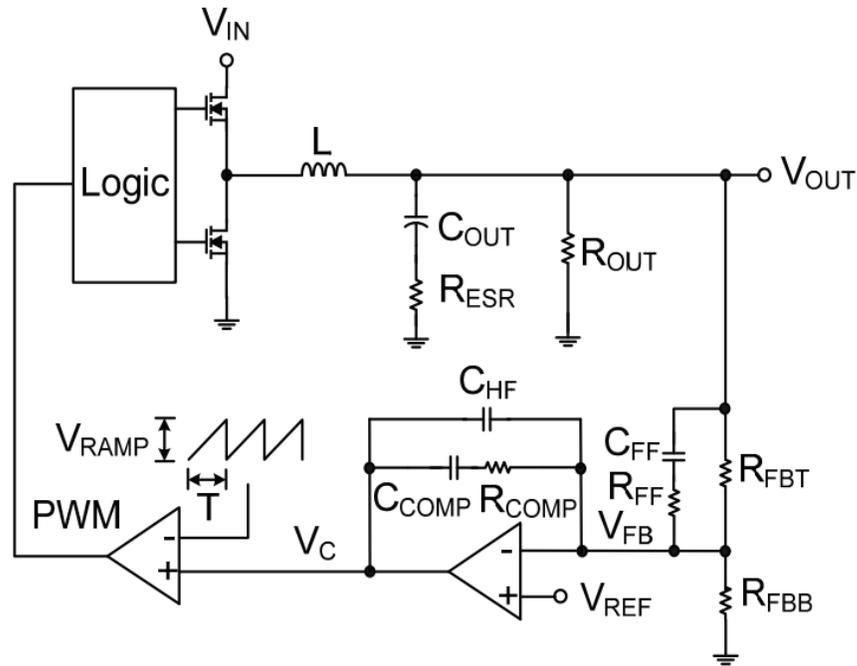


Figure 6-Type III Voltage Mode Compensation

$$A_{VM} = \frac{\omega_C}{A_{VC} \cdot \omega_O}$$

$$R_{COMP} = A_{VM} \cdot R_{FBT}$$

$$C_{FF} = \frac{1}{\omega_{FZ} \cdot R_{FBT}}$$

$$C_{COMP} = \frac{1}{\omega_{ZEA} \cdot R_{COMP}}$$

$$C_{HF} = \frac{1}{\omega_{HF} \cdot R_{COMP}}$$

- Choose a value for  $R_{FBT}$  based on the bias current and power dissipation.
- Pick a target bandwidth; typically,  $f_{SW}/10$ :  $\omega_C = 2 \cdot \pi \cdot f_C$ .
- Find  $A_{VM}$  to achieve the target bandwidth.
- Set  $\omega_{ZEA}$  and  $\omega_{FZ}$  equal to the output-filter complex conjugate pole  $\omega_0$ :  $\omega_{ZEA} = \omega_{FZ} = \omega_0$ .
- Set  $\omega_{FP}$  equal to the output-filter zero,  $\omega_z$ :  $\omega_{FP} = \omega_z$ .
- Set  $\omega_{HF}$  equal to half the switching frequency:  $\omega_{HF} = 2 \cdot \pi \cdot f_{SW}/2$ .

Figure 7-Type III Compensation Component Selection Methodology

### 2.2.3 Microcontroller Unit

The microcontroller subsystem consists of the ATmega328p chip, a voltage regulator, a LTC2630ACSC6-LZ12 Digital to Analog Converter (DAC), two 74hc595 shift registers, and buttons for power and for setting the voltage. It also has indicator LEDs for power and for a fault signal. Finally, it has connections to current and thermal signals and an AVR ISP header for programming. The schematic for the Microcontroller PCB is shown below.

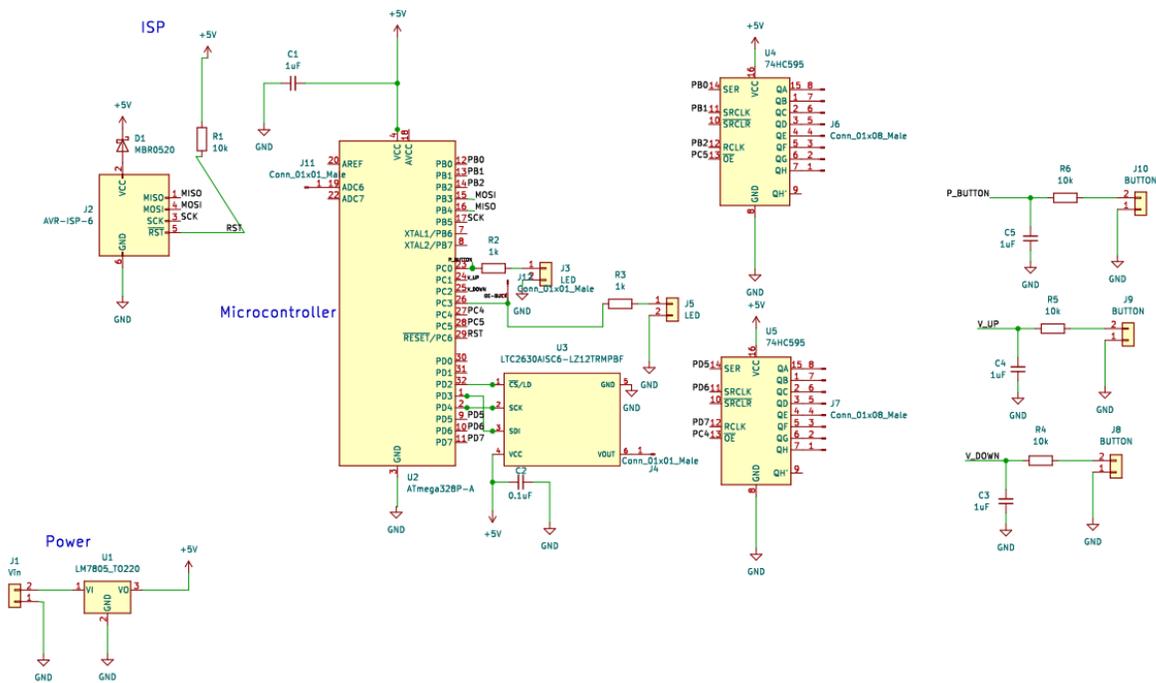


Figure 8-PCB schematic of MCU

In the figure above, the ATmega328p chip is powered by a voltage regulator that delivers 5V to it. The chip enables or disables the DC-DC buck converter using an output enable signal, which is generated based on the current and thermal sense signals as well as the status of the power button. The voltage is set using the voltage up and down buttons. Interrupts are set for these two buttons so that the MCU does not have to continuously check for the voltage state. The voltage data is sent over to the DC-DC converter via the LTC2630ACSC6-LZ12 DAC using SPI protocol. This specific DAC was chosen due to its high level of resolution and accuracy, and because its operating voltage being between 2.7 and 5.5V.[10]. The schematic also features 2 shift registers which are there to expand the number of GPIO pins of the ATmega328p chip. This allows us to use just a few pins to display 3 digits of both voltage and current data on a 7-segment display board such as the LDQM516RI. Pictured below is the high-level flowchart which provides a visual representation of the code's logical flow.

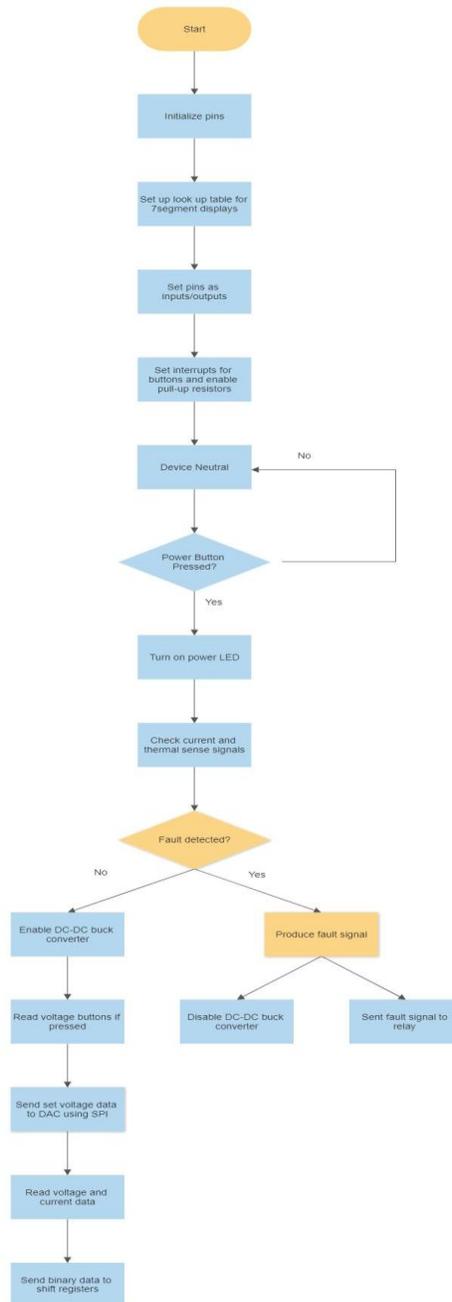


Figure 9-Flowchart for MCU code

### 2.2.4 Case and Hardware

Our case and hardware are intended to hold all PCBs together intact. We have a separate enclosure for our step-down transformer as well as appropriate plug extensions and a switch to turn the transformer on and off. A display as well as dials and banana plugs are intended for the user to know what the output voltage is and to be able to plug into an external circuit.

### 3. Design Verification

Our line operated variable voltage power supply utilizes switched-mode conversion for high efficiency, isolation, and correction of the power factor and harmonic distortion.

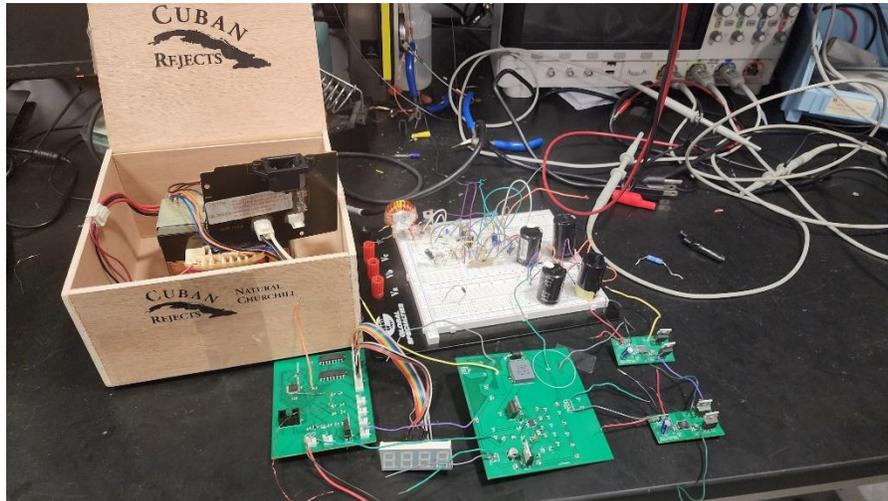


Figure 10-Line Operated Variable Voltage Power Supply Prototype

#### 3.1 Isolated Input Rectification & Power Factor Correction

Two of our high-level requirements were intended to be met by this subsystem. However, we encountered problems with our gate signal that would not appropriately boost and cause us to operate in DCM. When we replaced the shunt resistor connected to  $V_{sense}$  we allowed our gate signal to generate a PWM waveform. However, shortly after there was an inrush of current that led our output capacitor to fail. The high voltage we operated at made it difficult to debug when the circuit was on and check for what was not working. We did end up using a variac for a soft start and found that the gate signal failed to provide a PWM waveform for low voltage which is not supposed to happen. However, we were able to verify that our input and output were galvanically isolated by the step-down transformer, and we confirmed this via a continuity tester to verify that the windings were isolated. A couple of things we would change is to have an output capacitor with a higher rated voltage, this would give us more leeway when testing our circuit and figuring out why we were boosting so much. Some other components in our circuit were not appropriately rated as well due to smoke coming from certain components like  $R_{sense}$ . We would reorder certain components with the appropriate rated values if we had to start over. Using the variac during debugging we found that we could boost to a higher voltage however we were only able to operate in DCM.

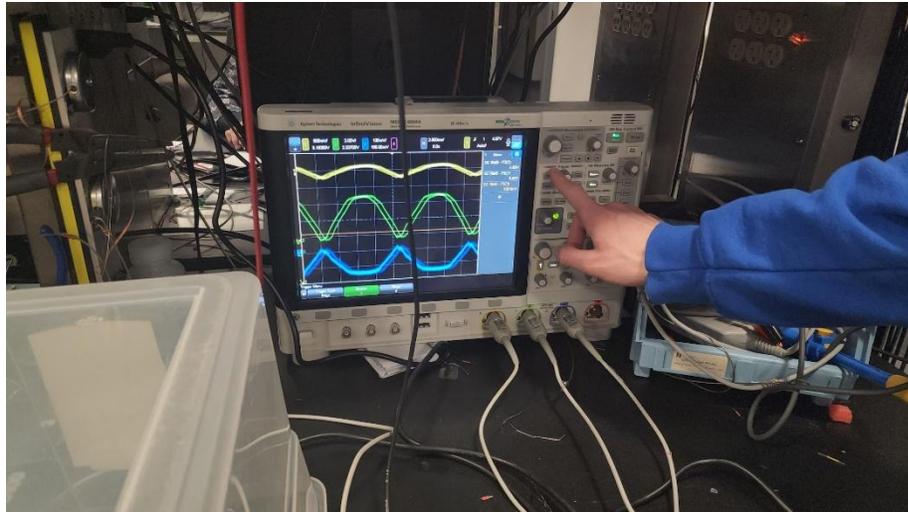


Figure 11-Boost PFC Controller operating in DCM

### 3.2 DC-DC Converter

Ultimately, an acceptable DC-DC Converter PCB did not arrive on time. Therefore, verifications are limited to simulations. We can observe the ripple specifications to see that they are met. We can observe that at 5V, 10A, there is approximately 6.7mV of output voltage ripple expected. This is much less than the requisite 50mV. This output can meet specifications across the whole output range.

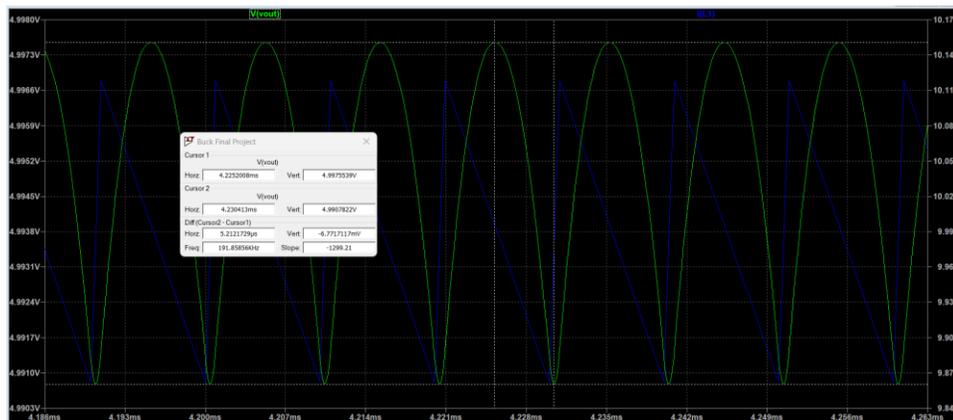


Figure 12-Inductor Current Ripple and Output Voltage Ripple

### 3.3 Microcontroller Unit

The requirements of the microcontroller unit were difficult to verify due to the lack of the DC-DC converter. Both the voltage selection and the output enable signal required the DC-DC converter to interface with. The voltage selection SPI bitstream was not able to be verified but the

output enable/disable signal was verified using an LED labelled as J6 in the PCB schematic given in Figure 8. The current and thermal overload signals were also successfully processed by the MCU. These overload conditions were simulated using signal generators. The following snippet of code was used to test these signals.

```
int currentSense = analogRead(A6);
int thermalSense = analogRead(A7);

// Check if current sense and thermal sense values are within the acceptable
range
if (currentSense < 500 && thermalSense < 500) { // 0-1024 500 ~ 2.5V
    digitalWrite(OE_PIN, HIGH);
} else {
    digitalWrite(OE_PIN, LOW);
}
```

Here A6 and A7 are the analog input pins that correspond to the current and thermal sense signals respectively. An arbitrary threshold of 500 was set which equates to roughly 2.44V. In the equation below, the 5V is the reference voltage and the range of the ADC is 0 to 1023 bits.

$$((5V/1024) * 500) = 2.44V \quad (1)$$

## 4. Costs and Schedule

### 4.1 Parts

Table I: Total Cost of Components

Description	Part Number	Price	Quantity	Extended Price
Switching Controllers CURR MDE PWM CNTRLR FWD FLYBCK APPS	NCP1252BDR2G	\$0.94	2	\$1.88
PFC boost controller IC	UCC28180	\$1.056	2	\$2.11
Microcontroller chip	ATMega328p	\$3.08	3	\$9.24
Single 12-/10-/8-Bit Rail-to-Rail DACs with Integrated Reference in SC70	LTC2630ACSC6-LZ12	\$6.54	2	\$13.08
Temperature sensor	NTE7225	\$1.79	5	\$8.95
Voltage Regulator	LM7805	\$1.65	3	\$4.95
Shift registers	SN74HC595N	\$0.67	3	\$2.01
LED (green)	754-1731-ND	\$0.37	2	\$0.74
Power button	RF1-1A-DC-2-R-1	\$1.26	2	\$2.52

Tactile switches	1825910-6	\$0.13	5	\$0.65
SMPS Controller IC	TEA1892TS/1H	\$1.16	2	\$2.32
100 $\Omega$ resistor	CFR-50JB-52-100R	\$0.11	10	\$1.10
1k $\Omega$ resistor	CFR-25JB-52-1K	\$0.10	10	\$1.00
10k $\Omega$ resistor	CFR-50JB-52-10K	\$0.11	10	\$1.10
100k $\Omega$ resistor	CFR-50JB-52-100K	\$0.11	10	\$1.10
0.1 $\mu$ F capacitor	C320C104J5R5TA7301	\$0.49	10	\$4.90
10 $\mu$ F capacitor	C322C106K3R5TA	\$0.79	10	\$7.90
0.33 $\mu$ F capacitor	C322C334Z5U5TA	\$0.46	10	\$4.60
Diode	1N4935-T	\$0.21	10	\$2.10
EMI filter	DSS1NB31H473Q91A	\$0.48	2	\$0.96
7-segment display	LDQM516RI	\$9.08	3	\$27.24
Molex connector 1x8	WM4117-ND	\$0.71	4	\$2.84
Molex connector 1x2	900-0022232021-ND	\$0.21	7	\$1.47
Jumper wires	1568-1513-ND	\$2.10	1	\$2.10

## 4.2 Labor

Each member in the group expects a salary of  $\$40/hr \times 2.5 \times 56hr = \$5600$ . If we include every team member that number is equal to  $\$5600 \times 3 = \$16,800$ .

Total cost of components = \$106.86

Total cost = combined labor cost + total cost of components = \$16,800 + \$106.86

= \$16906.86

### **4.3 Schedule**

See Appendix B for schedule.

## 5. Conclusion

### 5.1 Accomplishments

We were able to meet some of our requirements and verifications. For example, we were able to galvanically isolate our input and output via a transformer. We also used a relay for the converter to respond to the MCU signal to enable and disable the output. We also had adequate case and hardware for our step-down transformer. The MCU was also able to respond to the current sense signal and the thermal sense signals to produce and display a fault condition signal.

### 5.2 Uncertainties

We debugged the Boost PFC Controller circuit for any unusual circuit characteristics. We found that at a low voltage we were able to boost, however our gate signal would not provide a PWM waveform and was not able to regulate the output voltage. For this reason, we suspect that when we turned on the transformer an inrush of current flowed through Risense which made it go up in smoke. Our output was boosted to a voltage higher than what the capacitor was rated for and made it blow. We used a variac to control the input voltage and found we operated in DCM. The MCU was also able to appropriately determine and display an output enable signal based on the circuit conditions and the output enable button.

### 5.3 Ethical considerations

We would like to reiterate the importance of ethics and safety in our project. Working with high voltage requires proper training and caution. As such, all members of our team underwent high voltage safety training. When testing at high voltages, we ensured that we took proper safety precautions such as covering the circuit with a plastic box to prevent any arcs. We ensured that the input and output was galvanically isolated. Furthermore, we implemented a slow start during our testing by using a variac. This helped prevent any damage to us as well as the circuitry. We used heatsinks for components that were prone to heating and as mentioned earlier, we were able to successfully implement a relay subsystem which would disconnect the output if a fault signal was to be detected. The specifications of the device were also properly measured, characterized, and accurately reported so that the user can operate within a safe and predictable region. Additionally, to respect and credit the work which helped us build our project, we will cite our sources. Citing our sources as well as accurately reporting specifications falls under IEEE Code of Ethics I.5 [7].

### 5.4 Future work

Future work includes ordering, assembling, and verifying the DC-DC Converter, updating the PFC board with appropriately rated traces and components, and integrating the microcontroller system to the DC-DC converter.

## References

[1] Kungber, (2021). Kungber Adjustable DC Power Supply, Switching Regulated Power Supply with 4 Digital Display and Voltage Current Adjustments.

[https://www.amazon.com/Kungber-Adjustable-Switching-Regulated-Adjustments/dp/B08DJ1FDXV/ref=sr\\_1\\_3?keywords=Bench%2BPower%2BSupply&qid=1674944329&sr=8-3&th=1](https://www.amazon.com/Kungber-Adjustable-Switching-Regulated-Adjustments/dp/B08DJ1FDXV/ref=sr_1_3?keywords=Bench%2BPower%2BSupply&qid=1674944329&sr=8-3&th=1)

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[8] Meeks, D. “Loop Stability Analysis of Voltage Mode Buck Regulator with Different Output Capacitor Types – Continuous and Discontinuous Modes.” Texas Instruments Application Report (SLVA301), April 2008

[9] TPSI3050, Texas Instruments Inc. (2022). Data Sheet. Retrieved from:

[10] Analog Devices, Inc. (2017). LTC2630/LTC2631 - 12-/10-/8-Bit Rail-to-Rail DACs with I2C Interface Data Sheet. Retrieved from <https://www.analog.com/media/en/technical-documentation/data-sheets/2630fg.pdf>

## Appendix A

## Requirement and Verification Table

Table II: Subsystem Requirements and Verifications

Subsystem	Requirements	Verifications	Met?
Isolated Input Rectification & PFC	<ol style="list-style-type: none"> <li>1. The power factor of the subsystem must be greater than 0.9.</li> <li>2. The input current must meet or exceed IEC 61000-3-2 standards for harmonic current.</li> <li>3. The output voltage must be maintained between 60VDC and 80VDC.</li> <li>4. The input and output must be galvanically isolated.</li> </ol>	<ol style="list-style-type: none"> <li>1. We can analyze the power factor using a power factor meter.</li> <li>2. A spectrum analyzer will allow us to measure harmonic current. We will need to reference the IEC 61000-3-2 document.</li> <li>3. We can easily measure this by oscilloscope or DMM.</li> <li>4. A continuity tester will determine if the transformer windings are isolated.</li> </ol>	No
			No
			No
			Yes
DC-DC Converter	<ol style="list-style-type: none"> <li>1. The converter must convert the HV DC bus voltage to the specified output voltage between 5Vdc and 25Vdc within 1% static error at 50W.</li> <li>2. The converter must be able to respond to the MCU signal to enable and disable its output.</li> </ol>	<ol style="list-style-type: none"> <li>1. The output voltage and current could be measured with an oscilloscope or a DMM.</li> <li>2. The fault can be simulated using a signal generator. The disconnection can be measured with an oscilloscope or continuity tester.</li> </ol>	No
			Yes

Case & Hardware	<ol style="list-style-type: none"> <li>1. The case must be able to contain all of the circuitry and allow mounting with adequate venting.</li> <li>2. The case must have displays, buttons, switches, and plugs for user interaction.</li> </ol>	<ol style="list-style-type: none"> <li>1. This can be verified by inspection.</li> <li>2. We can verify with a DMM that the case is not electrically live.</li> </ol>	Yes
			No
Microcontroller Unit	<ol style="list-style-type: none"> <li>1. This system must process the voltage selection input and output a SPI bitstream for the DC-DC converter.</li> <li>2. This system must respond to the current sense signal and the thermal sense signals to produce and display a fault condition signal.</li> <li>3. This system must be able to process the set voltage and the measured current for display.</li> <li>4. This system must be able to appropriately determine and display an output enable signal based on the circuit conditions and the output enable button.</li> <li>5. The system must have connections for programming.</li> </ol>	<ol style="list-style-type: none"> <li>1. The SPI bitstream can be verified by a logic analyzer, or by inspecting the DC-DC converter DAC output.</li> <li>2. Current overload and thermal overload conditions can be simulated using signal generators, the response can be observed by DMM.</li> </ol>	No
			<ol style="list-style-type: none"> <li>3. The display can be observed visually, or by logic analyzer, upon forcing MCU input signals with a signal generator.</li> </ol>
		<ol style="list-style-type: none"> <li>4. This can be done by inspecting the DC-DC converter or by using an LED.</li> <li>5. The programming success can be determined by the Arduino IDE.</li> </ol>	
			Yes
No			

## Appendix B Schedule

Table III: Final Project Schedule

Week	Task	Person
February 19th-February 25th	Order parts for prototyping and desoldering parts from scrap equipment	Everyone
	LTspice simulation of power circuit	Cesar
	Researching/developing microcontroller interface	Feroze
	Verify design topology	Kevin
February 26th-March 4th	Start PCB Design	Everyone
	Test PFC > 0.9 using the power factor meter and revise circuit	Cesar
	Verify SPI bitstream with a logic analyzer and inspect DC-Dc converter DAC output	Feroze
	Verify Output Voltage bw 60 & 80 VDC through oscilloscope and DMM	Kevin
March 5th-March 11th	<b>PCB Orders March 7th</b>	Everyone
	Finalize PCB Design	Everyone
	Measure harmonic current with spectrum analyzer	Cesar
	Ensure input/output is galvanically isolated	Kevin
	Simulate overload and thermal overload conditions using signal generators and observe through DMM	Feroze
March 12th-March 18th	SPRING BREAK	Everyone
March 19th-March 25th	Test converter takes HV to 5 and 25Vdc and is within 1% static error at 50W.	Cesar
	Ensure converter is able to respond to the MCU signal and can enable and disable its output	Kevin
	Test system is able to process the set voltage and the measured current for display	Feroze

March 26th-April 1st	<b>PCB Orders March 28th</b>	Everyone
	Make final adjustments to PCB board	Kevin
	Ensure MCU is able to appropriately determine and display an output enable signal based on the circuit conditions and the output enable button	Cesar & Feroze
April 2nd-April 8th	Finalize MCU testing and ensure the system has the connections for programming	Everyone
April 9th-April 15th	Fault detection simulations	Cesar
	Thermal Sense protection simulations	Feroze
	Integral tests on subdivision components	Kevin
April 16th-April 22nd	Mock Demo	Everyone
	Final adjustments to MCU	Feroze
	Revisions to PCB Design	Kevin
	Further Integral tests on subdivision components	Cesar
April 23rd-April 29th	Final Demo and attend Mock Presentation	Everyone
April 30th-May 4th	Last minute adjustments for Final Presentation and work on Final Paper	Everyone