ECE 445: Design Document

ACTIVE CELL BALANCING FOR SOLAR VEHICLE BATTERY PACK

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1 Introduction

1.1 Objective

In solar vehicles, charge is collected via a solar array and stored in a battery pack. Illini Solar Car (ISC) utilizes a lithium-ion battery pack with 28 series modules of 15 parallel cells each. The nominal voltage of the battery pack is 100.8 V and the maximum voltage is 117.6 V. In order to ensure safe operation, each battery cell must remain in its safe voltage operating range (2.5-4.2 V). When any single module leaves the safe operating range, the entire pack must stop charging or discharging. During testing and competition, ISC has observed a steady unbalancing of the voltages of the 28 modules. The battery is considered to be unbalanced when the voltages of parallel sets of cells (which we call modules) differ in voltage. As this occurs, the effective capacity of every module in the pack decreases to that of the weakest module. This occurs because once one module reaches 2.5 V, the battery pack can no longer be used even if energy remains in other parts of the pack. In previous competitions, this has rendered as much as 5% of the total energy in the pack unusable. Figure 1 shows how the imbalance in battery modules during the final portion of the race resulted in shutoff of the car while some cells had a significant amount of charge remaining.

To combat this loss in state of charge (SoC), we propose the addition of an active cell balancing system to ISC's battery pack design. Our system will redistribute charge from modules with more charge to modules with less charge. This design allows for the full capacity of each module in the pack to be utilized to power the car, rather than charge being left unusable in the pack. In this semester, we aim to complete a proof of concept for an active balancing system on a smaller scale that could be extended and integrated into future ISC battery packs.

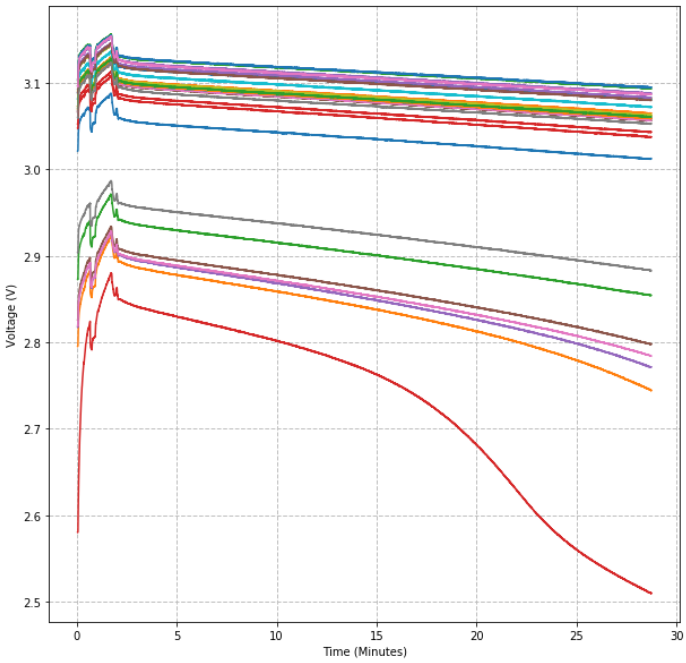


Figure 1: Module voltages during the last 30 minutes of race. Each color represents a different battery module.

1.2 Background

Solar-vehicle racing is an engineering-based competition where university teams compete to design, build, and race the best car powered only by the sun. These competitions are 2,000 mile endurance races that take place on public roads and highways over the course of many days. The primary goal is to build a reliable car that can maximize efficiency in order to travel the greatest distance during the event.

In order to fully utilize the charge in the battery pack, and travel the greatest possible distance, we believe a custom designed active balancing system to be the best choice. In a passive-balancing system, charge is dissipated from cells with higher voltages such that they are all discharged to the same voltage. Although it is a less complex design, passive balancing does not increase the amount of usable charge in a battery pack as active balancing does.

Additionally, a custom system offers additional benefits that are not available in off-the-shelf, active-balancing controllers. In off-the-shelf options such as the LTC3300, charge can only be transferred between neighboring modules [1]. In a custom design, charge could be transferred from any overcharged module to any undercharged module directly. Designs such as the LTC8584 are rated for a low balancing current that would require a parallelized design with multiple chips to reach a reasonable speed for pack balancing. The LTC8584 and other options are also monolithic, meaning an overcharged cell can charge the entire pack, but the pack cannot transfer charge to an undercharged cell [2]. As Figure 1 illustrates, the problem of an under-voltage cell is more relevant to our use case on a solar car. Furthermore, other options such as an EMB1428Q only support up to 60 V for total pack voltage, and the LTC3300 requires an interleaved design to reach higher voltages, which decreases overall balancing efficiency [1],[3]. A custom design could be highly extendable where more balancing units could simply be added to the bus with an extra control signal.

In conclusion, a custom active-balancing system would allow for high-current bidirectional balancing that is scalable to a battery pack of 28 modules.

1.3 Visual Aid

Figure 2 shows the motivation and objective for the project. Overall, active-cell balancing moves charge from cells with more charge to cells with less charge to fully utilize the capacity of all modules in the pack. Once the leftmost module is fully discharged, the remaining capacity of the other cells is useless. Manufacturing differences, age, and operating temperature over the cell lifetime can all cause a cell to discharge faster than another. Active balancing rectifies this difference by averaging the capacity of each cell during a charge or discharge cycle so that the entire capacity of the pack is useful. As Figure 2 shows this is advantageous over passive balancing as it does not waste charge.

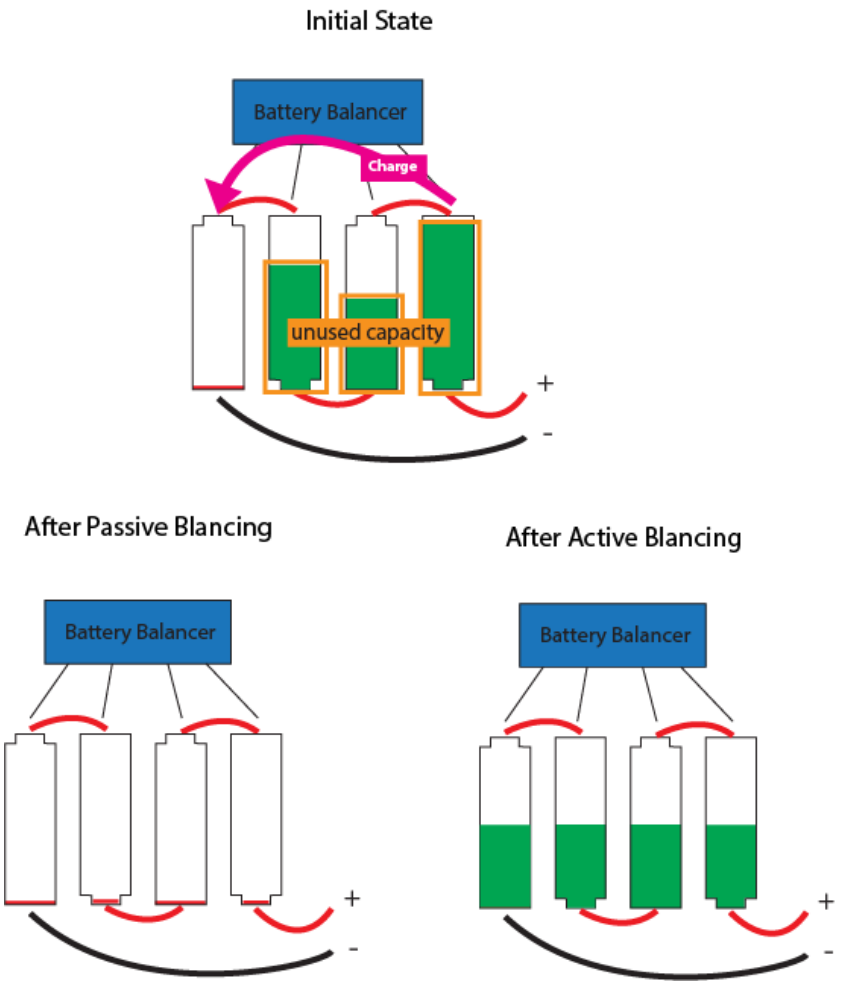


Figure 2: High-level system objective

1.4 High-Level Requirements

As a first revision in a new custom design, assessing the potential of the design is more important than meeting performance requirements required by a race. These high-level requirements reflect the goals of having a simple proof-of-concept design that future revisions will expand upon. The proof-of-concept design will operate on a pack with four modules in series and each module will have three cells in parallel.

- The active balancing circuit must be able to redistribute energy from the top module to the bottom module with $> 50\%$ efficiency.
- Over the course of 30 minutes of balancing, modules more than 0.2 V away from the average pack voltage must see their voltage move towards the pack average by at least 0.1 V.
- Individual module voltages must remain between 2.5 V and 4.2 V for the entire duration of a 30 minute balancing test.

2 Design

2.1 Block Diagram

The block diagram for this project is difficult to understand at a technical level without first understanding the high-level intent of the active-balancing architecture we are using. Figure 3 shows the general energy transfer path and the control loop for each DC/DC converter. The intent of this architecture is to transfer energy between each module and the supercapacitor storage element. The controller uses voltage feedback to set the transfer ratio of each converter, which determines if the corresponding module is charging or discharging. Thus, individual modules can be charged and discharged to maintain balance in the pack.

Figure 4 shows the implementation of our intended architecture as a full block diagram. The main energy transfer objective of the design is identical; however, the control and drive of the converters are explained in more detail. The feedback loop for module voltages now goes through existing voltage sensing hardware on the battery management system (BMS) and is transferred to the active balancing microcontroller on a controller area network (CAN) bus. Feedback on the supercapacitor side is measured as an analog voltage by the microcontroller after appropriate resistor divider circuitry. The microcontroller also enables a precharge resistor between the converter and the supercapacitor to limit the initial inrush current on start-up.

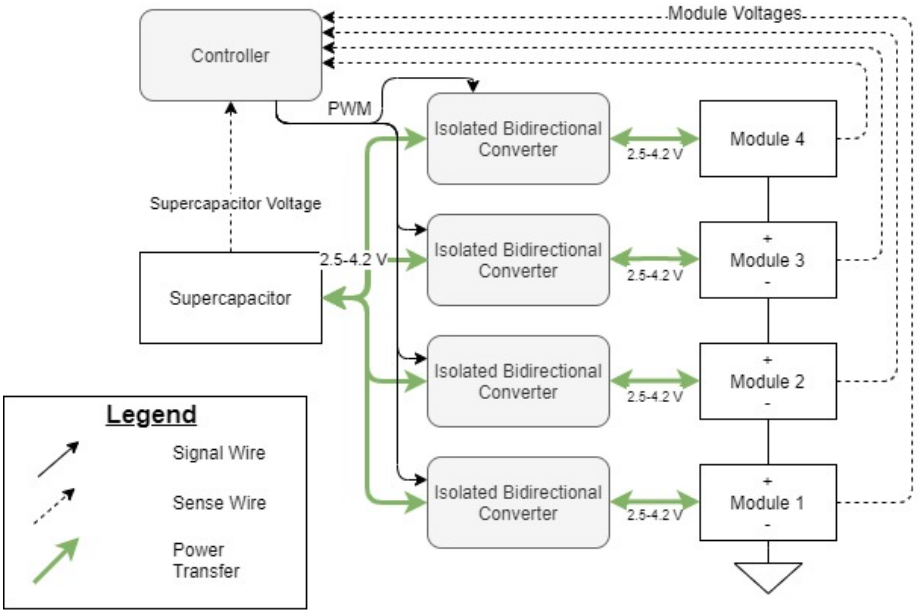


Figure 3: High-level architecture of active-balancing system with energy transfer and control loop

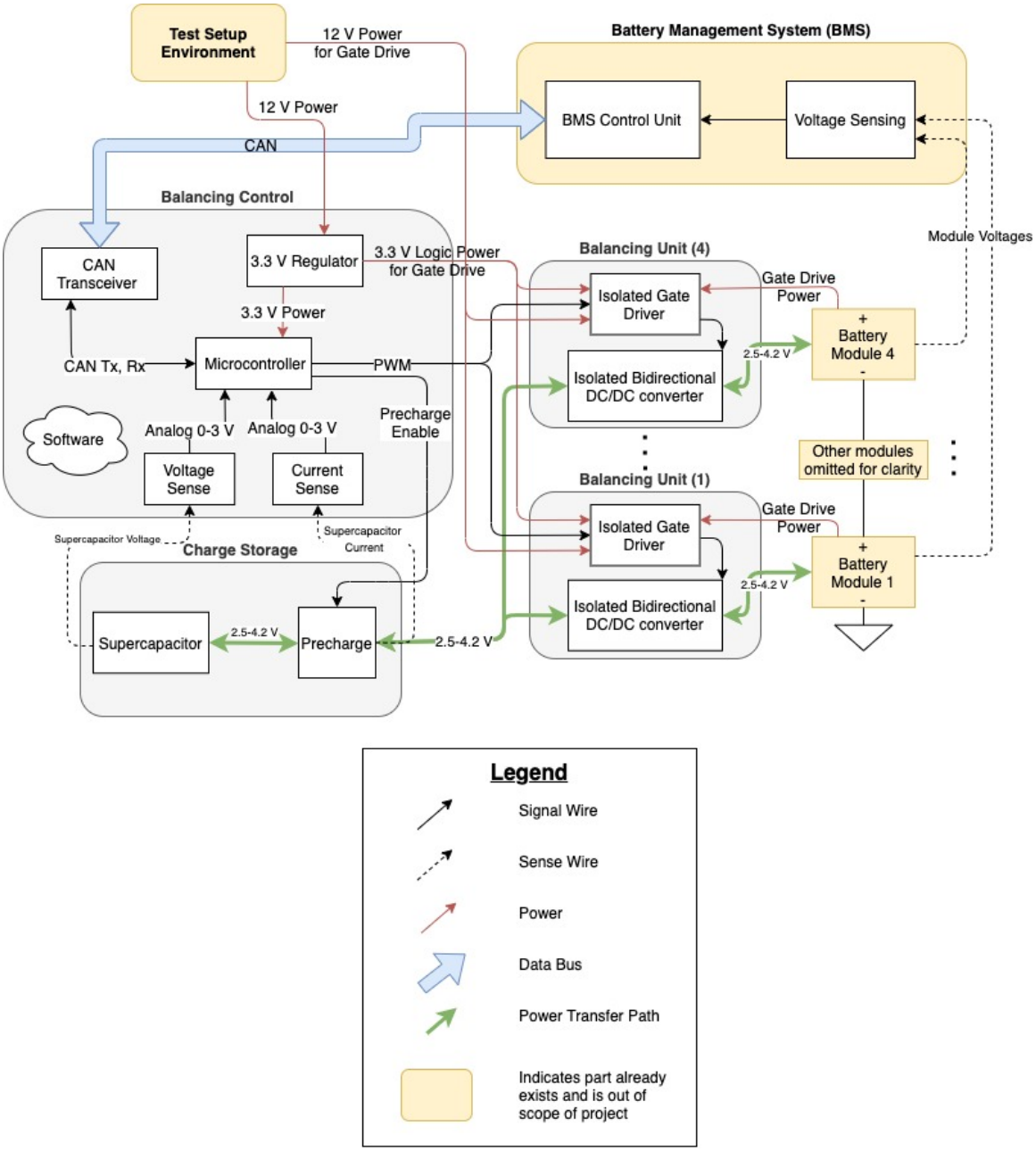


Figure 4: Full block diagram of active-balancing design

2.2 Balancing Control

The balancing control system is responsible for driving each of the isolated DC/DC converters to transfer charge either to or from the supercapacitor. The supercapacitor voltage is measured directly from the supercapacitor system as an analog reading, while the module voltages are received from the BMS via CAN. The balancing control then uses the respective voltages to drive each balancing unit using a pulse width modulation (PWM) signal.

2.2.1 3.3 V Regulator

The 3.3 V regulator provides power to the logic elements of the balancing circuit including the microcontroller and gate-drive circuitry. The microcontroller draws on the order of 100 mA during active operation, with a maximum of about 300 mA, and each gate driver draws a maximum of 10 mA from the 3.3 V input. With four gate drivers, and allowing for headroom, the 3.3 V regulator must be able to supply at least 500 mA. None of the components are sensitive to an incorrect supply voltage, so the regulator must be 3 ± 0.3 V of regulation.

2.2.2 Microcontroller

The LPC1549 microcontroller controls the balancing unit, measures and controls the super capacitor module, and interfaces with external systems. It interfaces with the BMS via CAN through the CAN transceiver. We chose the LPC1549 because it is used for other systems on ISC and features a CAN interface, analog inputs, digital IO, and state configurable timers (SCT) which are useful for high speed PWM control.

Requirement	Verification
1. Microcontroller must transmit and receive messages on CAN bus.	1. Program microcontroller to send a CAN message and blink an LED when receiving a CAN message. Connect microcontroller to CAN bus through the CAN transceiver. See that messages are received on the CAN bus and that the LED blinks when messages are sent.
2. Microcontroller must read analog inputs with accuracy of ± 10 mV from 0 to 3 V.	2. Connect the analog input to a potentiometer and measure the voltage of the potentiometer with a multimeter. Send measurements via CAN. Verify that measured values are accurate to multimeter reading within ± 10 mV.
3. Microcontroller must generate 4 PWM signal with frequency of at least 250 kHz.	3. Write code to generate 4 PWM signals and probe their outputs with a oscilloscope. Verify that the signals have defined minimum frequency.
4. Microcontroller must generate digital output signals.	4. Write code to blink an LED at 1Hz. Verify visually that LED connected to the output pin blinks. Connect output from microcontroller to oscilloscope to verify blinking is at a frequency of 1Hz.

2.2.3 Voltage Sense

The voltage sense circuit will convert the supercapacitor voltage to a voltage range that can be read by the ADC of the microcontroller. It will do this through a resistor divider.

Requirement	Verification
1. Voltage sense must output an analog voltage between 0 and 3 V that can be read as a voltage value with accuracy of ± 10 mV from 0 to 5 V.	1. Connect a voltage source to the resistor divider circuit. Set the output of the voltage source from 0 to 5 V in 0.25 V increments. Connect the analog output of the resistor divider circuit to a multimeter. Verify that the output of the resistor divider circuit remains between 0 and 3 V and varies linearly with the input.

2.2.4 Current Sense

The current sense will create an analog voltage signal to be read by the microcontroller. The voltage across a shunt resistor will be amplified by an op-amp to produce signals that can be interpreted by the microcontroller.

Requirement	Verification
1. Current sense must output an analog voltage between 0 and 3 V that can be read as a current value in both directions with accuracy of ± 50 mA from -10 A to 10 A.	1. Connect a voltage source across the shunt resistor. Vary current from -10 A to 10 A at 0.5 A increments and measure output voltage signal using multimeter attached between the current sense output pin and ground. Calculate current from voltage measurement using Ohm's Law. Confirm that the measurements are within the specified accuracy.

2.2.5 CAN Transceiver

The CAN transceiver is responsible for converting the differential wire pair from the CAN bus to transmit and receive lines that the microcontroller is able to interpret. The CAN transceiver also provides isolation between the board and the CAN bus and converts the 3.3 V board logic to 5 V CAN logic. If the CAN transceiver works correctly, the microcontroller should be able to send and receive messages from a connected CAN bus. See Figure 5 for a complete CAN schematic.

Requirements	Verification
1. CAN transceiver must relay messages on the CAN bus in a readable format for the microcontroller.	1.1. Program microcontroller to send heartbeat message via CAN once every second. Attach a CAN bus analyzer to the CAN bus and use it to provide CAN power. Read CAN messages in software to determine if heartbeat message is sent from the balancing microcontroller. 1.2. Program microcontroller to blink an LED on the receipt of a certain CAN message. Connect the CAN bus analyzer and supply CAN power. Send designated message using CAN bus analyzer and confirm that an LED blinks on the board.

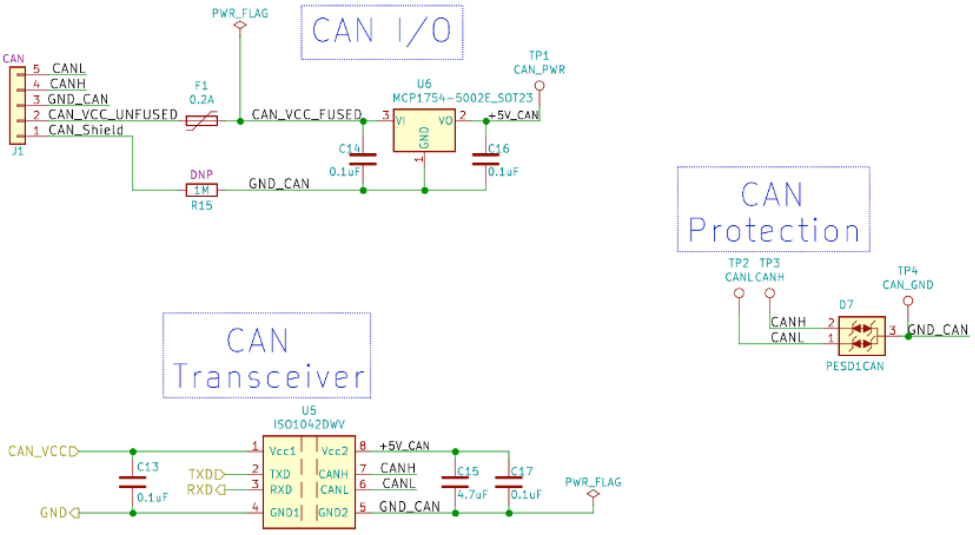


Figure 5: Detailed schematic of CAN transceiver, input and output, and protection

2.2.6 Software

The primary purpose of the software in this system is to control the individual balancing units through PWM control of a number of MOSFET gates in the balancing unit and in the precharge circuit. This requires voltage and current inputs to achieve closed loop control. The software must decide where to move charge. It will do this by determining which module has the least charge and which has the most charge based on their voltage readings. The software then must generate PWM signals to charge the supercapacitor and enable precharging when necessary based on voltage inputs. It will then generate PWM signals to transfer the supercapacitor charge to the low voltage module. In addition to these functions, the software will send log messages over CAN for diagnostics and performance analysis.

Requirement	Verification
1. The software must enable precharging whenever the supercapcitor's voltage is below 2 V.	1. Connect a voltage source to the supercapcitor voltage sense input on the microcontroller. Based on supercapacitor's resistor divider circuit, provide voltage inputs to the microcontroller corresponding to supercapcitor voltages from 0 V to 4.2 V. Measure the precharge enable output with a multimeter and see that it enabled when the supercapcitor voltage is below 2 V.
2. The software must disable all isolated gate drivers when in safe state.	2. Connect a power supply configured to output 4.3 V in place of one module. Measure with a multimeter that the enable digital output from the microcontroller is disabled. Perform the same procedure for a 2.4 V input.
3. The software must be able to identify modules above and below pack average and generate PWM signals to drive the redistribution of charge such that the identified modules approach pack average.	3. Provide voltage readings with a voltage source such that one module is above average and one is below average. With an oscilloscope, probe the output signals. Verify that PWM signals are generated for the high and low modules.

2.3 Balancing Unit

There is one balancing unit per module. The function of the balancing unit is to transfer energy in either direction across the converter between the supercapacitor bus and battery module. The PWM control responsible for setting the conversion from module to bus is received from the balancing control.

2.3.1 Isolated, Bidirectional DC/DC converter

The DC/DC converter implements an isolated flyback topology with synchronous switching. The secondary side voltage will be between 2.5 V and 4.2 V. The primary voltage will be nominally set at the pack average voltage. See Figure 6 for a schematic implementation used for simulation.

Requirement	Verification
1. Converter must be able to sink or source at least 3 A of current on the secondary side.	1.1. Connect a power supply at 3 V to the supercapacitor side of the converter and a 1 Ω power resistor to the module side. Attach a function generator set to a 250 kHz 0-3.3 V PWM wave to the gate drive circuit. Also connect a Yokogawa power meter to measure output voltage and current into the load resistor. 1.2. Ramp up the duty cycle of PWM signal and measure output RMS voltage and current on the load using a Yokogawa power meter. Ensure that RMS output current reaches 3 A on the load and the converter remains functional at this current draw for at least 1 minute.
2. Converter must have an adjustable input and output range of 2.5-4.2 V.	2.1. With a function generator, create an input supply of 4.2 V. With a multimeter measure the output voltage and adjust the input duty cycle until the output voltage is 2.5 V. 2.2. While changing the PWM duty cycle on the function generator to keep output voltage at 2.5 V, lower the input voltage to 2.5 V. 2.3. Keep the supply voltage constant and adjust duty cycle until the output voltage is 4.2 V. 2.4. Increase the supply voltage to 4.2 V while using the duty cycle to maintain a 4.2 V output.
3. Converter must be capable of bidirectional power transfer.	3. Turn off the supply move the power supply to the module side of the transformer and the load resistor to the secondary side. Repeat the above verifications with input and output reversed.

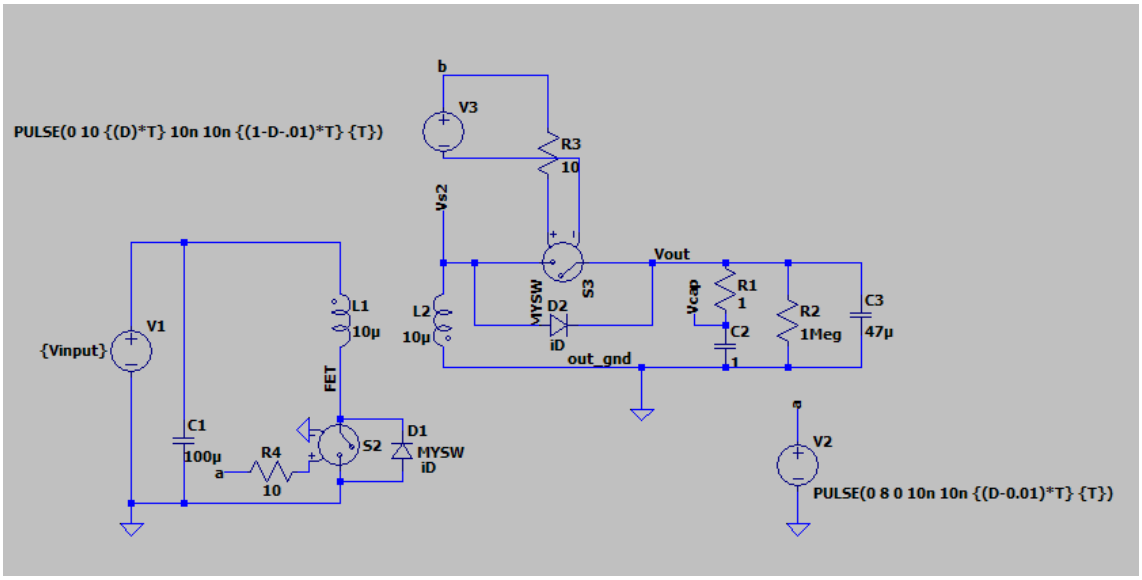


Figure 6: Schematic for simulating synchronous flyback converter using ideal switches and diodes

2.3.2 Isolated Gate Driver

The isolated gate driver is required for the balancing unit because the each battery module is isolated from the control logic and the gate drives for a power MOSFET require large currents, which cannot be supplied from a microcontroller. The primary-side gate drive is powered from the 12 V external supply while the secondary-side gate drive is powered from a battery module. To minimize the number of signals from the microcontroller, the isolated gate driver IC should also implement inversion and deadtime.

Requirements	Verification
1. Gate driver must transfer a logic side PWM to the primary drive pin output and an inverted signal with deadtime to the secondary drive pin output.	1. Supply logic power at 3.3 V and power each gate drive at 3.5 V using a power supply. Apply a PWM input to the logic side and probe the voltage on each gate drive pin using a differential oscilloscope probe. Ensure that the duty cycle for the input and primary-output are the same and that the secondary-side drive is inverted.

2.4 Charge Storage

The function of this subsystem is to store charge from the modules of higher voltage to be redistributed back to the modules of lower voltage.

2.4.1 Supercapacitor

The supercapacitor will store and release charge to enable the redistribution of charge between any sets of modules. The supercapacitor will also regulate the voltage on the shared primary power bus. The voltage rating of the supercapacitor must be greater than 4.2 V.

2.4.2 Precharge

On start-up, the supercapacitor can be susceptible to initial current spikes which can damage the system components. While it is possible to limit the current inrush using the control loop, a simple hardware solution is to use a precharge circuit. This circuit will consist of a power resistor that is temporarily connected in series with the supercapacitor to limit the inrush current upon startup. Once the circuit voltage steadies, the power resistor will be disconnected and the precharging will be complete.

Requirements	Verification
1. Precharge circuit must limit inrush current to at most 10 A, beyond which the transformer is likely to saturate.	1.1. Connect a power supply to the input of the precharge circuit and the supercapacitor to the output. Set up current measurement using an oscilloscope on the supercapacitor power supply input leads. Ensure that the supply current limit is at least 10 A. 1.2. Step up the supply voltage to 4.2 V. Confirm that current on input does not exceed 10 A as measured on the oscilloscope.

2.5 Battery Management System

The Battery Management System (BMS) queries all peripheral hardware to ensure that the batteries are operating within specifications outlined in the datasheet. This includes voltage, temperature, and current sensing within the car. In the event that unsafe operation is detected, the BMS will isolate the batteries from the load and disable any balancing from occurring. The BMS is out of scope for our project but it will be used to monitor cell voltages and to send that data to the Balancing Control PCB via CAN.

2.6 Test Setup Environment

The Test Setup is out of scope of this project but will be used to supply 12 V power to the Balancing Control PCB and 12 V power to the isolated gate drivers.

2.7 Battery Modules

The battery modules are out of the scope of this project. We will be using four modules in series of 3 parallel cells each to conduct testing and verification of our proof-of-concept design. These cells will be 18650 lithium-ion battery cells.

2.8 Tolerance Analysis

The essential feature of our design is a bidirectional flyback converter. A bidirectional converter is one of the unique advantages of our custom architecture in that it will allow any module to charge or discharge into any other module. The bidirectional flyback topology is shown with ideal components in Figure 6. There are three main requirements for the flyback converter: 1) It must have a 2.5 to 4.2 V adjustable input range and a 2.5 to 4.2 V adjustable output range. 2) The converter must be able to handle at least 3 A of

current input or output. 3) The converter must be capable of bidirectional operation. It is critical that even including tolerances the flyback convert module meets the requirements.

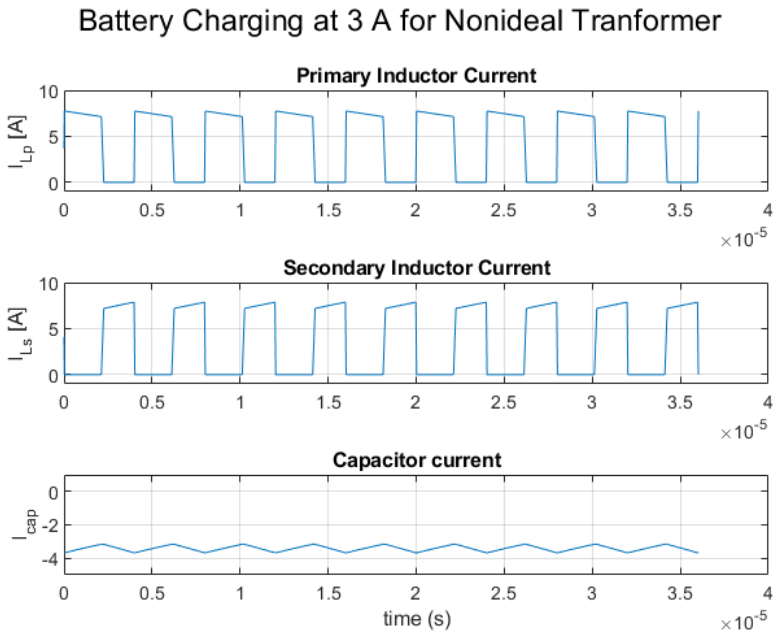
The primary components in the flyback converter are the transformer, the primary-side switch, and the secondary-side switch. To ensure proper operation of the flyback converter, we performed simulations using the worst-case tolerances for each of these real components. The PA6605-AL from CoilCraft is an off-the-shelf transformer that is rated for 12 V and 60 W with a saturation current of 12.5 A. The nonidealities of the transformer are its leakage inductance, copper losses, and core losses. The CoilCraft transformer has a maximum total leakage inductance of 0.13 μH and a maximum DC resistance of 4.7 mΩ per winding. No core losses are specified in the datasheet, so we will use the simplified model that ignores core losses. The transformer also has a magnetizing inductance of at least 9 μH referred to the primary. This inductance is utilized as part of the converter energy transfer process, so a large magnetizing inductance is ideal [4].

The synchronous flyback design requires active switches on both the primary and secondary side of the transformer. The selected MOSFET, an ON Semi NVTFS5C478NL, is rated for 40 V and 26 A. It also has a gate charge of 2 nC and a maximum R_{ds},on of 45 mΩ [5]. The last tolerance to consider is the derating and equivalent series resistance of the two filtering capacitors on the input and output. The chosen capacitors are 100 μF, with an ESR of 74 mΩ and a tolerance of 20%. Thus, in a worst-case each capacitor is only 80 μF instead of its desired 100 μF. The goal is to show that within these specifications, the converter can still operate at maximum power without exceeding the transformer saturation limit of 12.5 A or the switch blocking limit of 40 V. Operation was simulated in two scenarios worst-case scenarios: 1) The supercapacitor at 4.2 V is charging an undercharged module at 2.5 V. 2) A 4.2 V module is charging the supercapacitor at 2.5 V. In both simulation cases, the current was set to approximately 3 A by changing the duty cycle.

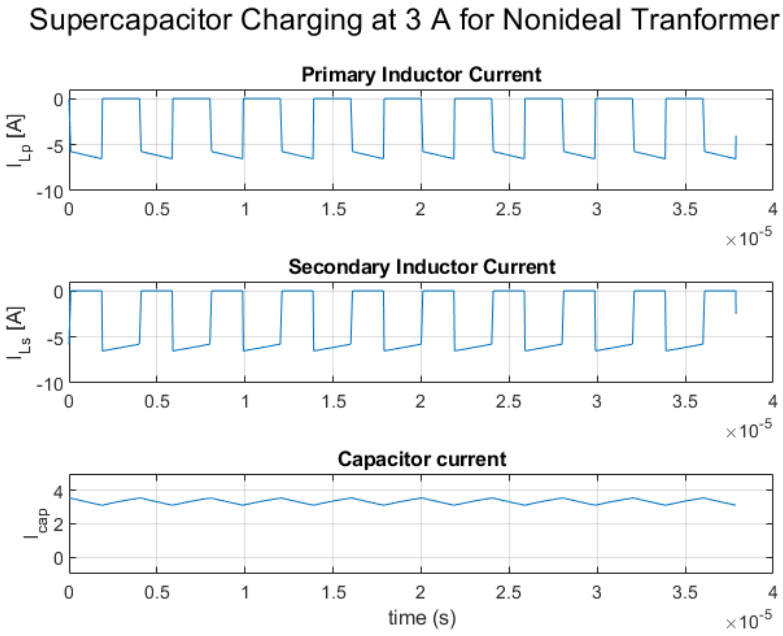
Mathematical derivations of the flyback operation become unrealistically complex when accounting for all real components, so we verified operation using LTSpice simulation software. Figure 7 simulates the operation of the circuit using a real inductor model and ideal switches. The results from this figure show that without considering the real switches and capacitors, the transformer tolerance will still yield a product well within specifications.

Next, the real switches and capacitors were included in the simulation. Figure 8 shows the complete converter simulation with worst-case tolerances. The simulation results for full-current charge and discharge is shown in Figure 9. The results of the simulation show that, the inductor currents do not exceed saturation limits. The peak inductor current was approximately 8.5 A, and the rms current was 3.4 A in both simulations. Furthermore, the maximum gate voltage due to ringing is 30 V, which does not exceed the MOSFET rating of 40 V. Thus, the converter can still operate within specifications given worst-case tolerances.

In the process of this analysis, we gained additional insight into the large ringing a flyback topology induces on the MOSFET drains. We will take care to design the circuit board layout to avoid parasitic inductance that can induce more ringing. In further analysis we plan to analyze snubber options to reduce this ringing including a resistor-capacitor-diode clamp circuit, or a zener clamp circuit.



(a) A 4.2 V supercapacitor charging a 2.5 V battery at approximately 3 A



(b) A supercapacitor at 2.5 V discharges a 4.2 V modules at approximately 3 A

Figure 7: Simulation results of for peak inductor current and capacitor charging current for a non-ideal transformer

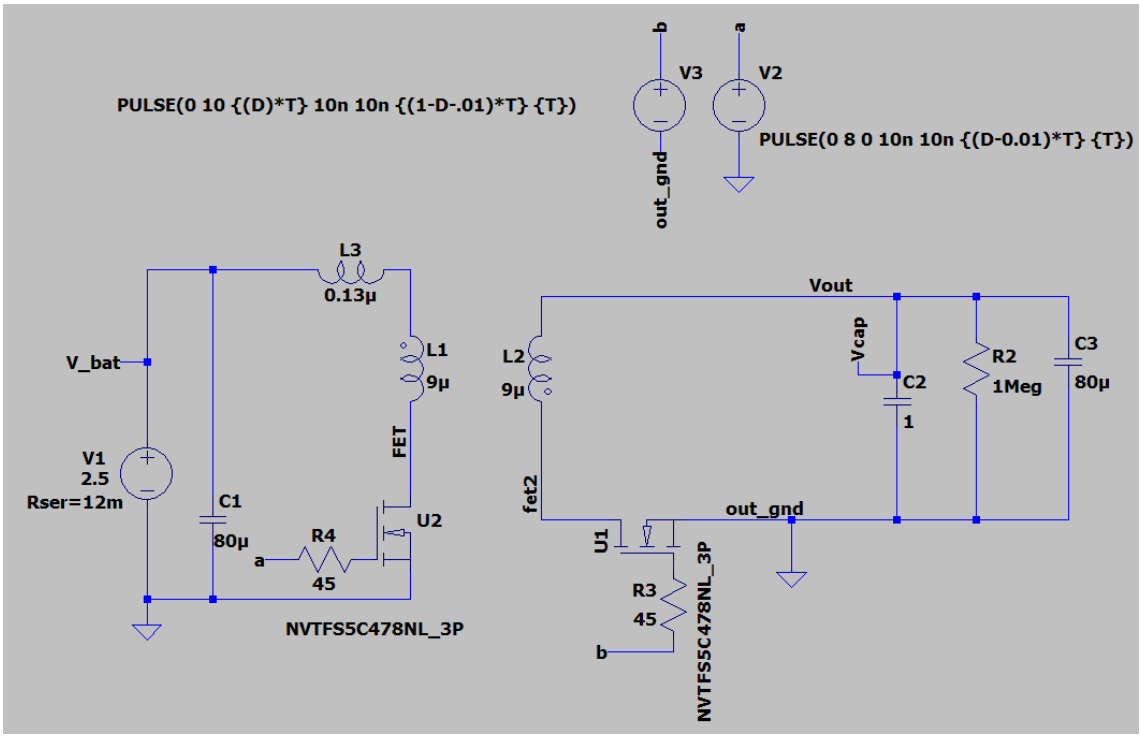
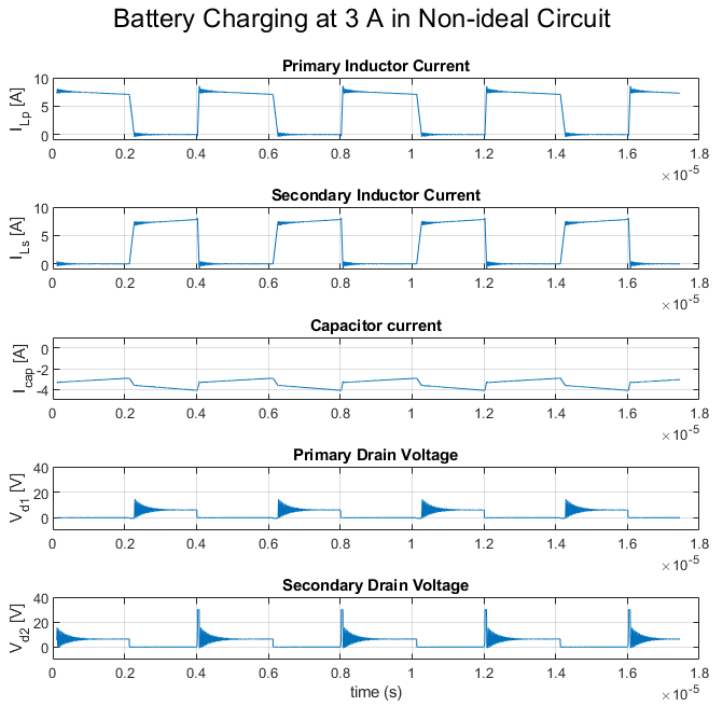
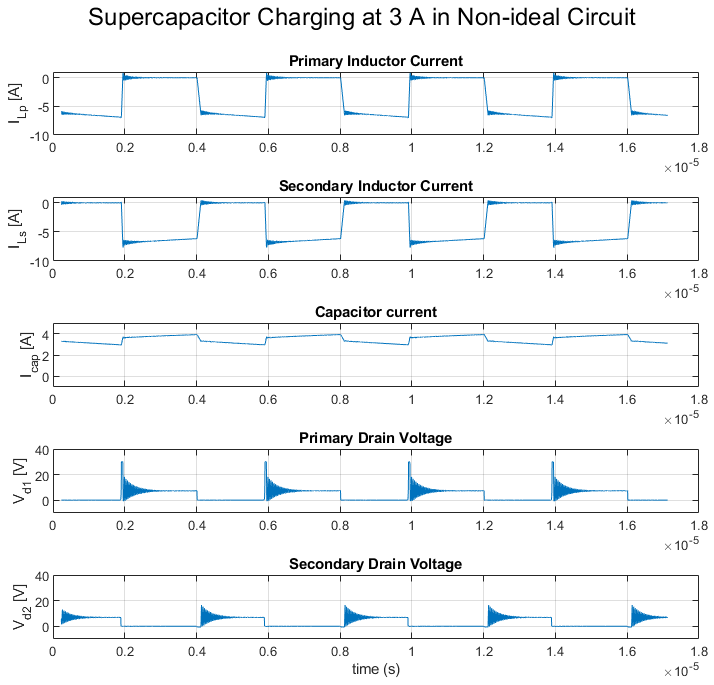


Figure 8: Schematic for simulating synchronous flyback converter with real components at worst-case tolerances. Note: series resistances are not shown because they are set within the properties of each component



(a) A 4.2 V supercapacitor charging a 2.5 V battery at approximately 3 A



(b) A supercapacitor at 2.5 V discharges a 4.2 V module at approximately 3 A

Figure 9: Simulation results of for peak inductor current, capacitor charging current, and drain blocking voltage for a non-ideal circuit

3 Cost and Schedule

3.1 Cost

We estimate 20 hours of work per week for 3 people over 15 weeks at $ 50 per hour. With 2.5 times overhead, we estimate a total development cost of $ 112,500 for this proof-of-concept design.

To build the devices we estimate a total cost of $ 230.19 with the cost breakdown shown in Table 1. Note that the components shown in the cost breakdown are derived on current preliminary part selection and are subject to change. If our design were to be produced in bulk, we estimate a total cost of $ 138.01.

Table 1: Cost breakdown of required components

Part	**Part Number**	**Unit Price**	**Qty**	**Total**	**Bulk Cost**
Microcontroller	LPC1549	$ 9.62	1	$ 9.62	$ 4.15
3 V Regulator	R-783.3-1.0	$ 7.08	1	$ 7.08	$ 5.77
CAN Transceiver	ISO1042DWVR	$ 3.94	1	$ 3.94	$ 2.00
Supercapacitor	DGH255Q5R5	$ 3.05	1	$ 3.05	$ 1.55
Isolated Gate Driver IC	Si8274	$ 2.40	4	$ 9.60	$ 8.58
Transformer	PA6605-AL	$ 16.95	4	$ 67.80	$ 42.70
Power MOSFET	NVTFS5C478NL	$ 1.00	8	$ 8.00	$ 2.16
Electrolytic Capacitors	DGH255Q5R5	$ 3.05	2	$ 6.10	$ 3.10
Lithium-Ion Battery	18650 GA	$ 5.00	12	$ 60.00	$ 55.20
Passive Components	n/a	$ 0.10	100	$ 10.00	$ 2.00
Connectors	Molex KK series	$ 1.00	15	$ 15.00	$ 8.80
PCB Manufacture	n/a	$ 30.00	1	$ 30.00	$ 2.00
			Total Cost	$ 230.19	$ 138.01

In total, development and component costs sum to an overall project cost of $ 112,730.19. This overall cost would be reduced should our design be produced in bulk.

3.2 Schedule

Our project schedule is broken down by group member as follows.

Table 2: Schedule overview of all project team members broken down by week

Week	Tara D'Souza	John Han	Rohan Kamatar
3/8	Design balancing control schematic	Create high-level design for software to generate PWM signals for balancing control	Design balancing unit schematic
3/15	Design balancing control PCB layout	Spot weld batteries into modules for testing, cycle battery modules	Design balancing unit PCB layout
3/22	Finalize and order PCB components	Program PWM control	Program PWM control
3/29	Conduct basic testing for balancing control PCB , make appropriate revisions	Assist with PCB assembly and testing	Conduct basic testing for balancing unit PCB, make appropriate revisions
4/5	Complete second revision of balancing control PCB and send for manufacturing	Program Balancing algorithm and additional diagnostics	Complete second revision of balancing unit PCB and send for manufacturing
4/12	Perform complete assembly and hardware testing of balancing control PCB	Perform full system testing with software	Perform complete assembly and hardware testing of balancing unit PCB
4/19	Conduct full system testing	Conduct full system testing	Conduct full system testing
4/26	Final Demonstration	Final Demonstration	Final Demonstration
5/3	Final Paper	Final Paper	Final Presentation

4 Ethics and Safety

This project will deal with two significant dangers: high-voltage electronics and lithium-ion batteries. High-voltage electronics pose a danger of electric shock. At higher voltages greater current can flow through the body, delivering more power and therefore an increased risk of injury and death [6]. We will minimize this risk by utilizing the one hand technique and always utilizing proper tools and safety equipment.

Lithium-ion batteries pose a significant risk due to their high energy density and instability. In a 5 year period over 25,000 overheating and fire incidents involving lithium ion batteries were reported. However, this risk is only significant when the batteries are damaged or utilized outside of their specified operating conditions [7]. The safe operation of lithium-ion batteries is well defined by the American Solar Challenge regulations [8] under which ISC designs its vehicles. These regulations require active protection of overvoltage, undervoltage, over current and over temperature where active protection means that the system will shut off automatically in any of the above fault conditions. The team will implement these systems and verify them before relying on them to provide protection.

While working with these dangers it is also important to minimize danger and risk to the public. The IEEE Code of Ethics states that it is our responsibility "to hold paramount the safety, health, and welfare of the public"[9]. We will ensure this through safe storage of our batteries, isolation of high voltage, and clear labeling of enclosures to protect the public from the dangers of our project. Our batteries will be stored in a fire cabinet while not in use and will always be stored at safe charge levels. Additionally, the battery pack will only be operated under supervision of our team members.

Should an accident occur during assembly or otherwise, the team will follow Division of Research Safety guidelines [10]. This includes always being prepared with proper safety equipment such as fire extinguishers and sand. The risk of thermal runaway of damaged batteries can also be mitigated through discharge in a saltwater solution. If a battery is damaged we will follow DRS procedures for disposal by placing the battery in a saltwater solution to discharge and contacting the DRS for proper disposal.

While high voltage batteries can be dangerous, with proper procedures and design, these risks can be mitigated which will allow us to create a safe and functional system.

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