Low-Cost Integrated Spectrometer

Design Document Check

Group: 18 –

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1 Introduction

1.1 Objective

For three centuries, optical spectrometers have played instrumental roles in advancing nearly all branches of science, from discovering new elements, determining the composition of stars, or even identifying and characterization of Two-Dimensional materials [1, 2, 3]. Given the technology's maturity, modern-day spectrometers have evolved since their initial conception, collecting and quantifying their data for instant analysis. However, budget digital spectrometers, including their required software, start at over $1000 [4]. This cost barrier effectively limits spectrometry techniques to controlled laboratory environments in Universities and other research institutions.

We aim to bring the cost of the digital optical spectrometer, lowering the barrier of entry and extending the applications of spectrometry. A spectrometer's cost lies in its expensive optics and dedicated high-frequency data collection hardware. Our proposed solution is to eliminate costly optical components by integrating an optical circuit in acrylic plastic and collecting the diffracted light using a linear CCD image sensor driven by a low-cost microcontroller.

1.2 Background

Integrated Photonic Spectrometers (IPSs) are a well-studied subject, fabricated in various materials and geometries; however, such literature presents narrow and novel applications of the IPS like broadband single-photon spectrometers, while commercial devices start at over $350 for the sensor alone [5, 6, 7, 8]. Additionally, several open-source projects demonstrate digital spectrometers built with the Arduino framework but are limited in that capturing a single data frame takes 4 seconds over the 8-bit microcontroller's 115.2 Kbaud USB-UART connection [9].

1.3 High-Level Requirements

- The spectrometer's optics should be capable of resolving the plasma emission spectra of common gasses, such as argon.

- The spectrometer must be capable of live plotting and capturing data with a refresh rate of at least 10 hz.

- We must present a novel fabrication technique for a PMMA-based spectrometer to enable manufacturing at a significantly lower cost than current alternatives.
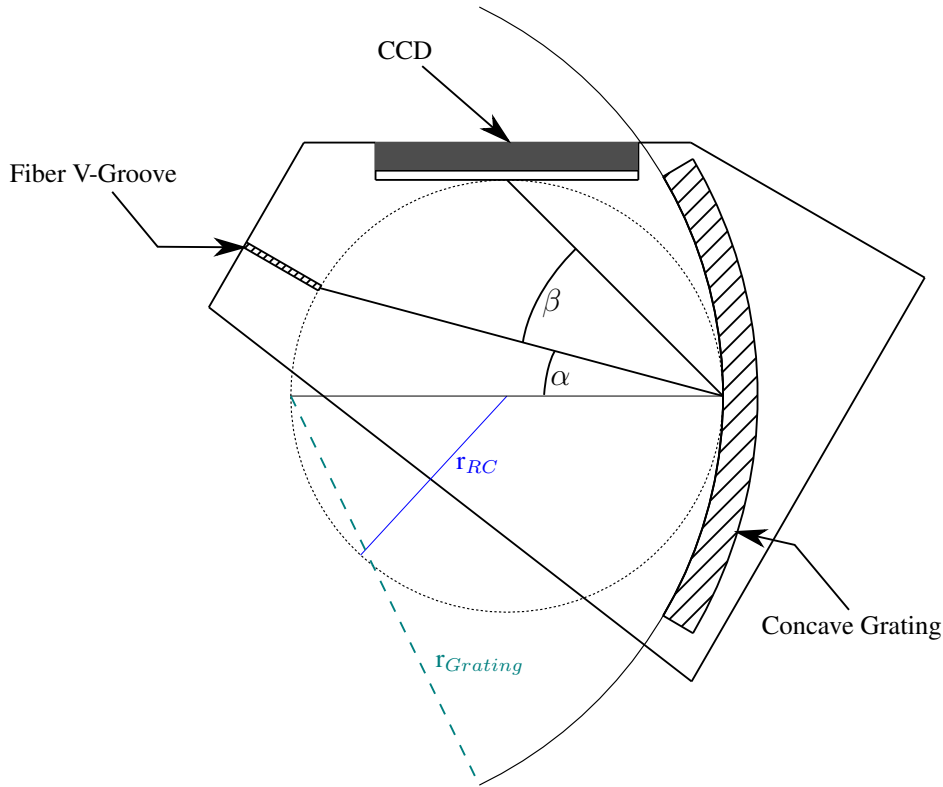
Figure 1. Spectrometer grating configuration. The grating lies on a circle of radius $r_{Grating} = 2r_{RC}$, which is tangent to the Rowland Circle. The Rowland pole is the tangent point between these two circles, angles are defined from the line normal to the pole

2   Design

2.1   Physical Design

Figure 2, The physical design of the spectrometer isolates the light sensitive hardware from the environment. Additionally, the optical feedthrough allows our spectrometer to connect to external optical fibers and instruments. The photonics are located off-center to allow for the ESP chip and its accompanying electronics. Also shown is the photonic slab mounted to the CCD. Figure 3 shows the photonics package relative to the CCD. Angular measurements follow the work of P. Pottier and M. Packirisamy, while other dimensions are maximized to accommodate the package [10].

The spectrometer design in Figure 4 requires three primary modules to fulfill the above requirements. The photonics demodulate light inbound through a coupled optical fiber, as in Figure 5 and the outbound light is coupled into waveguides carrying a given spectral band. By using a three-dollar microcontroller, the ESP32, we satisfy the remaining requirements, as it overcomes the communication bottleneck of the Arduino's USB-UART connection through

WiFi. Additionally, with its two 240 MHz cores, the tasks of data acquisition and serving data to the user are split amongst the cores.
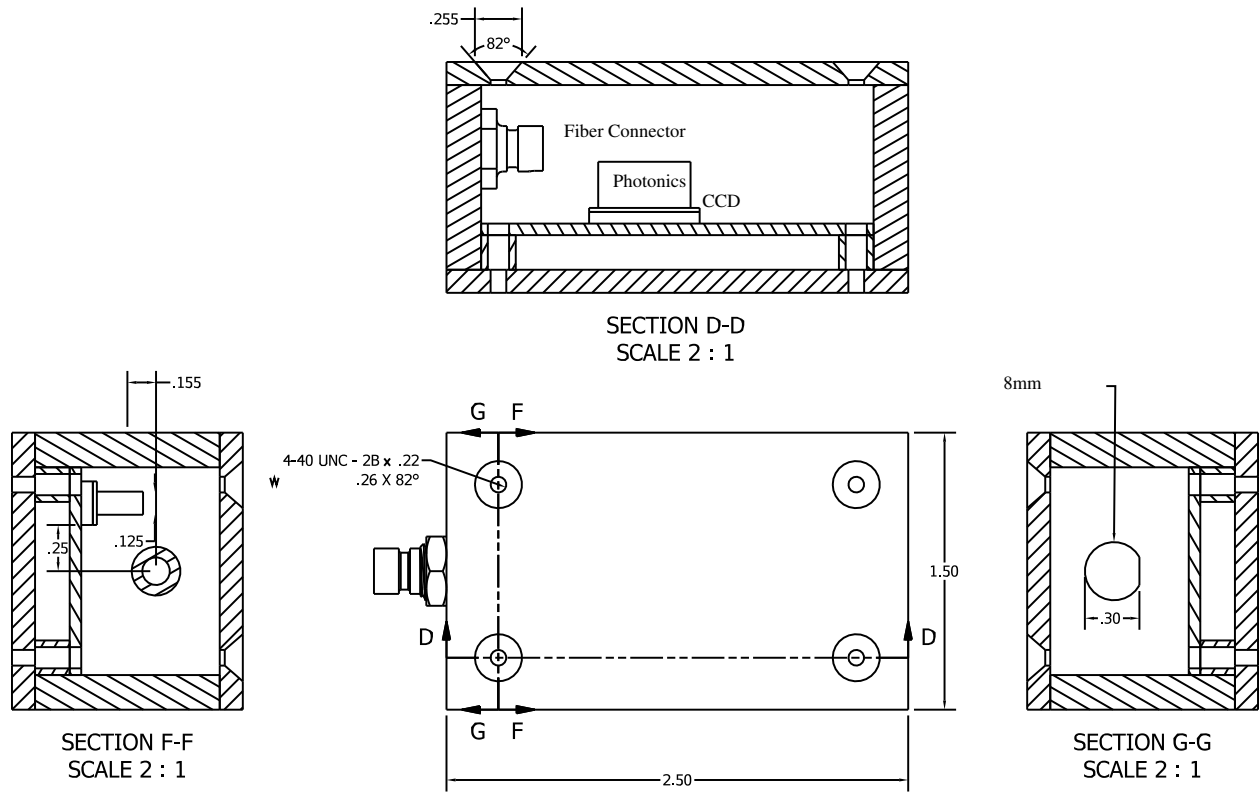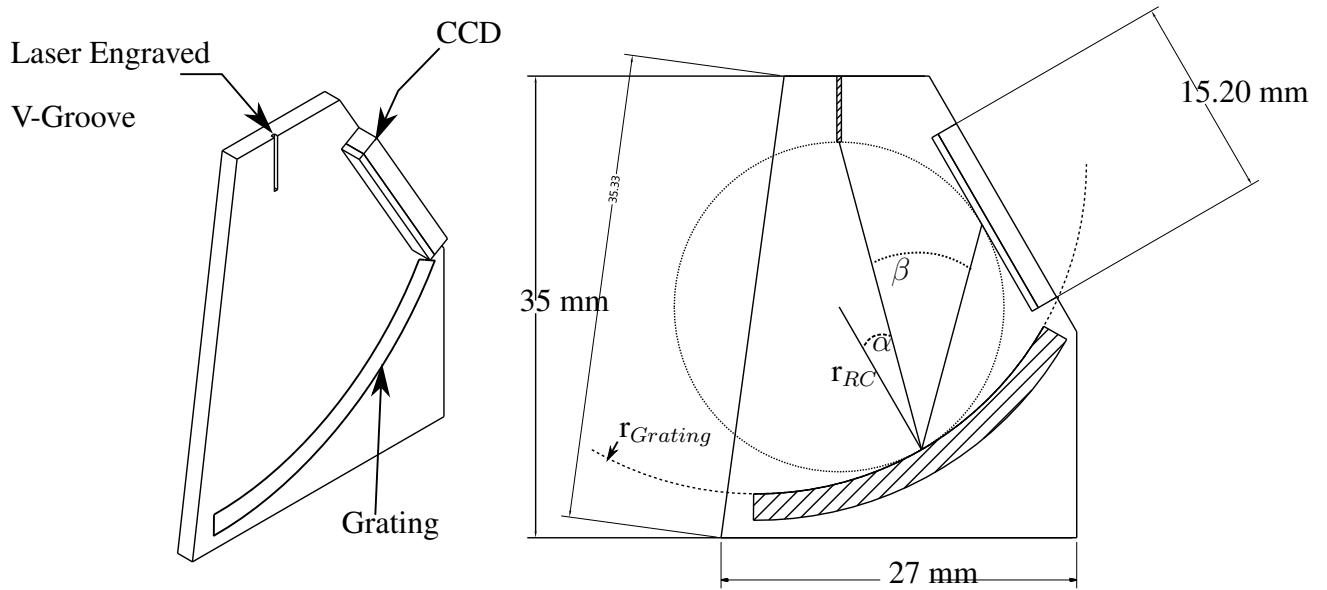

Figure 2. Spectrometer housing.

Figure 3. Photonics Schematic $\alpha = -15°$, $\beta = -45°$, and other dimensions scale to accommodate r_{RC}.

Low-Cost Integrated Spectrometer

Photonics

Optical Fiber

Echelle Diffraction Grating

Slab Waveguide

Data Acquisition

Diffracted Light

CCD

Analog Signal

Analog Supply

Digital Supply

ADC

MCLK

SPI

Microcontroller Core 0

Server

Microcontroller Core 1

Data Stream

Asynchronous Web Server

Web Socket

Captive DNS Portal

Soft Access Point

Client

Plotting Script

Connection Request

Power Supply

5v USB
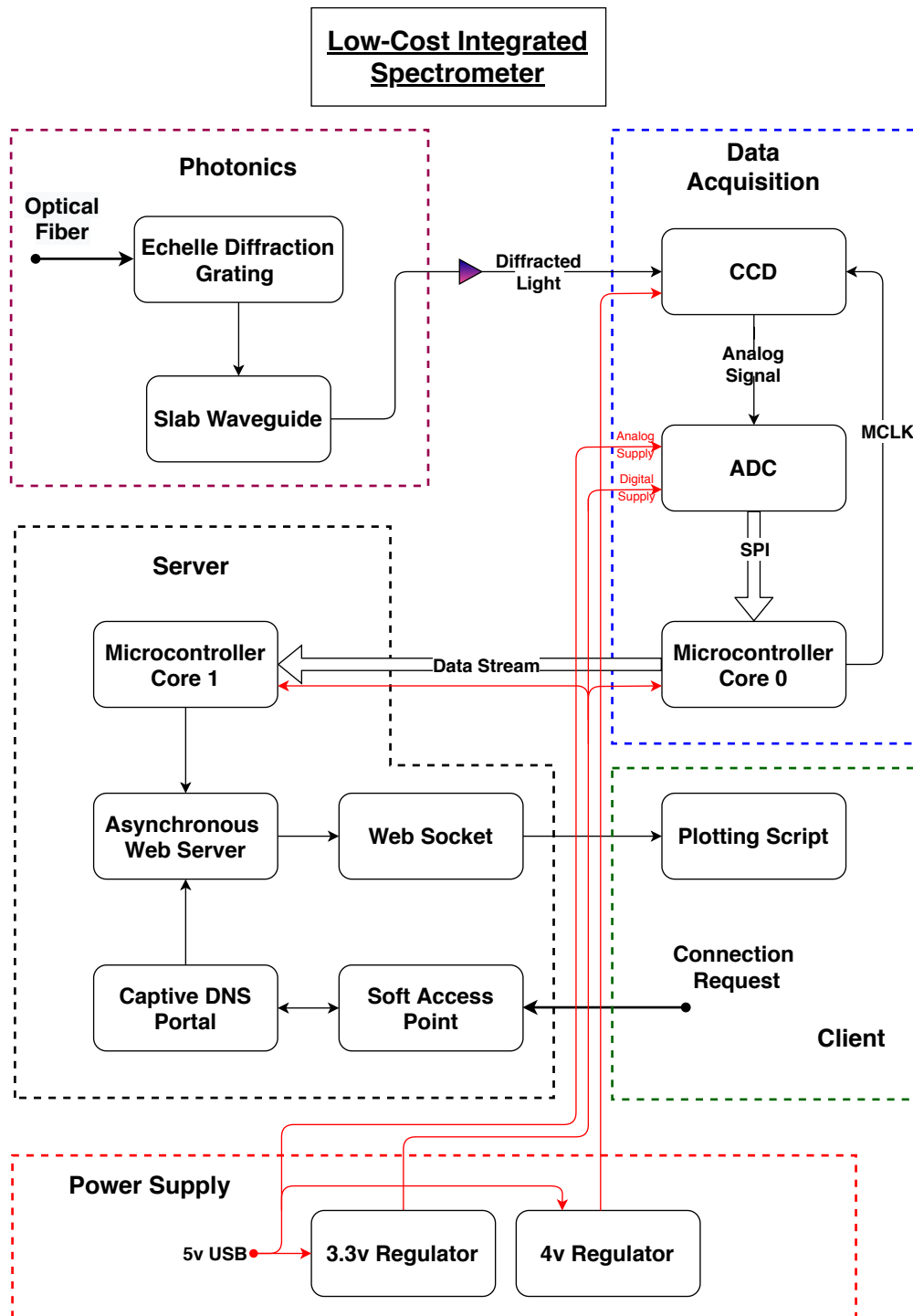
3.3v Regulator

4v Regulator

Figure 4. High-Level Block Diagram

2.2 Photonics

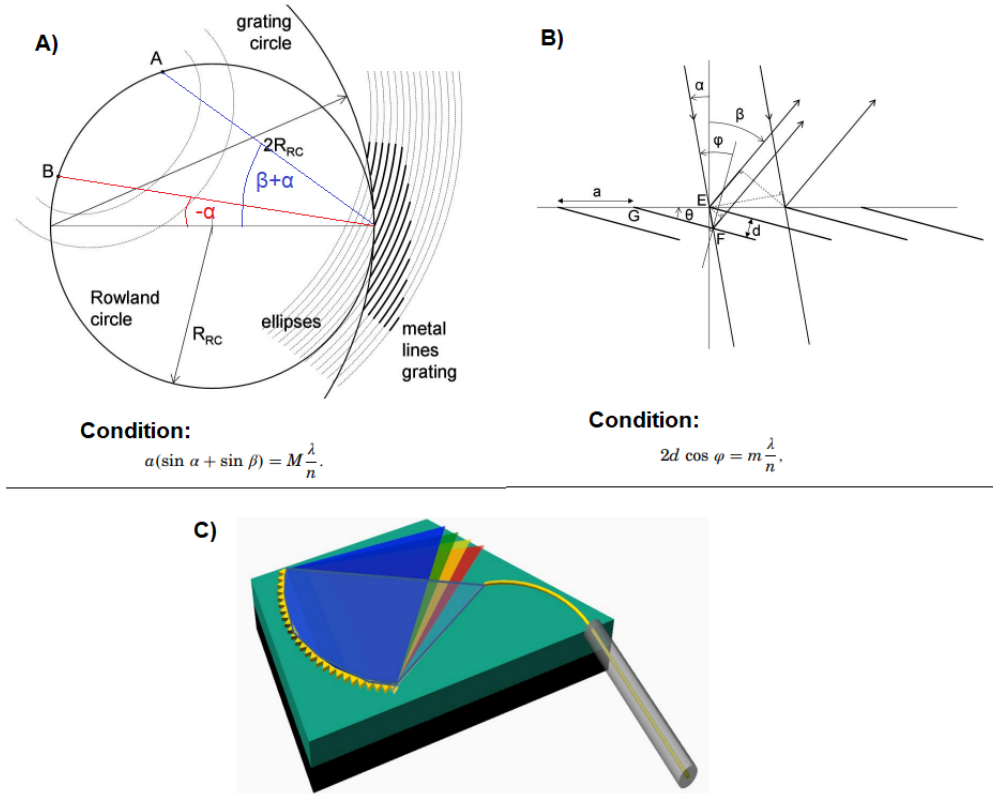### 2.2.1 Concave Blazed Diffraction Grating

Figure 5. Integrated Spectrometer geometrical constraints from P. Pottier et al. [6]. Subfigure A shows the general diffraction condition for a Rowland defined grating. Subfigure B shows the second, Bragg, diffraction condition of the elliptical grating. Subfigure C shows the device layout, the combined diffraction condition ensures only one output order [6, 11]

Different wavelengths of light will need to be physically separated. We plan to accomplish this by using an Concave Blazed grating, as in Figure 5. Our design's constraints demand a larger feature size than that of detailed by P Potter et al, since MNTL's Heidelberg mla150 has a feature size of 600 nm.

Equation 1 describes the general diffraction condition for the Rowland mounted grating; $\lambda_{blazing} = 600$ nm is the center wavelength for our detection band, M is the diffraction order, $\eta_{eff} = 1.5$, and $\sin\alpha$ and $\sin\beta$ are the input and output pole-angles respectively [12]. To meet the 600 nm feature size, $M \geq 2$, and in general a larger M implies a

larger device.

$$a(\sin\alpha + \sin\beta) = M\frac{\lambda_{blazing}}{\eta_{eff}}$$

$$a = M\frac{\lambda_{blazing}}{\eta_{eff}(\sin\alpha + \sin\beta)} \tag{1}$$

Equation 2 represents the blazing conditions of a two-material Distributed Bragg Reflector (DBR) system [12]. The chosen system is PMMA/air, $\eta_{eff} = 1.5$ and $\eta_2 = 1$, which is identical to the index of refraction differential of Pottier et al. Equation 3 describes the condition for the DBR's maximum reflectively, although such constraints can be relaxed if $d_2 \ll d$ [10, 12].

$$d = -a\sin\frac{\alpha + \beta}{2} = d_1 + d_2 \tag{2}$$

Given $\phi = \dfrac{\alpha - \beta}{2}$, and $\eta_{eff}\sin\phi = \eta_2\sin\phi_2$

$$d1 = \frac{(2k_1 + 1)\lambda}{4\eta_{eff}\cos\phi}, \text{ where } k_1 \in \mathbb{Z}$$

$$d2 = \frac{(2k_2 + 1)\lambda}{4\eta_2\cos\phi_2}, \text{ where } k_2 \in \mathbb{Z} \tag{3}$$

Equation 4 represents the Free Spectral Range (FSR), $\Delta\lambda$, or the maximum bandwidth of the detection region [13]. For our system $\Delta\lambda|_{M=2} = 525$ nm and $\Delta\lambda|_{M=3} = 333$ nm, in general as the bandwidth goes down the resolving power of our grating goes up. With these parameters, we can tune the wavelength response band and resolution within that band.

$$\Delta\lambda = \frac{\lambda_{blazing}}{M}(1 - \frac{M+1}{M}(1 - \frac{\eta_{eff}}{\eta_2})) \tag{4}$$
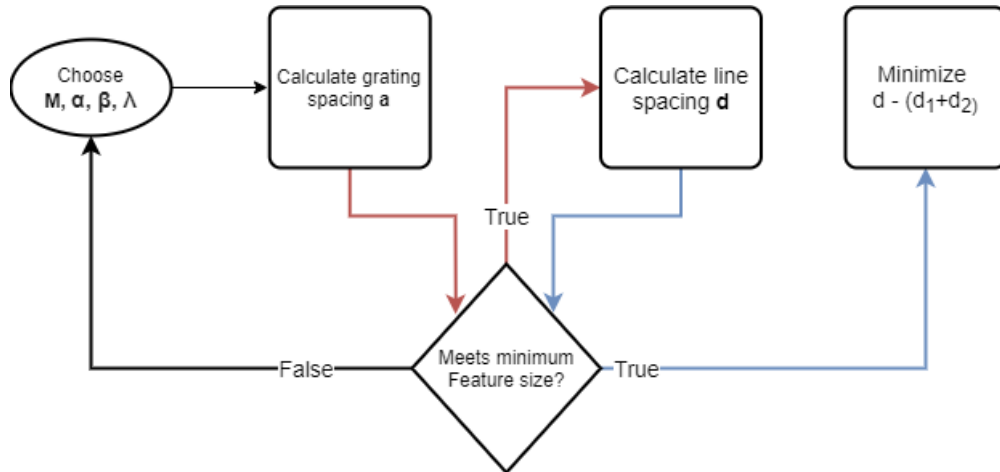

Figure 6. Diffraction Grating Design Flow-Chart

2.2.2 Slab Waveguide

An optical fiber must couple light into the acrylic. For this we propose a laser-engraved v-groove mounting, coupled via epoxy to an acrylic slab waveguide. The waveguide confines light within two dimensions and directs it to the CCD. Our fabrication should exceed a 10 micron etch depth to ensure multimodal transport.

2.3 Data Acquisition

2.3.1 CCD

Detects and measures the intensity of light on each pixel. The array of pixels allows us to resolve the output spectrum spatially. The CCD integrates the output spectrum with time, to prevent overexposure, it must be refreshed at a high rate, 1-2 MSPS. We propose using the TCD1103GF from Toshiba for its standard interface, low-cost, and 3.3V compatibility.

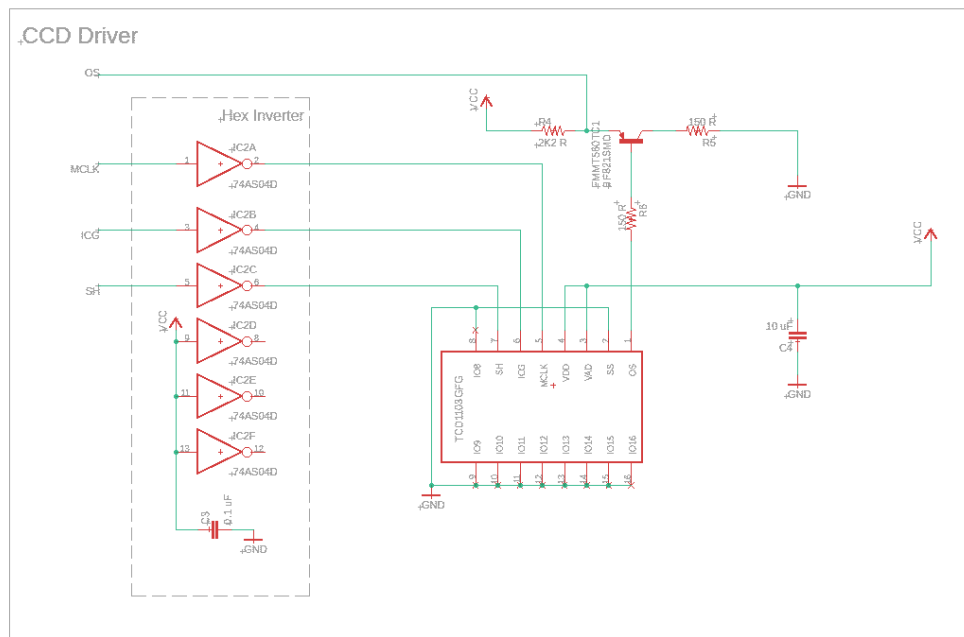*Requirement: Must drive the MCLK at 2-4 MHz.*

Figure 7. CCD Driver Schematic

2.3.2 ADC

The The ADC converts the CCD's analog readings to digital data for the ESP32. To match the CCD's speed the ADC must be compatible with the ESP's fastest serial communication standard SPI, and offer atleast 2 MSPS.
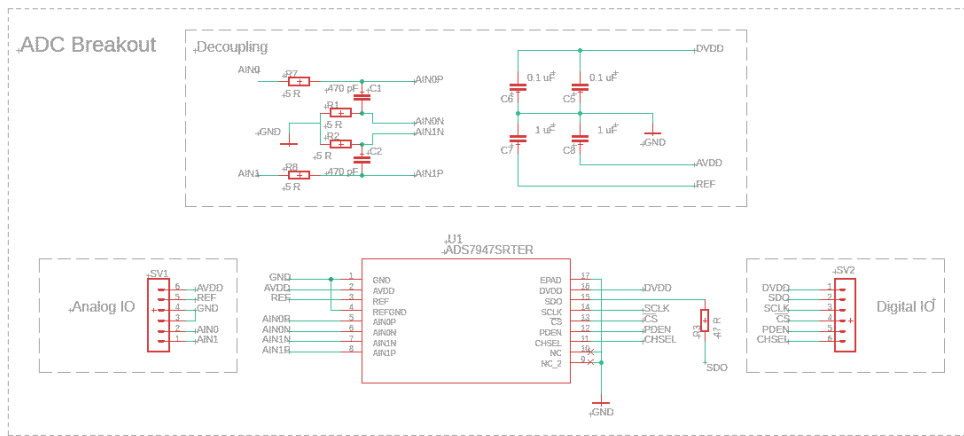
Figure 8. ADC Device Schematic

2.3.3 Microcontroller Core 0

At a high level, the ESP32 SOC is configured with two tasks. Initially, we configure the platform's 16 peripheral timers, capable of a maximum of 40 MHz, to generate the necessary clock signals signal. Then, the task of monitoring the board hardware communicates with the ADC over SPI. Incoming data is streamed to the second core, which hosts an asynchronous web server.

2.4 Server

The server will comprise an ESP32 hosting a network access point where the intended user can connect and log on to view their data in a web browser. The implementation of the server is beyond the scope of this class; however, the general requirements of each components are listed below.

2.4.1 Microcontroller Core 1

This Microcontroller asynchronously communicates to its WiFi IC and the other core. Additionally it hosts our web server with a complementary file-system.

Requirement: Cannot bottleneck the 10 frames-per-second required above.

2.4.2 Asynchronous Web Server

Requirement: Must serve the plotting script, and establish a websocket connection.

2.4.3   Web Socket

Connects to the user's plotting script to stream the spectrum's data. The async server host's the websocket, and connects the user to it.

Requirement: Must connect to the user's plotting script and stream the data atleast 30kbps.

2.4.4   Captive DNS Portal

Requirement: Must immediately forward anyone connecting to our network to a webpage with our plotting script.

2.5   Soft Access Point

Requirement: Must allow users to connect by joining the WiFi network.

2.5.1   Plotting Script

Requirement: Defines a set of API functions which receive data from the microcontroller and forward them to a JavaScript plotting API [14].

2.6   Risk Analysis

The most challenging component to design will likely be the photonic circuit. The diffraction grating's geometrical constraints have only been proven for a simple concave blazed grating, whose effieciency has been simulated at less than 39% [10, 12, 6]. The same work demonstrates using Bragg reflectors to produce Mono-Order diffraction gratings at greater than 99% efficiency.

The grating also challenges the fabrication process; we must maximize reflectively, while performing a high aspect ratio etch. We must tune our UV exposure and development time to reach our desired aspect ratio, and optimize our grating geometry. If the etch is not consistent throughout, our calculated path-length differences no longer hold and our grating will fail.

3 Requirements and Verification

3.1 Diffraction Grating [40 Points]

Requirement	Verification
Must diffract light within the range of 400-800 nm	(a) Place grating inside nanolab's quantum efficiency (QE) measurement system, between the Monochromator and CCD. (b) Sweep input wavelengths across the specified range, record the output diffraction order's position on the CCD as a function of wavelength. (c) Ensure our grating geometry supports a single high-order diffraction order, and that the output range falls within the detector length. (d) Compare input and output optical power across full band to calculate efficiency

3.2 Slab Waveguide [10 Points]

Requirement	Verification
The slab's thickness must exceed 10 microns.	(a) Record the time spent developing the diffraction grating. (b) Depth measurements at this feature-size are possible with the nanolab's Keyence VWX microscope's 3D imaging. (c) If etch depth is too shallow, increase development time.

3.3 Data Acquisition [20 Points]

Requirement	Verification
Must sample at a rate of 1-2 MSPS	(a) Establish SPI communication with the ADC (b) Generate a 0.5-1 MHZ sine wave with a function generator. (c) The data rate out of the CCD must be the same as the ADC, 1-2 MSPS, by the nyquist condition the ADC should reconstruct the signal. (d) Run SPI communication between ADC and CCD and ensure 10 Hz polling rate.

3.4 Microcontroller [30 Points]

Requirements	Verification

1. Must generate multiple 1-4 MHz clock signals for driving the CCD
 	
2. SPI communication must support atleast 10 full 1500-pixel frames each second (30kbps)
	1. (a) Configure the ESP to PWM 0-40 MHz on all clock related GPIO.
	    (b) Confirm all clock pins can output atleast their respective maximum frequencies with an oscilloscope.
	
	2. (a) Establish SPI communication with the ADC
	    (b) Generate a 500 KHz sine wave with a function generator.
	    (c) As before, if the microcontroller reconstructs the signal, the data-rate exceeds 30 Kbps.

4 Cost and Schedule

4.1 Cost Analysis

We estimate the hourly rate at approximately $42/hr using Engineering Illinois's calculated $84,250 for the year 2014-2015. The number of hours each of us spend per week will vary throughout the semester, but we estimate 10hrs/wk average for the three of us and be able to complete the prototype design within the 16 week semester, Equation 5 . Additionally, Equation 6, we estimate our cleanroom costs using UIUC's MNTL hourly-rate for industry at $75/hr. We assume two individuals will spend under 10 hours each weeks for 8 out of the 16 work weeks in the semester.

$$3 \times \frac{\$42}{\text{hr}} \times \frac{10\text{hr}}{\text{wk}} \times 16\text{wk} \times 2.5 = \$50,400 \tag{5}$$

$$2 \times \frac{\$75}{\text{hr}} \times \frac{10\text{hr}}{\text{wk}} \times 8\text{wk} \times 2.5 = \$12,000 \tag{6}$$

Our parts and prototype creation costs are estimated to be $42.98 per unit.

Part	Cost
ESP32 dual core microcontroller breakout board (mouser)	$10.00
TI Analog to Digital converter ADS7947SRTER (mouser)	$3.59
Toshiba CCD Linear Image Sensor TCD1103GFG (mouser)	$14.79
Assorted Resistors, Capacitors, ICs, Sockets	$10.00
PCB (PCBWay)	$4.60
Total	$42.98

We plan to build 5 prototypes with a total production cost of $62,614.90.
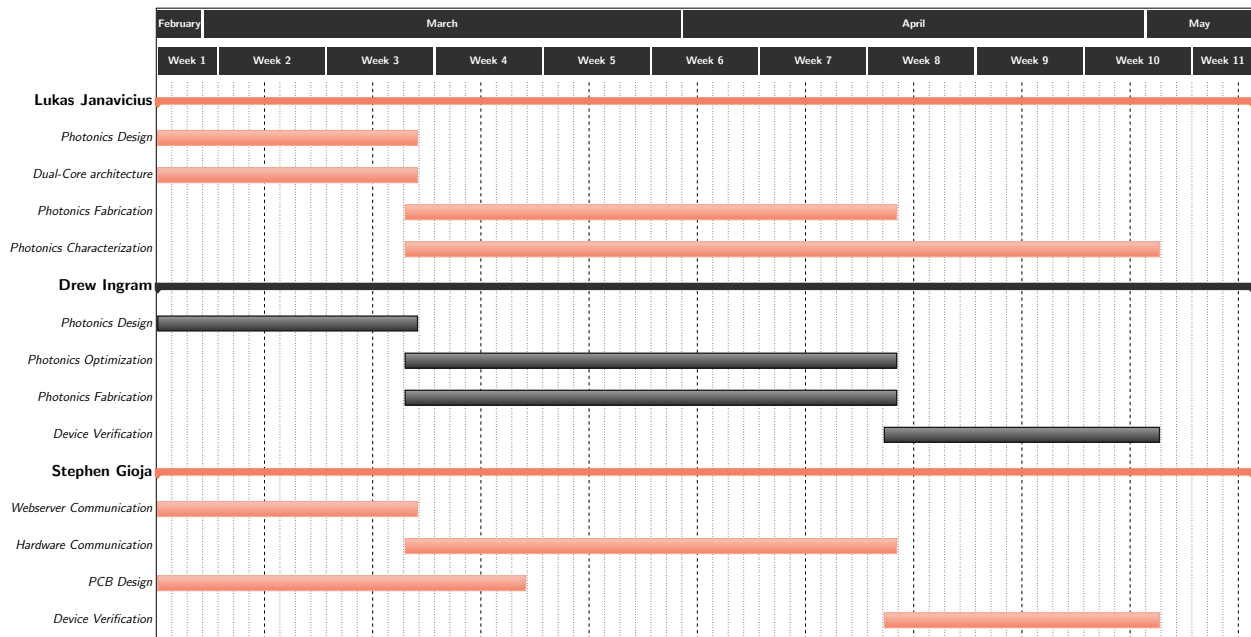
4.2 Schedule

Figure 9. Project Schedule.

5 Safety and Ethics

In the ACM Code of Conduct section 3.1 we see the main point of designing a new or enhanced device is should be to improve the lives of people [15]. This is our main goal which is reached by decreasing the cost of a spectrometer and therefore increasing the ability for people to obtain one. This would have a positive impact on scientific education from grade school to university.

We recognize that our device will handle data belonging to its users. Data from our device could potentially be used in scientific research and other sensitive applications. The user's data must remain private to the intended users

[15]. Our device will host a private network access point. Unauthorized users could potentially log in and access someone's data or cause data loss. We will mitigate these issues by presenting the users with a standard network login using password protection.

While developing we must respect the works of others, which includes citing our sources and not claiming the works of others as our own seen in Section 1.5 of the ACM Code of Ethics [15]. Section 2.4 of the ACM Code discusses giving/receiving feedback. We must listen to the feedback from our instructors and TA's and consider it in our design.

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