ECE 445

SENIOR DESIGN LABORATORY

Final Report

LASSI POWER BOARD

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May 1, 2019

Abstract

Our sponsor, the Laboratory for Advanced Space Systems at Illinois (LASSI) ran by Professor Lembeck, is currently designing the Illini-Sat 3; their next generation model of CubeSats. We have been tasked with designing the power board for this satellite design. The power board we designed and built provides regulated voltages from the solar panels and battery while ensuring the battery is in operational parameters. The power board is able to measure the power system parameters for telemetry purposes. Additionally, provides control measures to energize or secure loads as required through the interface. The system is able to interface with the rest of the satellite over a controller area network (CAN-bus).

Contents

1 Introduction

1.1 Background

The current power board used by the Illini-Sat 2 was developed for over a 2.5 year period and carries an impressive array of features [1]. Professor Lembeck wants the next generation board to have a more streamlined design such that it can be easily integrated into future systems. As a result, this new power board has been designed to be as reliable as possible. Since the rest of the satellite is still being developed, this power board design will serve as a baseline for future iterations. As this is the first design, we have implemented a single channel which can easily be scaled to meet the future requirements of the satellite; so additional modules can be added. Our board will serve as a test channel for the design and development of other modules.

1.2 High-level Requirements

1. From solar panels which output a nominal voltage of 17 VDC which can range from 5.4 to 21.3 VDC, provide regulated DC bus power rails, at 7.6 VDC(nominal[1]) and 3.3 VDC (+/-.2V), to support on-board instrumentation as well as provide means for on-board battery charging.

2. Provide a control system which can read voltage and current readings from essential points on the power board and can communicate with the Control and Data Handling Board(C+DH) via CAN-bus protocol.

3. Provide protective features[2] for the system to maximize resiliency of the power supply in case of fault conditions. This will include a watchdog timer which can reset the controller in the event of a fault.

[1] This voltage shall change based on the battery state of charge and will vary within a wide band.

[2] Full description of protective features is discussed in detail in the design portion of this document, qualitative requirements are discussed in great detail there.

1.3 Updates from the Illini-Sat2 Power Board

We have de-conflicted the role of the battery as a filtration device, by incorporating a more robust passive component scheme. Additionally, providing a means by which the battery can be utilized as an energy source only when required by the overall system conditions. This means that the battery is not required to run the satellite while it is illuminated. This ensures that satellite can operate with reduced functionality even if the battery fails.

2 Design

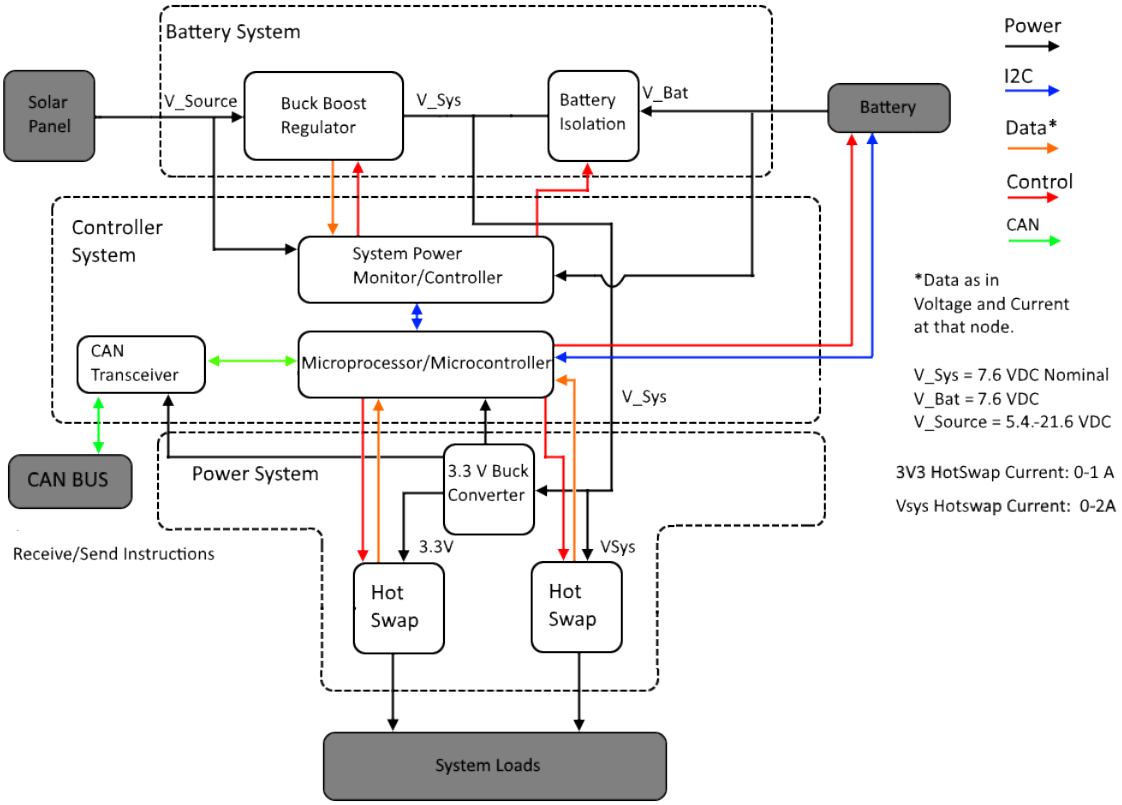

Figure 1: High Level Block Diagram.

2.1 Overall System Operation

Our overall system is composed of three subsystems: the Battery System, the Control System, and the Power System. The Battery system takes in an input voltage source from the solar cells, which can range from 5.4 to 21.6 VDC. The exact value cannot be specified as different solar cell configurations will be used by different satellites. A Buck Boost Regulator regulates the voltage on the V_{Sys} bus. The V_{Sys} and V_{Bat} bus operates between 6.14 to 8.4 VDC depending on the battery state of charge. The exact voltage is automatically

set by the Power Controller to facilitate proper battery charging. The Battery Isolation is provided through a P-MOS in order to provide protection and prevent unnecessary battery discharge.

The Control System interacts with the Battery System via the Power Controller. This controller controls the Buck Boost Regulator and the Battery Isolation MOSFET to ensure proper operation of the Battery Module. The Power Controller sends telemetry and receives instructions to the Micro-Controller module over the I2C bus. In addition, the Micro-Controller communicates with the Battery Module off-board via I2C bus to gather temperature readings. The Micro-Controller also to sends single bit digital control signals to the heating element in the battery module and the two Hot-Swaps. The controller also analyses voltage readings of current sensors within the Hot-Swaps as well as measures the voltage of the 3v3 regulated bus. The Micro-Controller additionally interacts with the Control and Data Handling module (C+DH) over a CAN bus through a CAN transceiver.

The Power System consists 3.3 V Buck converter which will regulate the voltage of the 3v3 bus; even though V_{sys} can range from 6.144 to 8.4 VDC. The 3v3 bus will operate at 3.3 VDC nominal +/- 0.08 V. The 3v3 Hot Swap will connect the the 3v3 bus to a regulated load. The V_{sys} Hot Swap which will connect the V_{sys} bus to an unregulated load as requested by our sponsor. The loads will be off board as they are outside the scope of our project.

2.2 System Power Monitor and Controller

The heart of the power board's design and functionality lies in the BQ25703 [2]. This 4 mm x 4 mm chip provides means for controlling the majority of the control functions for the system's vital buses. It functions not only as the gate driver for all of the major power MOSFETS, but also implements a wide array of protective features which increases the reliability of the design.

2.2.1 Device Initialization

Upon energization, the power board is capable of self starting on battery or solar power. Meaning, in the unlikely event that the satellite's battery completely fails, it will still function whenever it is illuminated. The device has been configured such that it will automatically start all the system parameters pre-loaded to ensure operating tolerances will not be violated prior to the start-up of the system Micro-Controller. Once the Power-Controller

is brought online, the optimal set-points will be provided through the I2C interface by the Micro-Controller, based on the current operating conditions.

Table 1: Average Power Generation and Payload Data

Configuration	Avg Bus Power Generated W	Avg Bus Power Required W	Avg Payload Power Allowed W
1.5U	2.85	1.5	1.35
2U	3.8	2	1.8
3U	6.65	2	4.65
6U	9.3	2.5	6.8

The current iteration of the power board design is functionally incapable of operating without a battery. This device does not have this limitation and can run off of solar power alone due to the inclusion of a P-Mos isolation switch for the battery bus. The isolation will also provide a means in ensuring that the battery is never unintentionally discharged when the systems loads are being met by the solar source alone. As a result, this will significantly reduce the number of battery charge cycles, the average depth of battery discharge, and will also serve to extend the system's battery life. The system will still be capable of immediately meeting power demand by supplementing with the battery, should this be necessary. Based on the data available for solar panel sizing vs. system demand, *Table 1* it is clear that the battery is only needed as a supplemental role.

2.2.2 Device Protection

1. WatchDog Timer

   The WatchDog Timer will open the battery MOSFET and terminate charging in the instance of loss of communications with the micro-controller. This ensures battery protection if the device control is lost. The Watchdog timer will be reset when communications are re-established with the Micro-Controller.

2. Input Over Voltage Protection

   Should the solar panels' input voltage rise above 23.5V, the chip will enter an over voltage condition. Here the switching regulator will be

de-energized and system loads will be powered by the battery. If the battery is already disabled by another protection, this will disable the satellite.

3. Input Over Current Protection

   In the event of an over-current condition, defined as 125 percent of the input current set point, the switching regulator will be turned off for a set period of time. This will result in the system cycling power.

4. System Over Voltage Protection

   In the event that System Bus Voltage (V_{sys}) exceeds 12 volts, the switching regulator will be turned off. The system bus will be powered by the battery, maintaining power continuity. The switching regulator will be re-enabled by the micro-processor.

2.2.3 Modes of Operation

1. System Voltage Regulation

   The battery MOSFET will be switched off, disconnecting the battery from the system bus. This will provide a regulated voltage to the system when power from the battery is not required or desired.

2. Battery Charging

   The battery MOSFET will be switched on, allowing the system to charge the battery in constant current (CC) and constant voltage mode (CV) at 4.2 volts per cell.

3. Battery Power

   The battery MOSFET is configured such that if power to the loads from the solar cells is insufficient, the battery will begin to discharge to supplement the load. Additionally, in eclipse conditions, the switching regulator will be fully de-energized and all power will come from the battery.

4. Reverse Power Mode

   Due to the symmetrical nature of the 4-switch buck boost converter Topology, bi-directional power flow is functionally possible. However, this function will be prohibited by placing the EnOtg pin to ground [2].

2.3 4-switch Buck/Boost Converter

The selection of the DC-DC Converter topology was not a trivial decision point. Due to the wide range of possible satellite configurations, the regulator must be capable of handling a wide range of inputs. The most common application will have a nominal input voltage of 17 VDC from the solar panel, but we must be able to accommodate an input up to 21.6 VDC (for a 8 solar cell 6U configuration at peak efficiency). The minimum voltage was determined by assuming a 1.5U design with one of the cells on each side not in operation; therefore a 5.4V input (nominal cell voltage for the solar cells is 2.7V). With these input voltage limitations, our design is sufficient. The battery configuration is a 2S/2P (Two-series, Two-parallel) with a nominal voltage of 7.6V utilizing INR18650 MJ1 3500mAh Li-ion cells [3]. The circuit was not configured to support more series cells due to the impact this would have on downstream buck converter sizing. However, minimal rework would be required to redesign these portions of the board to accommodate more series batteries (up to four).

Table 2: 4-Switch Buck/Boost Switching Strategy Overview

	Buck	Buck/Boost	Boost
Q1	Switching	Switching	on
Q2	Switching	Switching	off
Q3	off	Switching	Switching
Q4	on	Switching	Switching
Vo/Vi	D	D/(1-D)	1/(1-D)

In order to design as system capable of stepping up or down voltage, a 4-Switch Buck-Boost topology was chosen. This topology *Fig.2* operates either in buck mode, buck-boost mode, or boost mode based on the voltage transfer characteristic. As V_{in} approaches V_{out} from above or below, the converter will transition to a Buck-Boost switching strategy. This is to ensure a smooth transition from one voltage level to the other. However, it will cause the device to incur more switching losses due to the increased number of switches. Therefore as soon as the device is operating clearly as a buck or a boost, it will automatically enter into the appropriate mode to optimize efficiency. The output voltage of the converters will be based on the duty ratio of the high-side MOSFETS. *Please refer to Table 2 for an overview.* The Buck and Boost modes were also chosen to be synchronous in order to minimize

the size of the inductor needed in the circuit while precluding discontinuous conduction mode under light loads.

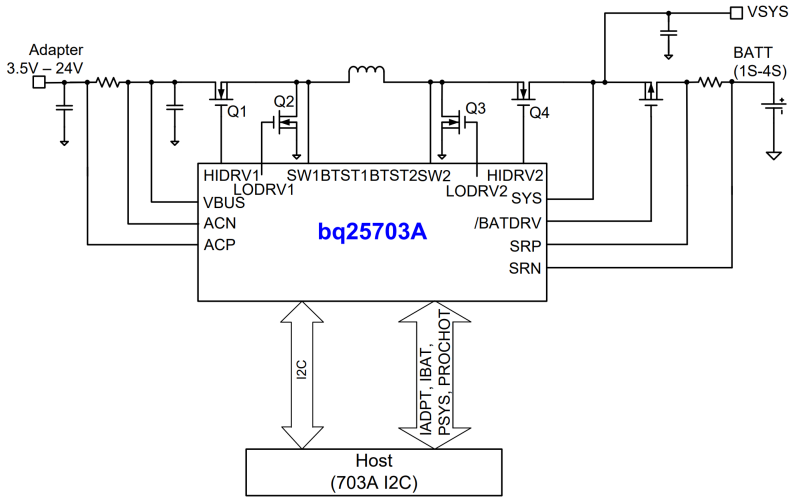

Figure 2: Application diagram from BQ25703 Data sheet[4].

The inductor for the buck-boost is a Wurth-Electronics $2.2\mu F$ with a self resonance of 24MHz[5]. An inductor should be operated at a frequency well below its self-resonance because beyond this point it will act like a capacitor. Hence this inductor is suitable for the switching frequency of 1.2 MHz. Additionally, it has a saturation current of 15.5 A which is greater than the rating of our solar panels. Additionally the foot print for this device is quite small (9.2mm x 8.5 mm) with a maximum height of 3.0mm.

The switching MOSFETs utilized are CSD17551Q3A n-channel MOSFETs with a voltage rating of 30 V and max current of 48 A both in excess of what is required with a significant safety margin [6]. Additionally the R_{dson} (Resistance drain-source) is minimal at less than $10m\Omega$ leading to low energy dissipation in the MOSFETs. These MOSFETs are well matched for the gate driving current of the BQ25703A.

2.4 Step Down DC Voltage Regulator

The DC-DC Stepdown converter is implemented with a monolithic design. The TPS53515 is an integrated MOSFET synchronous Buck converter with a footprint of only $26mm^2$. The passive components around the Buck are sized to accommodate up to 10 A drawn with an output ripple of less than 10 mV when its supply rail is at 8.3 V or 4.15 V / cell. This ripple specification is in order to be well within the requirements of the on board micro-controller; supplied off of the 3V3 rail as well as to supply system 3V3 loads. As of yet, the number and size of 3V3 loads has not been decided for any future projects. Therefore this buck converter is intentionally overrated in order to test the limitations of the battery and solar converter at high loads. In order to accommodate a 10 A load, while switching at a frequency of 416kHz, an output capacitive filter of $242\mu F$ will be constructed. In order to accomplish this without utilizing electrolytic capacitors, an unacceptable practice for space applications, eleven $22\mu F$ ceramic capacitors will be used in parallel [1]. This parallel arrangement will minimize the effect of the equivalent series resistance (ESR) of the capacitors. A $2.2\mu H$ inductor was chosen to provide proper average forward current and current ripple sufficient to guarantee the voltage ripple specifications previously mentioned[7]. This Coilcraft inductor is shielded to minimize leakage flux and interference and has core characteristics satisfactory for operation at 416 kHz. Additionally it is shown that this inductor will not saturate at the maximum design current of 10 A.

2.5 Hot-Swaps

The design of this power board is fitted with two TPS2420 hot-swap controllers [8]. One controller will provide an unregulated V_{sys} supply while the other is for the 3v3 bus. The next generation of Illinois CubeSats is in the early stages of development therefore this board simply produces two controlled outputs for demonstration and testing purposes. Both of the Hot-Swaps will have a 19.45 mSec fault delay in case of a transient over-current condition. This value was determined to be sufficient for testing by our Sponsor. Setting the time delay is as simple as using eqn 1. In this case we have chosen a $0.5\mu F$ capacitor to set the appropriate fault delay.

$$C_{ct} = \frac{T_{fault}}{38.9e3} \tag{1}$$

The design the V_{sys} hot-swap required an over-current (OC) of 3A [1]. Therefore a $65.5k\Omega$ resistor is connected per eqn 2. This is the absolute OC set point for the device. I_{fault} is transient set point and will occur after a time delay of approximately 20 mSec as previously discussed. This was set at 1 A less the absolute max setpoint to facilitate testing per eqn 3. This gives a resistance value of $100K\Omega$.

$$R_{Imax} = \frac{201k\Omega}{I_{max}} \tag{2}$$

$$R_{Ifault} = \frac{200k\Omega}{I_{fault}} \tag{3}$$

The 3V3 hot-swap was designed in the same fashion except that the max current set point is 2 A and the transient set point is at 1 A. This gives $R_{Imax} = 100k\Omega$ and $R_{Ifault} = 200k\Omega$.

2.6 Micro-Controller

In order to coordinate the various components of the power board, we need a Micro-Controller that is capable of communicating through I2C and CAN bus protocols, has an internal WatchDog timer, and at least 6 General Input and Output Pins(GPIO) which are capable of Analog to Digital conversion(ADC). As such, the control system on the power board is run by a STMicroelectronics STM32F072RB Micro-Controller [9]. We have coordinated with our sponsor and have agreed that this Micro-Controller is the best fit, as it fulfills all of our requirements. In addition, the STMicroelectronics controllers have a good track record at a reasonable cost.

The controller interfaces directly with the various components on the board. *fig. 13* Our implementation leaves many of the resources of the controller open; which will allow future groups to easily scale up the size of the power system. This meets one of the high level requirements of the project as there are 9 remaining Analog to Digital Pins as well as 29 remaining Digital I/O pins.

Upon energization, the Micro-Controller executes an initialization sequence. Here the Micro-Controller sets the required parameters of the Power Controller. Then it will establish contact and alert C+DH to notify that system has been reinitialized. After the initialization sequence, the Micro-Controller enters the main sequence of operation. First, the controller checks

to see if it has received instructions from the C+DH and carry out the instructions accordingly. In our implementation, the C+DH will only instruct the Micro-Controller to set the Hot-Swaps, change the parameters of the Power Controller, or to test the WatchDog timer. Normally, after every operation our Micro-Controller will reset its internal WatchDog timer. However, in this test function we set the Micro-Controller in an infinite loop until the timer re-initializes the Micro-Controller. This function has been included for testing purposes only. Second, if there are no instructions from the C+DH, the Micro-Controller gathers all the necessary system telemetry data from the Power Controller as well as reset the Power Controller's WatchDog Timer. If the Power Controller's System Over Voltage Protection is activated, the Micro-Controller will clear this condition. Third, the Micro-Controller checks the internal temperature of battery and sets the heating coil accordingly. Fourth, the Micro-Controller then checks the voltage and current of the Hot-Swaps. Finally, after all the system data has been gathered, the Micro-Controller transmits this information to the C+DH before repeating the main sequence of operation. *fig. 16*

2.7 CAN Transceiver

The CAN bus protocol requires that we transmit a differential output signal onto the physical bus. This gives the CAN bus noise immunity, which is why our Sponsor requires CAN bus communications with the Micro-Controller. Our Micro-Controller is not able to perform this task. A 3.3 V CAN transceiver will allow communication between the on board micro-processor and the C+DH *fig. 13*.

There were few requirements given for this component by our sponsor. We simply needed a CAN transceiver that will operate at 3.3 V. This particular device can operate within a tolerance of 3.0 to 3.6 V, which will be met by the requirements of our Buck Converter. The transceivers maximum data rate is 5 Mbps; which is larger than our micro-processor's 1 Mbps data transmission rate over CAN protocols. The Texas Instruments TCAN330D was chosen due to its low cost[10].

3 Design Verification

3.1 Overall System Operation

We were able to meet all of the high-level design requirements of our sponsor while implementing a few design improvements. Our final board implementation was not able to fully synthesize all of our requirements, however, we were able to produce a working fully functional prototype design consisting of all of the modules connected together.

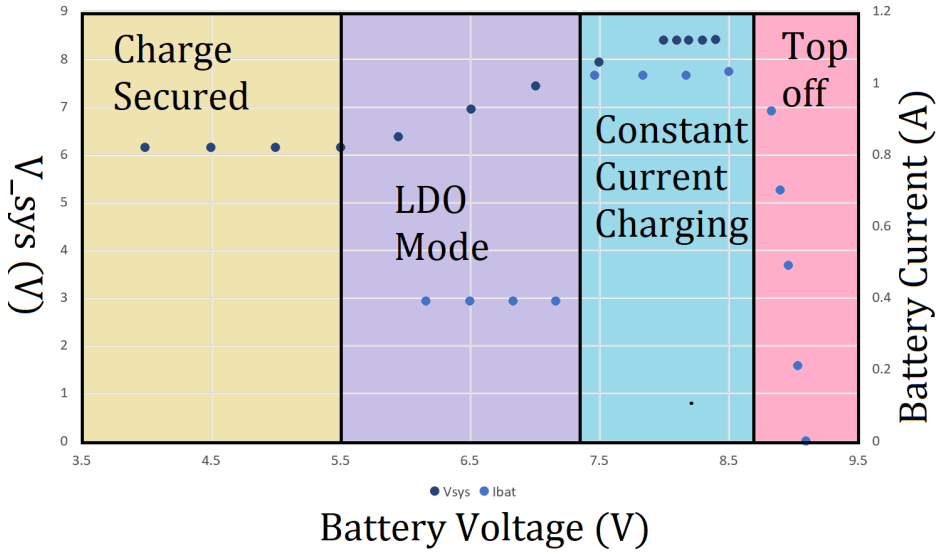

Figure 3: Battery charging over full battery voltage range.

3.2 System Power Monitor and Controller

We were able to fully configure the BQ25703A chip to operate properly for a general configuration. Our choice of IC satisfied all of the design requirements for the project and is an excellent candidate part for full implementation in the final flight ready design. We found this component to be capable of a great deal of customization for any of the projected cube-sat configurations.

3.3 4-switch Buck/Boost Converter

This converter topology meets the design requirements of all future satellite configurations, as opposed to simply a buck converter that was being utilized previously. This design is made to be configurable for any future designs of the solar source and battery module. This will provide the LASSI team with a "plug and play" design that will require no hardware changes between satellite designs and very few software changes. Figures 4 and 5 show the efficiency data collected at two operating points. This is an improvement from the previous design.

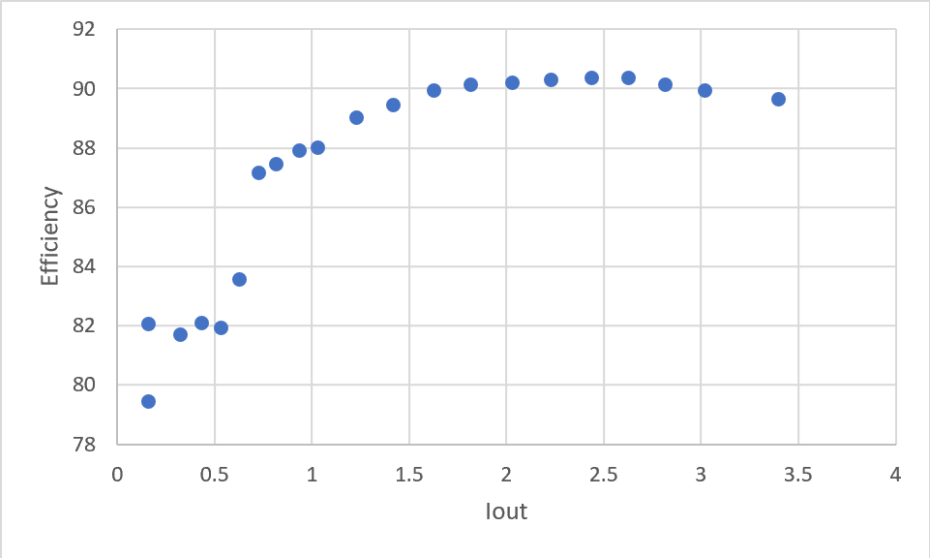

Figure 4: Efficiency measurements for buck-boost converter with a 17.6V solar input.

3.4 Step Down DC Voltage Regulator

The implemented buck converter is provided as a fully optimized configuration. This component is capable of obtaining power efficiency in excess of 95%. The specifications for average voltage and ripple were designed to be in excess of any previously stated design requirement. This serves two purposes for the sponsor. First, it establishes an excellent baseline performance of the function that can be used in component selection of payload modules. This

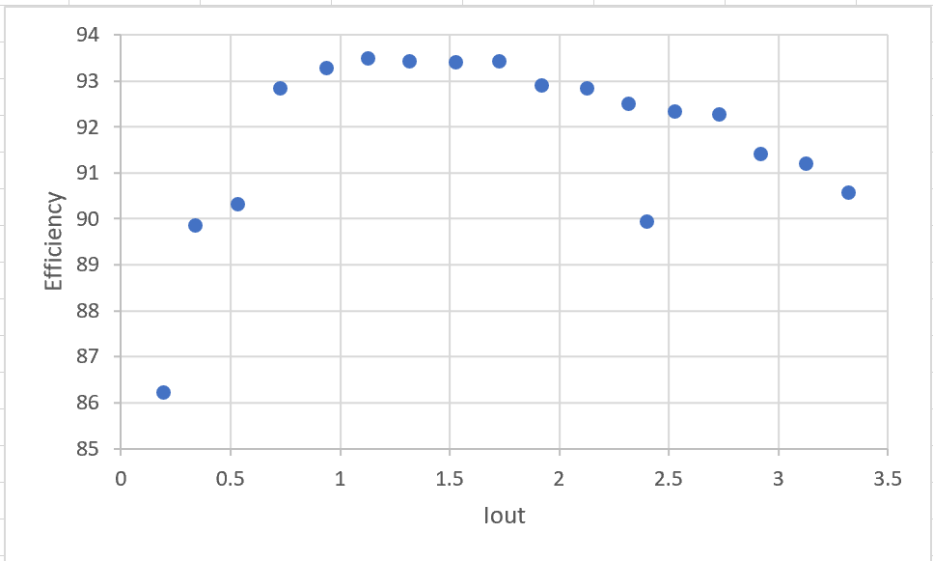

Figure 5: Efficiency measurements for buck-boost converter with a 8.1V solar input.

ensures that the step down regulator will never be the limiting factor on the type of 3.3 V payloads. Second, the system has been configured such that, if it is determined in the future that the design tolerances are unnecessarily tight for the payloads, the LASSI team can simply remove input and output filter components and save board space.

3.5 Hot-Swaps

The Hot-Swaps satisfied all of the baseline requirements imposed on them while occupying minimal board space. However, these Hot-Swaps have a fairly high on-state resistance (R_{ds-on}) of 33 mΩ. This unnecessarily lowers the systems overall efficiency and is a heavy cost to pay for a device that primarily is functions as a controlled switch. A perspective component for replacing the TPS2420 is the TPS25982. This component has the same 4x4 mm package size and external components but only 3 mΩ R_{ds-on}. This component is not yet commercially available, however, when it becomes available we highly recommend evaluating it as a replacement.

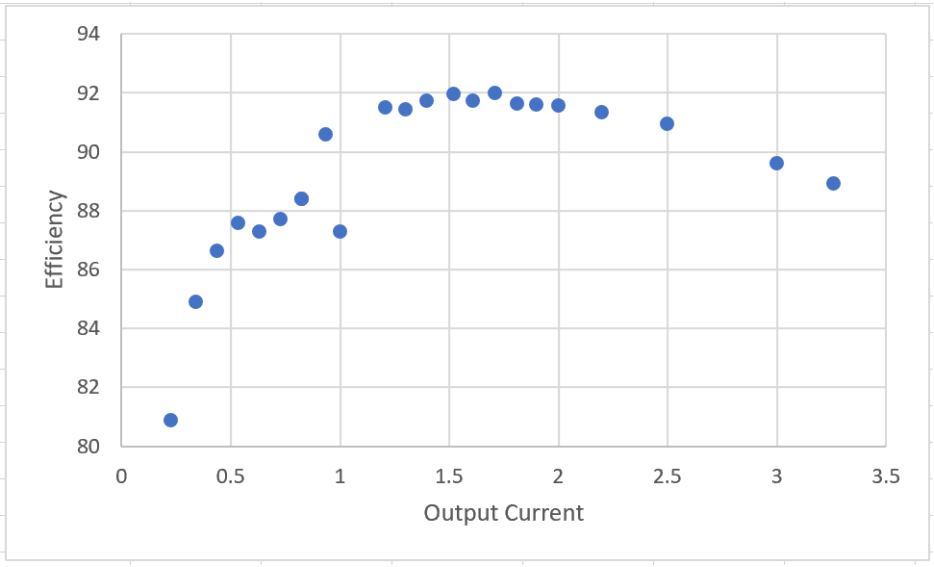

Figure 6: Efficiency measurements for the 3v3 buck converter

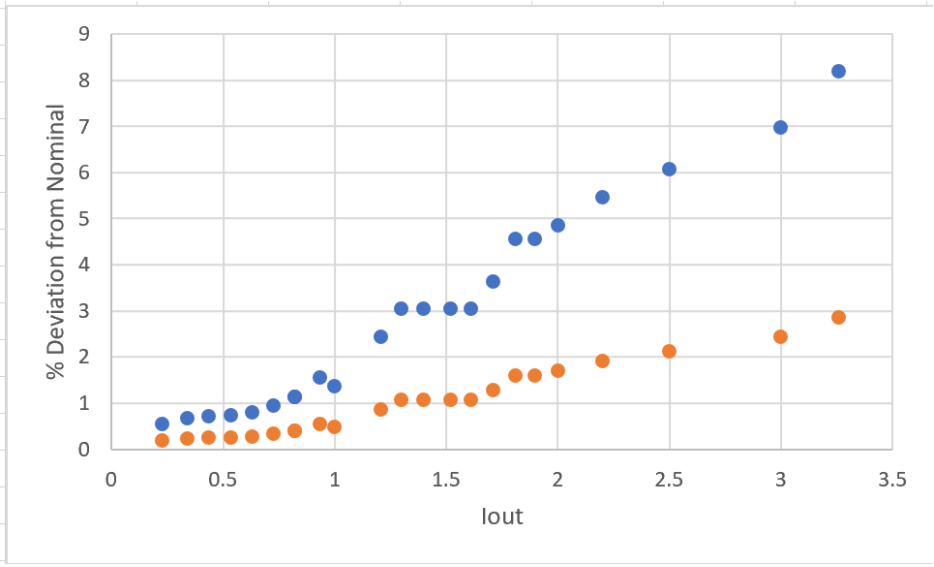

Figure 7: Average output voltage measurements for 3v3 buck expressed as a deviation from nominal. Blue curve is not adjusted for measurement equipment losses orange curve is adjusted for losses.

3.6 Micro-Controller

Our Micro-Controller met all of the software based requirements given by our sponsor. The Micro-Controller's single bit GPIO signals were able to control the operation of the Hot-Swaps as well as the simulated heating element of the Battery Module. The ADC readings of the Hot-Swaps' IMON pins were able to give accurate readings of the current passing through the Hot-Swaps. The conversion formulas below were derived using first order linear regression of IMON voltage readings off of a current sweep using an electronic load.4 These formula convert the voltage reading into the current in milliAmperes.

We were able to establish I2C communication with both the simulated battery module as well as the power controller. This was confirmed by reading telemetry from both systems and setting parameters within the power controller. We confirmed CAN Bus communication by sending this telemetry through our CAN Bus to our simulated C+DH. *See Software Block Diagram. 16*

$$I_{Vsys} = 0.77 * V_{adc} - 199 \tag{4}$$

$$I_{3V3} = 0.446 * V_{adc} - 118.4 \tag{5}$$

3.7 CAN Bus Protocol

We developed a polling based CAN Bus protocol which is capable of sending data at 1 Mbps. This communications protocol is asynchronous and is able to send messages of arbitrary length through multiple packets. The LASSI team has not developed their own CAN Bus communication protocol so this will be of great use in the development of the Illini-Sat 3. *See Software Block Diagram for CAN Bus Protocol. 18*

4 Cost

4.1 Cost of Parts

See table 3.

Table 3: Estimated Cost

Description	Part number	qty	Cost	Available
Power management eval board	BQ25703EVM	1	149.99	TI.com
Power management controller	BQ25703	1	5.28	digikey.com
Hot-Swap controller	TPS2420	2	5.88	digikey.com
Integrated Buck Converter	TPS53515	1	6.49	digikey.com
CoilCraft 2.2 uH Inductor	XAL7070-222MEB	1	3.14	mouser.com
Wurth Electronics	74437356022	1	2.08	mouser.com
CAN-Transceiver	TCAN330DR	1	2.37	digikey.com
Micro-Controller	STM32F072RB	1	3.84	mouser.com
Passives	numerous	1	10	digikey.com
Micro-controller dev board	NUCLEO-F072RB	2	20.66	mouser.com
Total			**209.73**	

4.2 Cost of Labor

The average hourly salary of an ECE graduate from the University of Illinois is $34.20 an hour. We have three people in our group and worked approximately 15 hours a week per person. Given the 13 weeks of design implementation in this course, we would expect labor to cost $16,929. This number was multiplied by a factor of 2.5 to account for unforeseen overhead costs. This brings the total cost to approximately $42,322 See the equations below.

$$\frac{\$71,166}{1yr} * \frac{1yr}{2080hr} = \$34.20/hr \tag{6}$$

$$\$34.20/hr * 3 * 15hr * 13 * 2.5 = \$42,322 \tag{7}$$

4.3 Schedule

See Schedule in Appendix B 23.

5 Conclusion

5.1 Accomplishments

We successfully met all of our high level requirements. Our power-board is able to operate with every solar cell configuration used by our sponsor. We have developed a robust system which can be easily scaled as need by the LASSI team and our CAN bus protocol will aid in the development of other systems on the Illini Sat 3. Most importantly, our power-board eliminates unnecessary cycling of the battery which will increase the lifespan battery module over the current power-board.

5.2 Uncertainties

Our greatest uncertainty was the construction process of the final build. Our board had many small components, some of which were very sensitive to heat. We ensured that the reflow oven was not set to a temperature that would damage components, keeping the temperature under 240 °C. However, when we attempted to make repairs we believe that we damaged some of our components due to the ground plane heating up. We have looked into this issue and have discovered that using a hot air gun is the best approach given the equipment available. In addition, we need to cover the rest of the board with aluminum tape to protect the other components on board from being exposed to the hot air. This will prevent other components from being damaged while making repairs.

5.3 Safety and Ethics

Prior to any testing performed in the accomplishment of this design, specific safety briefings were held regarding the testing procedures and hazards present. Additionally, all operating limits of the equipment were verified and observed during testing.

The Illini-Sat 2 battery module has an array of protective features required to utilize Li-Ion cells. Unfortunately, our sponsor was unable to provided us with a battery module this semester. In accordance with principle 1.2 the ACM Codes of Ethical and Professional Conduct, "Avoid Harm" we did not utilize unprotected cells [11]. As such we simulated the battery module with an electronic load to verify its functionality.

In addition to ensuring our safety and the safety of others, we developed a reliable power-board for our sponsor. According to ethical principle 2.9, we must "Design and implement systems that are robustly and usably secure." In striving to meet this standard we developed a product for our sponsor that will ensure a greater reliability of their next generation of satellites.

5.4 Future Work

We looked at past mission data and determined that our power-board design needed to be optimized around protecting the battery during the charge cycle. However, our power-board can implement Maximum Power Point Tracking (MPPT) through software. MMPT requires information on the specific loads of the satellite but the LASSI team can easily implement this feature in the future with our physical design. In addition, our board has many small components and several IC chips were damaged in the long construction process due to overheating. We recommend that our sponsor develop a more streamlined construction process to avoid damaging components in future builds of the system.

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Appendix A

6 Appendix A: Requirements and Verifications

All requirements were successfully met and verified during our demonstration.

Initial Conditions for Solar Source: 1 Points	
Requirements	Verification
1) System can initialize and utilize solar source while the battery is disconnected from the system at 17.6 V +/- 3 V nominal.	1) Isolate the battery from the system and have the simulated C+DH query the micro-controller. The return of system telemetry from the micro-controller will confirm this requirement has been met.

Initial Conditions for Battery Source: 1 Points	
Requirements	Verification
1) System can be energized from a battery source while solar cells are disconnected from the system.	1) Isolate the solar cells from the system and have the simulated C+DH query the micro-controller. The return of system telemetry from the micro-controller will confirm this requirement has been met.

WatchDog Timer: 1 Points	
Requirements	Verification
1) The WatchDog timer will time out when the BQ25703 does not receive the proper communication from the micro-controller.	1) Issue a command to the micro-controller to set the watchdog timer to 5 seconds and stop issuing instructions to the power-controller. This will cause the WatchDog Timer to time out and securing battery charging. We will verify this by observing V_{sys} and V_{bat} and verifying that they assume different values.

Input Over Voltage Protection: 1 Points	
Requirements	Verification
1) This protection will have the device go into over voltage protection when device exceeds the voltage set point. 2) We will accomplish this by current limiting a power supply to 0.20A and increasing the supply voltage to 30V which is above the 27V input voltage limit.	1) When the input rises above safety threshold the system will secure operations to the switching regulator. Subsequently, the regulator will remain de-energized until the voltage drops below the voltage limit.

Input Over Current Protection: 1 Points	
Requirements	Verification
1) This protection will have the device to go into over-current protection mode when input current exceeds device's set point.	1) Decrease the input over current protection set point to the system minimum. Observe that the switching regulator will de-energize by observing V_{sys}. This is a discrete test.

System Over Voltage Protection: 1 Points	
Requirements	Verification
1) This protection will cause the system to go into over-voltage protection mode when the system's voltage exceeds system's set point.	1) Decrease the over voltage protection set point to the minimum. Observe that the switching regulator will be de-energized and not re-energize until a proper control signal is sent by the micro-controller. This can be verified by measuring V_{sys}.

System Voltage Regulation: 3 Points	
Requirements	Verification
1) System regulates output voltage to the Vsys bus between 6.0V and 8.7V without the aid of the battery. System can initialize and utilize solar source while the battery is disconnected from the system.	1) Measure the average voltage reading using an oscilloscope. This test is intended to show the voltage regulation ability of the system with the battery disconnected. A DC power source will be applied to the input of the circuit and the V_{sys} output will be connected to a power resistor for constant load conditions. DC source will be swept from 5.4 volts to 20 volts in one volt increments. No data points shall be outside of the specified range.

Battery Charging: 10 Points	
Requirements	Verification
1) Utilizing a programmable load, the full charging sequence is demonstrable from LDO mode to constant current and constant voltage mode.	1) Simulating a battery, confirm the full operations of the BQ25703 charging operation cycle by using an oscilloscope to show the charging sequence is executed properly. [2] a) Prior to reaching 5V at the battery terminal, the BATFET shall be off and the current into the load should be zero. b) At the 5.5 volt level the battery will charge in LDO mode. This will be indicated by a charge current not to exceed 500mA. c) Constant current charging mode is verified between 6.5 and 8.0 V. At these data points current into the battery should be maintained at 1A (+/- 100mA). d) From 8.0 V to 9.0V, data points will be taken more frequently. At 8.2V (+/- .1V), the charger will enter constant voltage mode. This is demonstrated by current into the load decreasing over each subsequent voltage step until termination at 8.4 (+/- .1 V). e) At the point that current goes to zero, only one more test point will be required to verify the BATFET stays off when voltage is greater than 8.4(+/- .1 V).

Battery Power: 3 Points	
Requirements	Verification
1) The battery will transition from System Voltage Regulation Mode, to Battery Supplement Mode, to Battery Only Mode.[2].	1) VR mode verification. Set the E-load current to 1 A constant current on the V_{sys} bus. Verify BATFET is off by observing the battery current output. Then slightly lower the simulated Solar input and verify that BATFET does not turn on. 2) Supplement mode verification. Maintain E-load current at 1A. Set solar input current limit to 1.2 A and slowly lower the solar input current until solar supply is current limited (simulating reduced power output for solar cells). The BATFET shall turn on and the battery will discharge to maintain load demand. 3) Battery only mode verification. The solar source supply will be deenergized and the battery shall begin to discharge.

Reverse Power Mode; 0 Points	
Requirements	Verification
1) During testing sequence, make sure that Reverse Power Mode will not occur or be triggered.	1) Make sure the bit that's sent to the Reverse Power Mode is low and that no other function can cause the bit to be high.

Step Down DC Voltage Regulator: 3 Points	
Requirements	Verification
1) Average Voltage: Shall maintain output voltage at 3.3VDC average (+/-) 80 mV. Satisfies requirement for CAN-transceiver. 2) Voltage peak to peak shall not exceed 5%.	1) Will observe average voltage output over operating range of 3V3 buck with an oscilloscope and verify condition is not violated. 2) Will be performed in conjunction with the average voltage test.

Hot-Swaps: 2 Points	
Requirements	Verification
1) Transient Over-Current: Shall secure power to the load if the transient over current setpoint is exceeded within 40mSec. 2) Imax Over-Current: Shall secure power to the load within 40mSec and not allow current to exceed the absolute limit 2A for the 3V3 hot-swap and 3A for the Vsys hot-swap. 3) Both hot-swaps will be energized and secured with control from the micro-controller.	1) For both hot-swaps, this functionality will be tested by adjusting current to 1.5A for the 3V3 hot-swap and 2.5A for the Vsys hot-swap. The load will be simulated with a variable load. The resistance will be lowered raising the current. The current will be calculated using Ohm's law and by measuring the voltage drop across the load. 2) Repeat part 1 but adjust the current to 2.5A for the 3V3 hot-swap and 3.5A for the V_{sys} hot-swap. 3) This verification is met in the micro-controller verification section.

I2C Communication with Power Control Module: 6 Points	
Requirements	Verification
1) Our micro-controller must be able to send instructions to the Power Controller over the I2C bus, which will run I2C standard protocols. 2) Our micro-controller must be able to receive data from the Power Controller over the I2C bus.	1) Upon energization, the Power Controller does not engage in normal operations without presets from the micro-controller. As such, proper initialization of the Power Controller, as described by its requirements and verification, will show instructions has been successfully sent by the micro-controller via I2C. 2) The micro-controller will send the telemetry from the Power Controller to the C+DH. This telemetry will be displayed on a monitor. The displayed result will confirm this requirement has been met.

I2C Communication and Control of Battery: 2 Points	
Requirements	Verification
1) The micro-controller must be able to receive data from the battery over an I2C bus. The battery will report its current temperature to the micro-controller. This will allow our system to keep the battery within optimal temperatures. 2) The micro-controller can send a one bit digital signal to the battery to control the heating element within the battery module.	1) LASSI currently does not have additional battery packs to lend us for our project. With this in mind, the Battery Pack will be simulated with a simple I2C temperature sensor to be provided by our sponsor. This will allow us to simulate temperature readings. These readings be read by our micro-controller and sent to the C+DH. The display of the temperature readings on the monitor will confirm this requirement has been met. 2) The single digital bit signal will control a LED to confirm when the heating element signal is active. This signal will turn on/off when the temperature rises/fall above/below a set threshold. The actual temperature constraints of the battery are outside of what we can realistically simulate in lab. As such, we will set the threshold temperature to roughly 10 degrees F above room temperature. This will ensure that the heating element is active. We will then raise the temperature of the sensor above the threshold and will set the signal to low and turn the LED off. We will then let the sensor cool and the LED will turn on again. This will confirm that this requirement has been met.

Voltage Measurement of 3v3 Hot-Swap: 1 Points	
Requirements	Verification
1) Our micro-controller must be able to make voltage measurements at the node of the 3v3 Hot-Swap. We will require an accurate reading to +/- 0.2V. We will not need to make voltage measurements directly off the V_{sys} Hot-Swap as the Power Controller will provide our processor with this information.	1) We will connect an ADC pin on our micro-controller to the 3v3 bus node. The micro-controller will make measurements of this node every second. The telemetry will be returned to the simulated C+DH and be read off of a monitor. This will be confirmed by measuring the node voltage directly with an oscilloscope.

Current Measurement of both Hot-Swaps: 1 Points	
Requirements	Verification
1) Our micro-control must be able to make current measurements at each of the Hot-Swaps. Our Hot-Swaps have a built-in current sensor that outputs a DC voltage signal proportional to the current passing through the Hot-Swap. Our micro-controller will measure this voltage signal with an ADC pin in the same way it will measure the 3v3 Hot-Swap voltage. Our processor can then calculate the current. Our sponsor did not give us quantitative requirements concerning the accuracy of this measurement. We have chosen an accuracy of +/- 5 percent.	1) Our micro-controller will measure this voltage signal and use it to calculate the current passing through the Hot-Swaps and be relayed back to the C+DH and display it on a monitor. We can confirm this by directly measuring the voltage across the simulated load which will be a variable resistor. We can use Ohm's law to calculate the current.

Direct Control of Hot-Swaps: 1 Points	
Requirements	Verification
1) Our micro-controller must be able to activate and deactivate the Hot-Swaps at will; which will allow us to control the current flow through the Hot-Swaps. This will be done with a single bit signal to each of the Hot-Swaps.	1) We will have our simulated C+DH instruct our micro-controller to turn each Hot-Swap on and off. We can confirm this as by measuring the voltage across our simulated loads with an oscilloscope. The voltage across the loads will essentially drop to zero. This is a discrete process.

CAN Bus Communication with C+DH: 10 Points	
Requirements	Verification
1) The micro-controller must be able to send telemetry to the C+DH over a CAN Bus through CAN Bus protocols. This telemetry will be sent once per second. 2) The micro-controller must be able to immediately send notifications to the C+DH in case of potential unexpected changes in operation of the power system such as a fault. 3) The micro-controller must be able to receive and execute instructions passed by the C+DH.	1) Since the C+DH has not yet been designed by LASSI, we will simulate the C+DH on a development board. The development board will interface with our personal computer. The simulated C+DH will display the telemetry on a monitor. This will confirm that the first requirement has been met. 2) While verifying the over current protection of the HotSwaps, the micro-processor will alert the C+DH that the HotSwap has opened. The reception of the signal will demonstrate that the signal is sent immediately to C+DH. 3) We will give an instruction to turn the HotSwaps on/off and this will be confirmed through direct measurements (This will be a discrete process). This will demonstrate that the micro-controller is able to execute and receive instructions from the C+DH.

Create Differential Signal on CAN Bus: 0 Point	
Requirements	Verification
1) Create a differential signal so that our micro-processor can communicate with other micro-processors through a CAN bus interface.	1) We will connect the transceiver on our power board to another one-off board. We will be using a micro-processor development board to simulate the C+DH. When communications are established between the two micro-processors, we will have verified that this part is working.

Independent Watchdog Timer: 2 Points	
Requirements	Verification
1) Our micro-controller must have an independent watchdog timer that can restart in the event of an internal error. Our micro-processor has a 12-bit internal watchdog timer on an independent 40 kHz clock. [1] This means if the timer is not reset through software every 0.1024 seconds the micro-controller will restart.	1) In normal operation, our micro-controller will reset the watchdog timer after every major task. However, since we cannot count on an internal error for demonstration, our simulated C+DH will give our micro-controller the command to enter an infinite loop; where the WatchDog timer will not be reset. When the timer finished counting down, it will restart our controller and the C+DH will receive the restart message from the micro-controller. This will verify that the Watchdog timer is working.

Appendix B

7 Appendix B: Large Figures

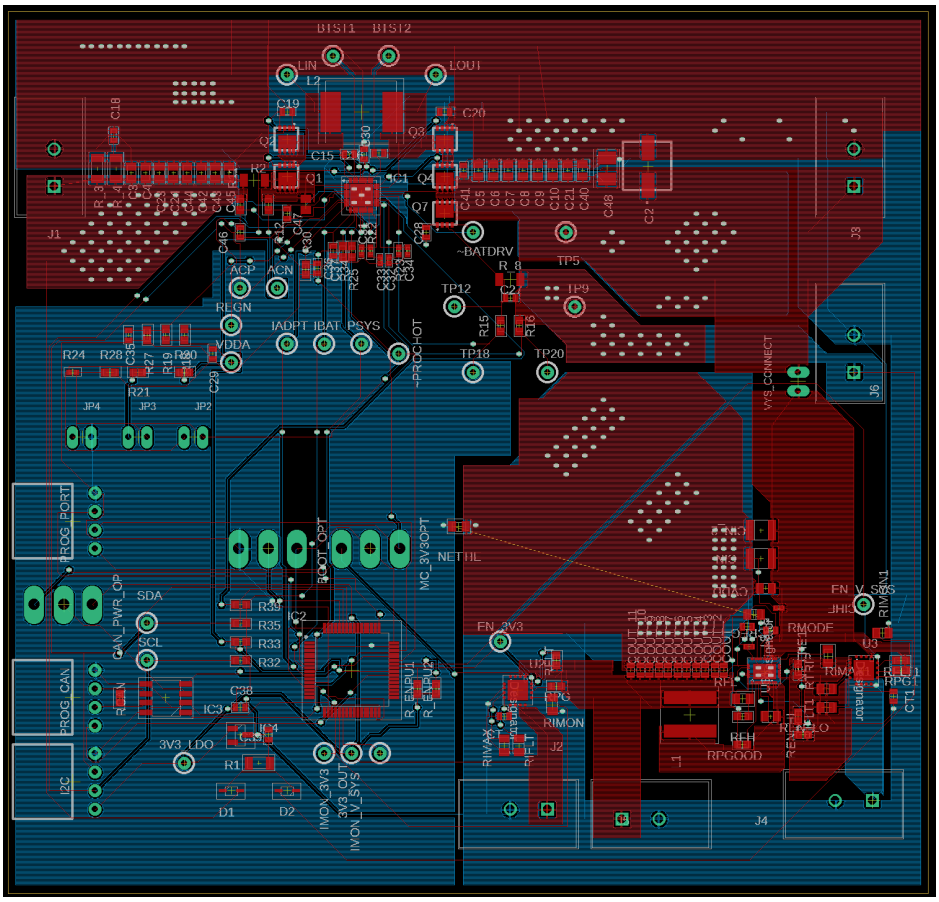

Figure 8: PCB Layout

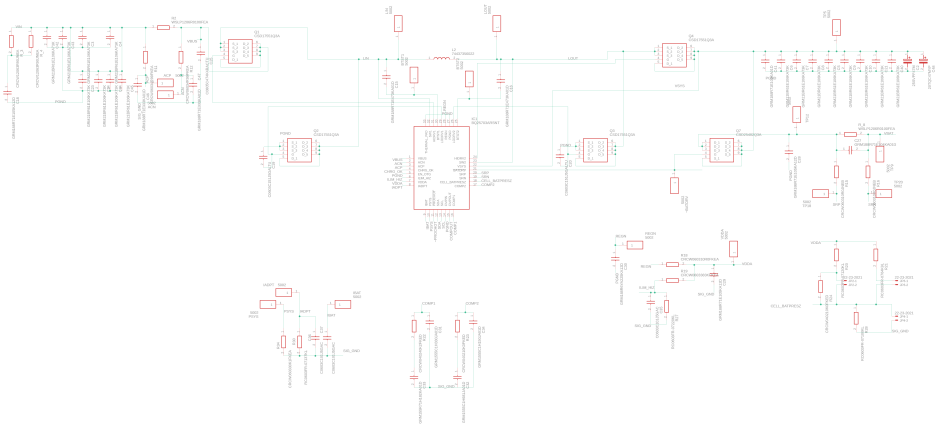

Figure 9: BQ25703 Schematic

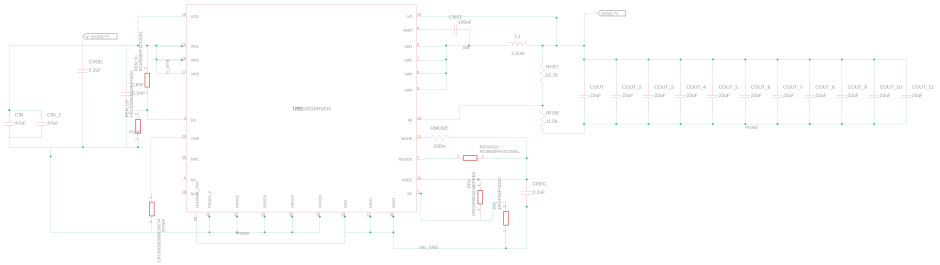

Figure 10: Eagle Schematic for 3.3V DC step down regulator

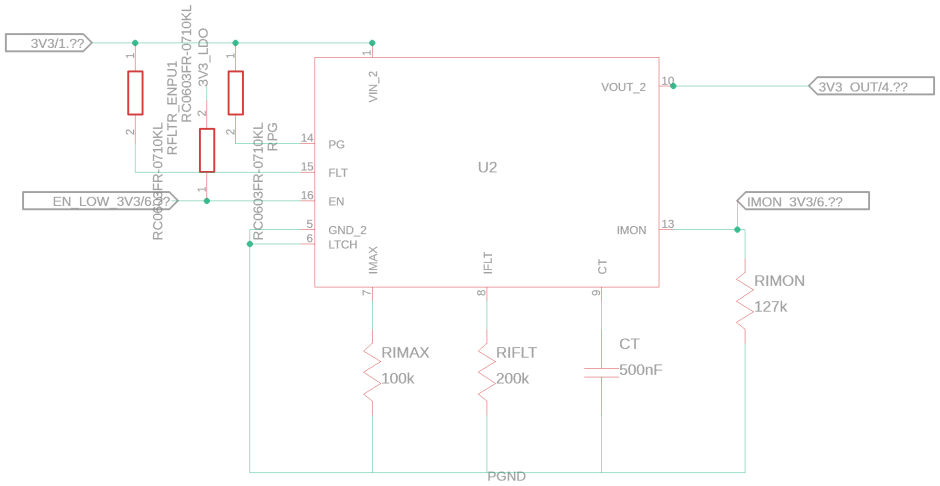

Figure 11: Eagle Schematic for 3v3 Hotswap Controller

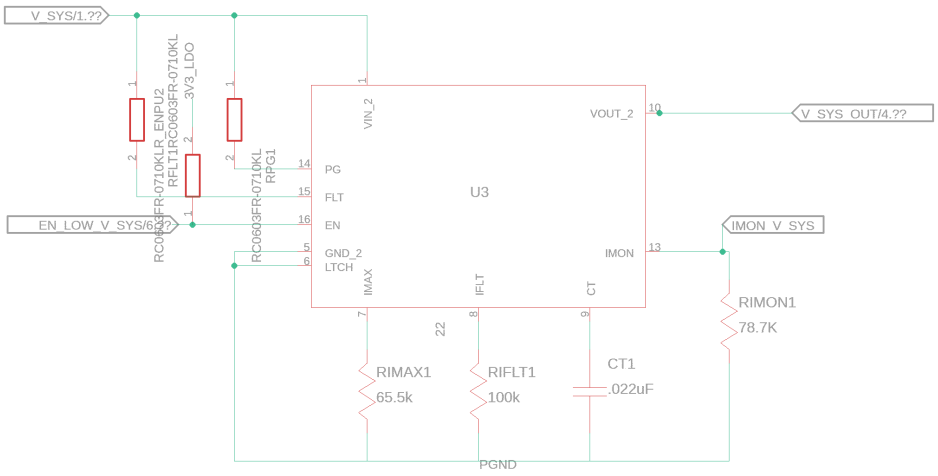

Figure 12: Eagle Schematic for VSys Hotswap Controller

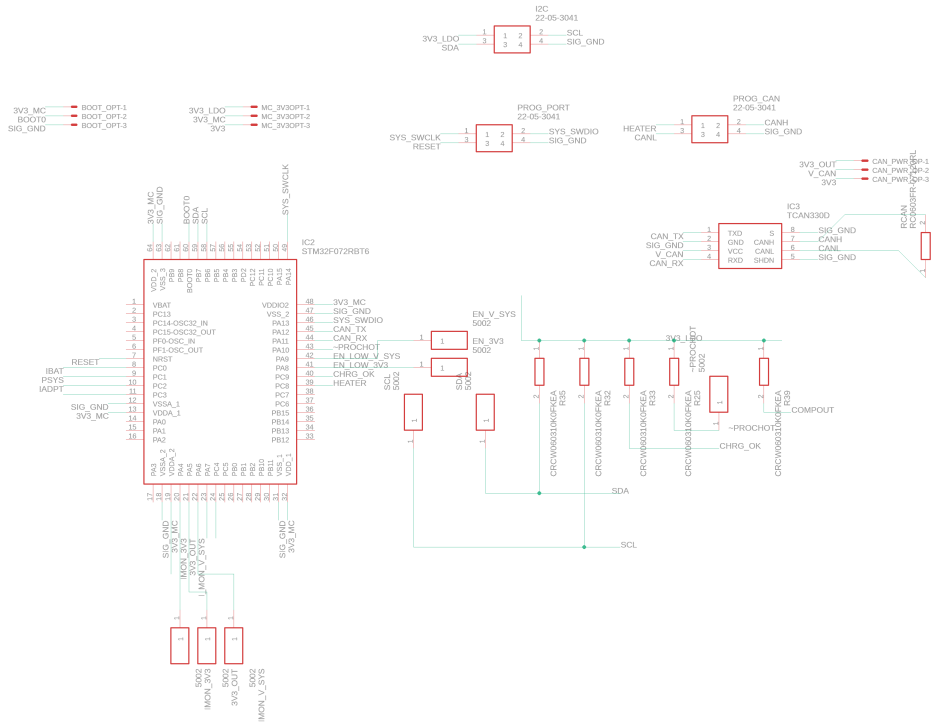

Figure 13: Eagle schematic for microprocessor and support circuits.

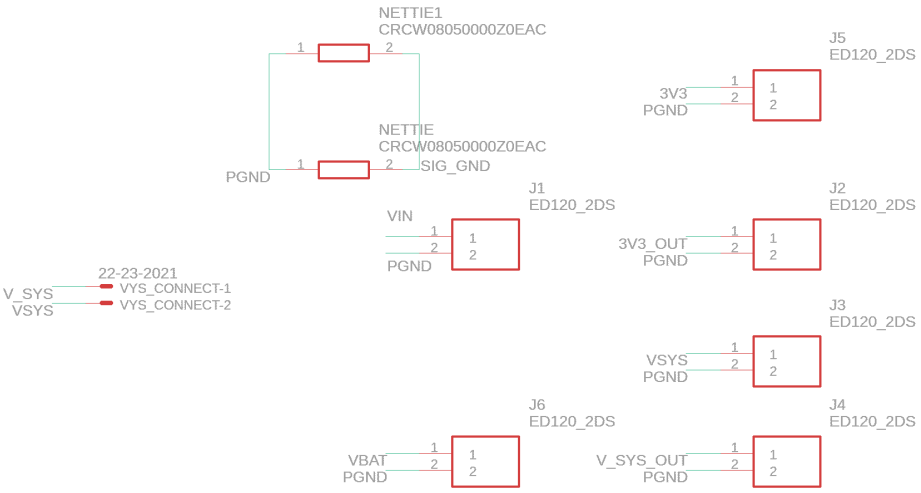

Figure 14: Eagle Schematic of Connectors

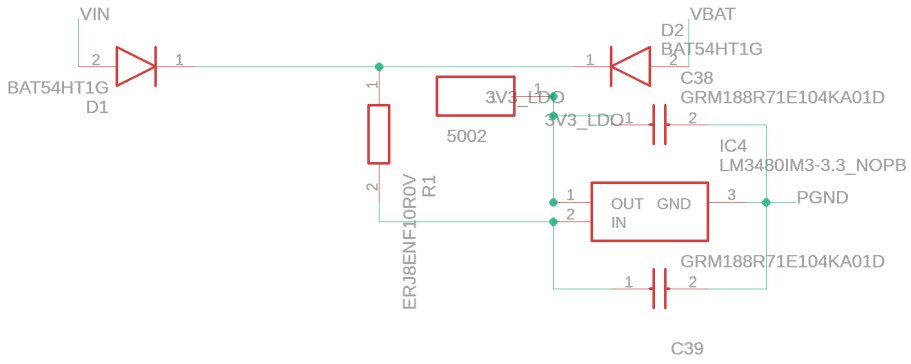

Figure 15: Eagle Schematic of LDO

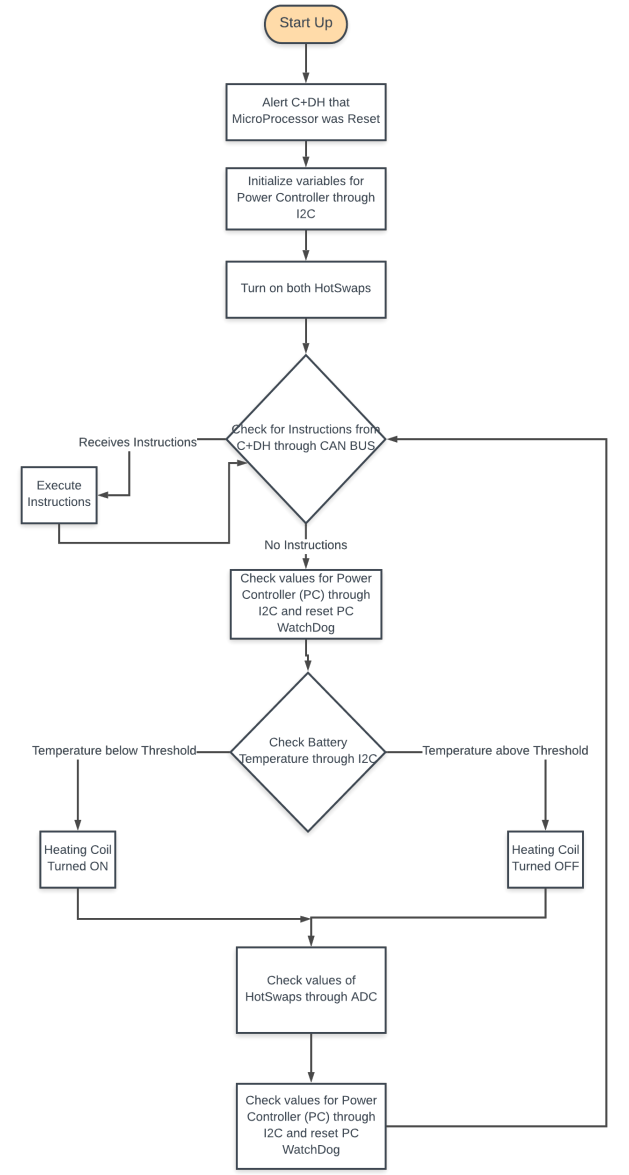

Figure 16: High Level Software Block Diagram

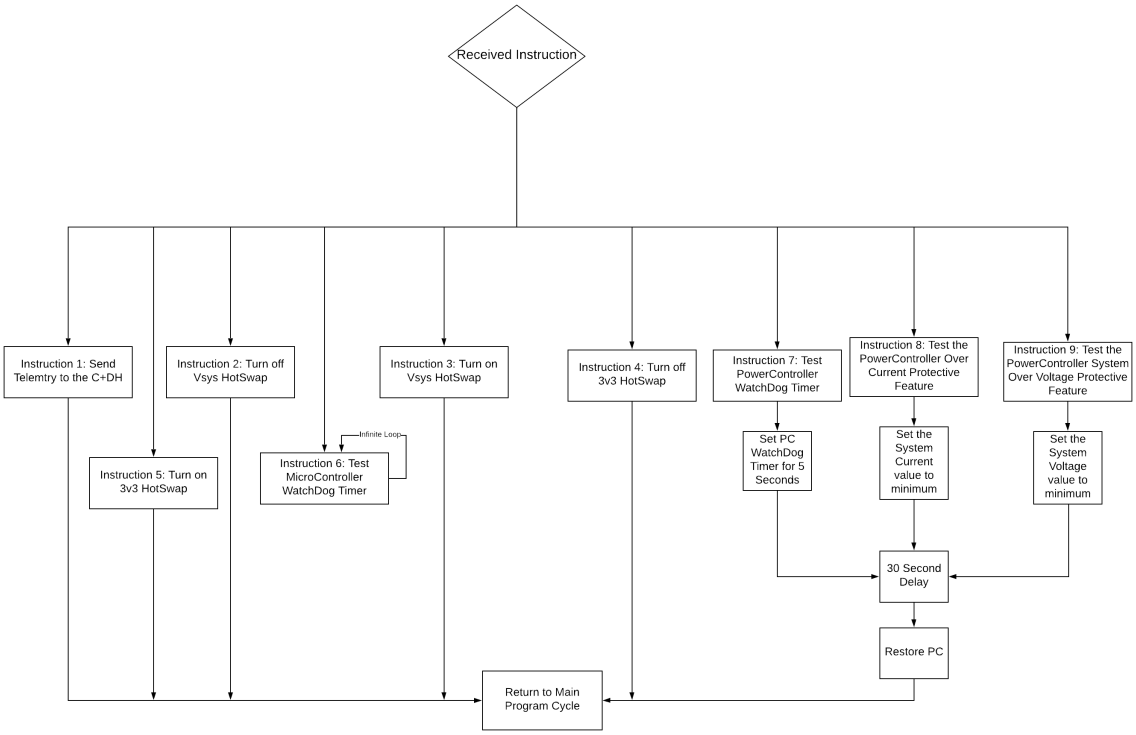

Figure 17: Software Block Diagram of Instructions

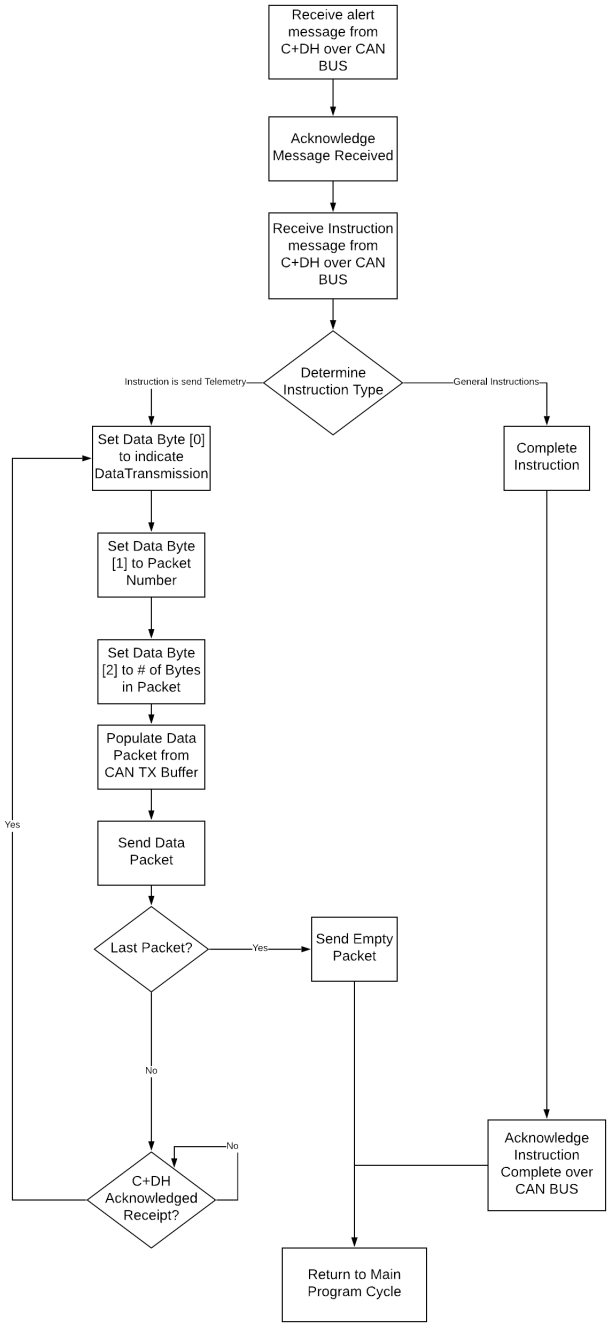

Figure 18: Software Block Diagram of CAN bus Communication Protocol

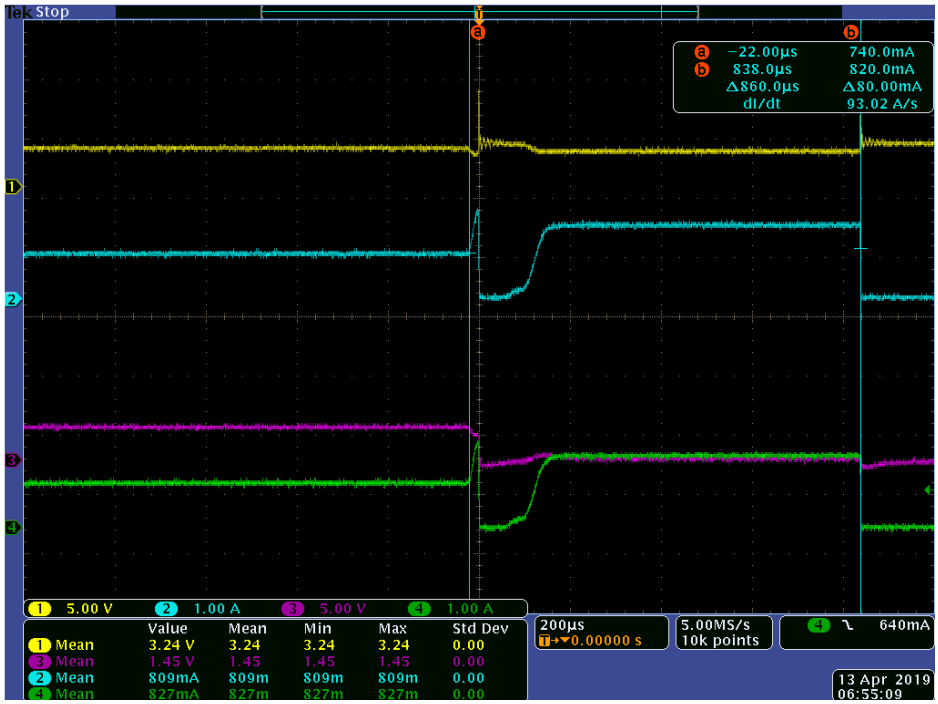

Figure 19: 3v3 Hot-swap response to 1.5A over-current condition

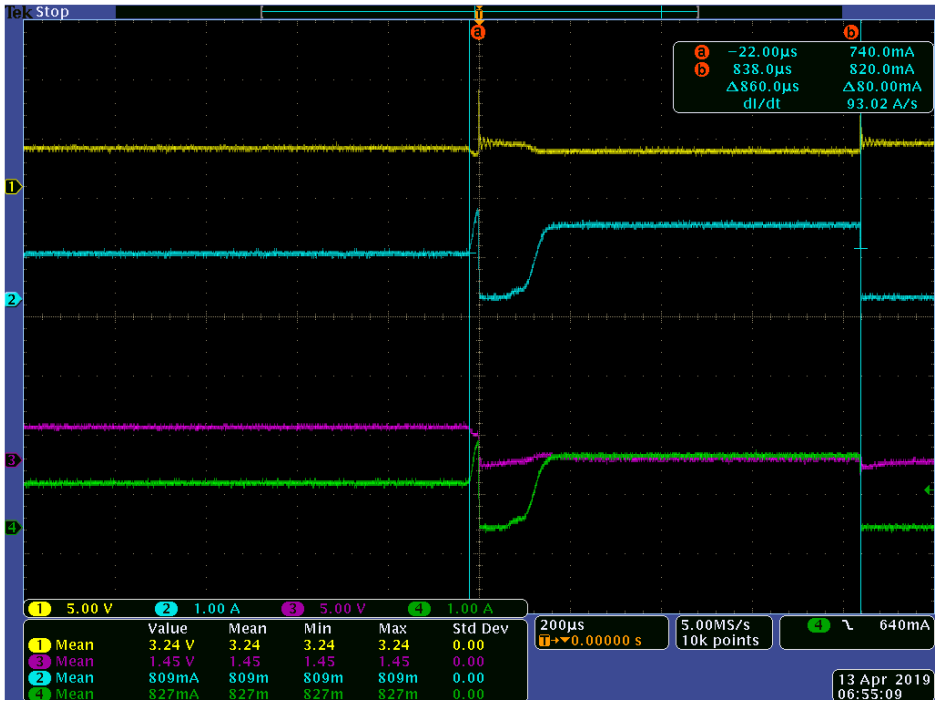

Figure 20: 3v3 Hot-swap response to 2.5A over-current condition

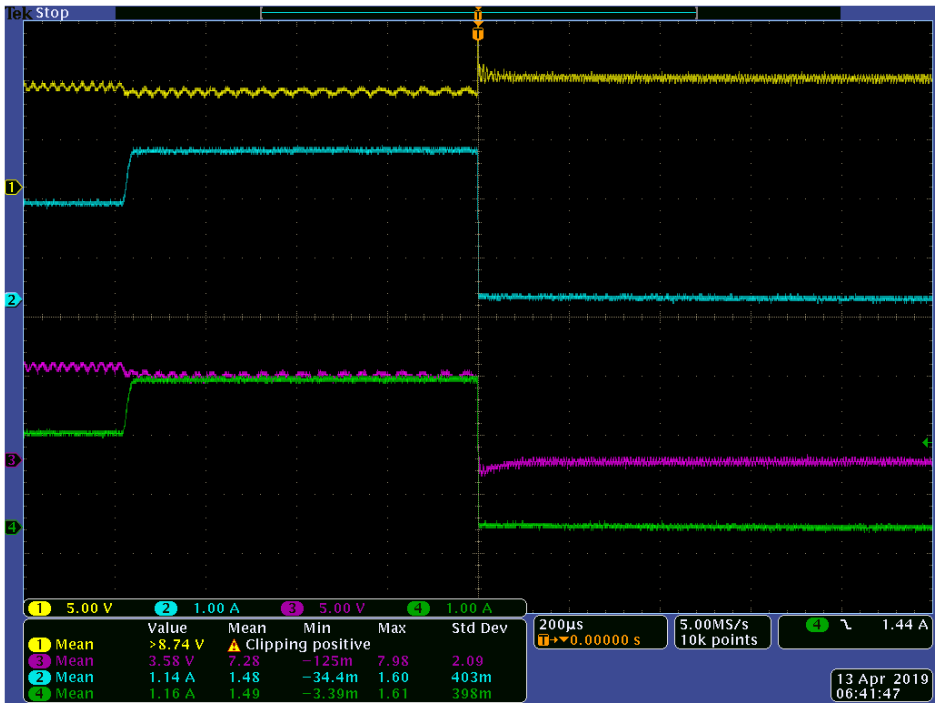

Figure 21: Vsys Hot-swap response to 1.5A over-current condition

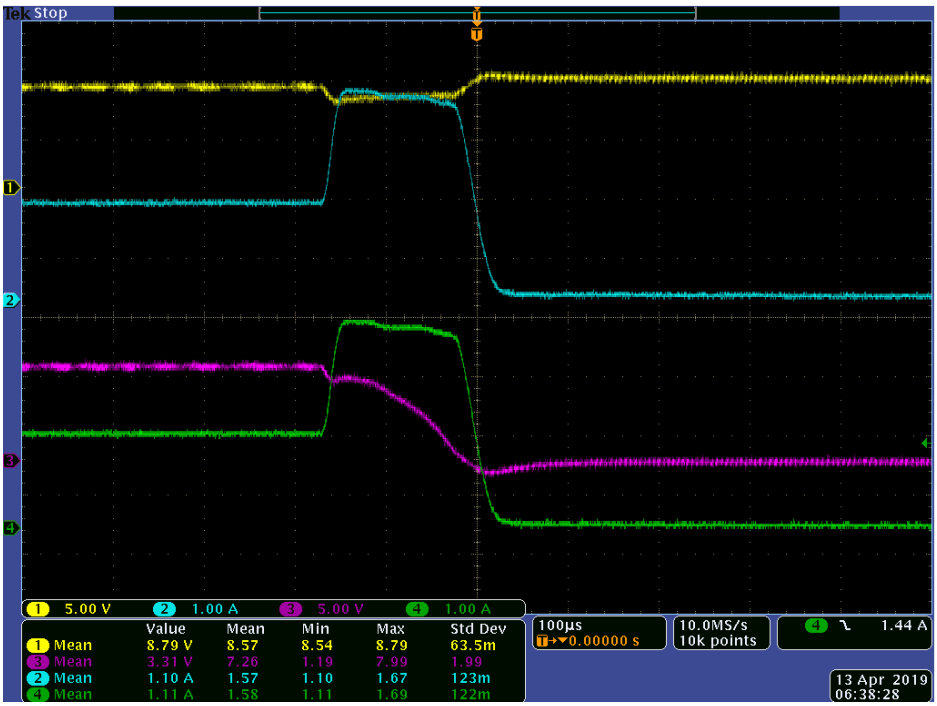

Figure 22: Vsys Hot-swap response to 2.5A over-current condition

Week	Andrew	Chris	Dan
2/18/19	Write Design Document	Write Design Document	Write Design Document
2/25/19	Master Module Schematic and Board Layout	Program the micro-controller to establish CAN bus communications	Program the micro-controller to establish I2C communications
3/4/19	Develop Power Control Board Layout	Finish micro-controller to establish CAN bus protocols, finalize CAN-grammar	Establish I2C communications with the Power Controller on development boards
3/11/19	Finalize Power Control Board Layout	Write code to simulate the battery pack on I2C and simulate C+DH on CAN bus	Write code for micro-controller. Focus on analog and 1 bit control signals
3/18/19	Spring Break	Spring Break	Spring Break
3/25/19	Soldering Power Controller Components onto the PCB	Soldering Power Controller Components onto the PCB	Soldering micro-controller onto to PCB
4/1/19	Soldering Power Controller Components onto the PCB, test operation	Soldering Power Controller Components onto the PCB, test operation.	Soldering micro-controller onto to PCB, test operation.
4/8/19	Testing Power Components, Troubleshooting	Testing micro-controller operation, troubleshooting, refine simulated systems.	Testing micro-controller operation, troubleshooting, refine simulated systems.
4/15/19	Demonstration Refinement	Demonstration Refinement	Demonstration Refinement
4/22/19	Write Report	Write Report	Write Report
4/29/19	Write Report	Write Report	Write Report

Figure 23: Schedule of Design and Production.