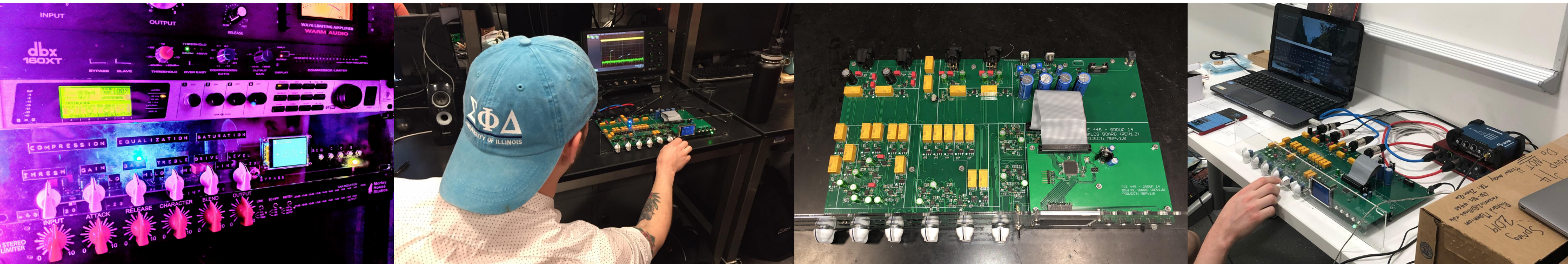


# Master Bus Processor

Group 14 - Clay Kaiser, Philip Macias, Richard Mannion  
ECE 445 - TA: Zhen Qin

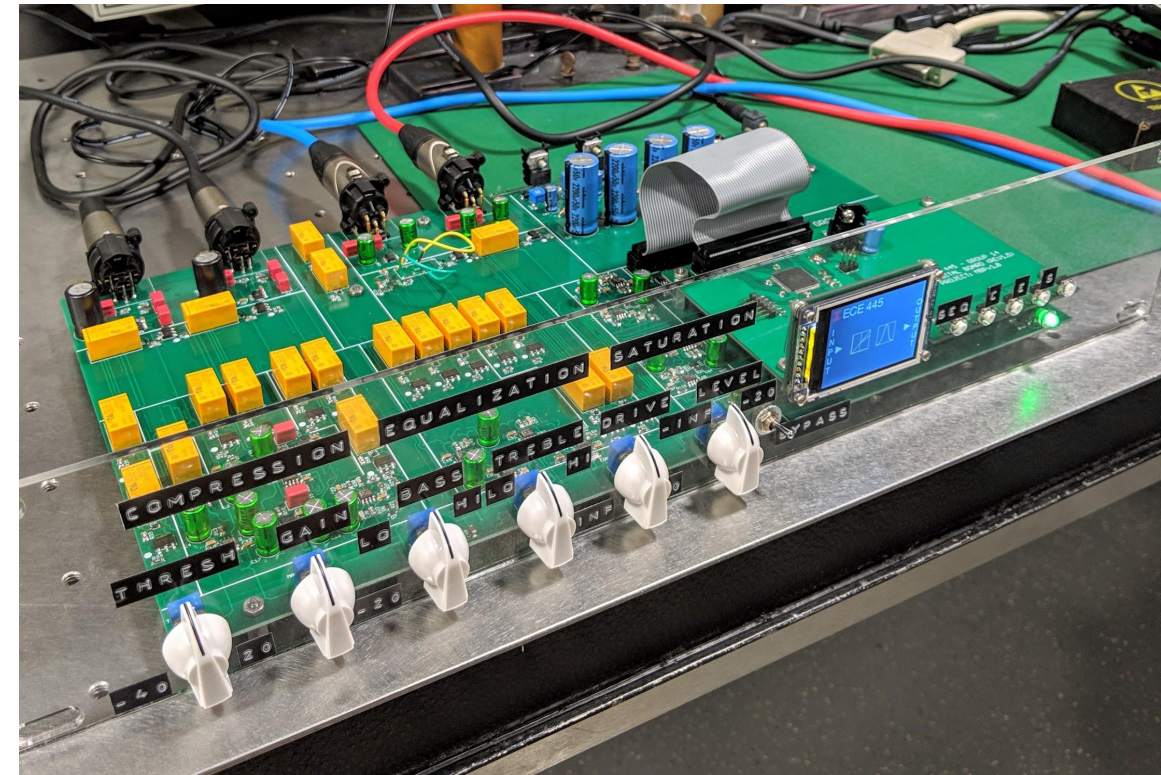


**I** ILLINOIS

Electrical & Computer Engineering  
COLLEGE OF ENGINEERING

# Introduction

- Why Analog?
  - Many Musicians and Audiophiles find it “much deeper and fuller”
  - Reduces the number of digital/analog conversions
- Existing Product → Rupert Neve Portico II
  - Too Expensive → \$4000
  - Not Flexible → Audio chain constant
- Want a Hybrid
  - Flexibility of Digital Control
  - Fidelity of Analog Processing
  - Breakdown Cost Barrier
    - leverage modern design techniques

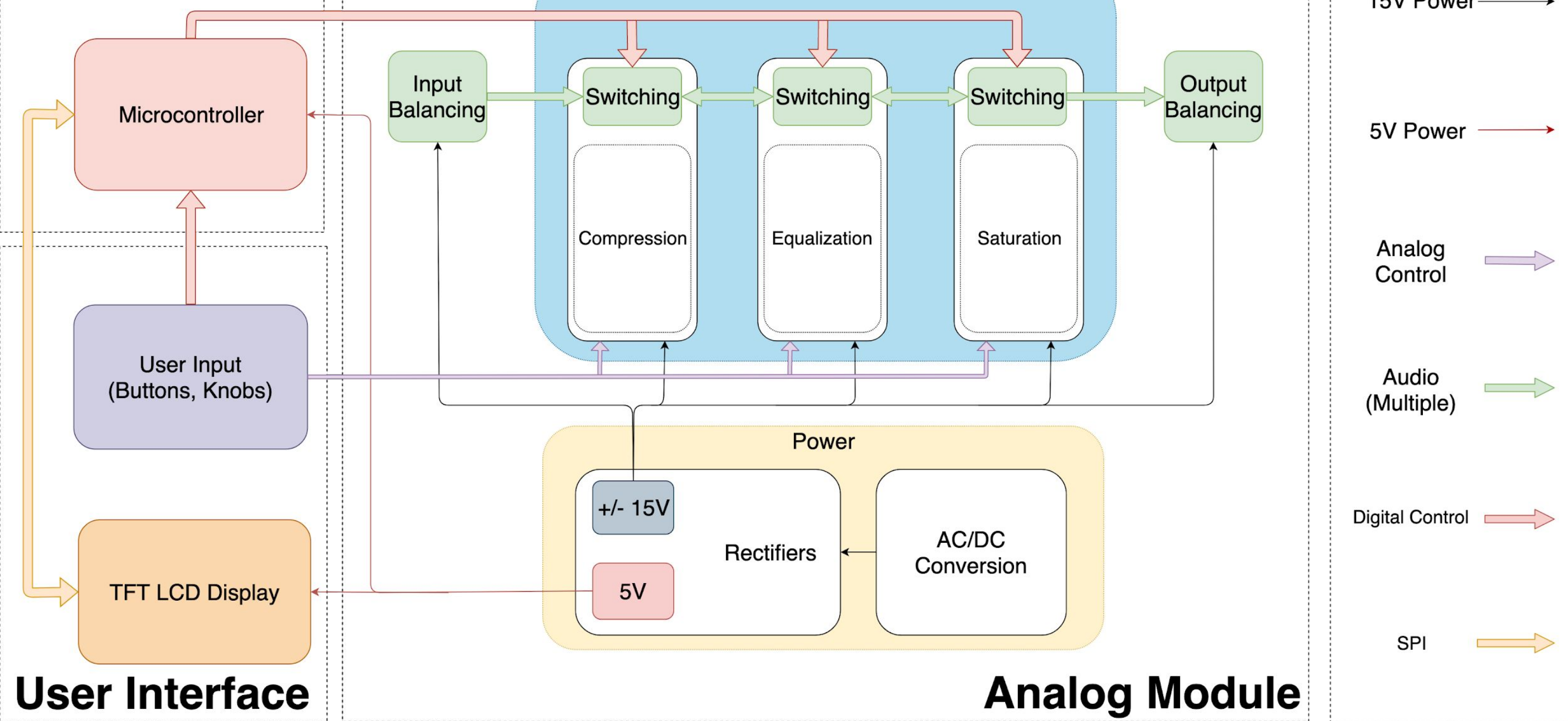




# Objective

- Affordability
  - Sub \$2500 price point → prototype has \$500 in parts
- Performance
  - **Compression**: automatic gain control
  - **Equalization**: filter banks
  - **Saturation**: harmonics
- Accessibility
  - 2 knobs per analog block
  - 5 buttons total with LCD display

# Digital Module



# Design: Power Conversion and Rectification

- ***Requirement:*** Convert 120 V AC to 18-30 V DC
- ***Verification:*** Measure voltage with max load (14 relays on)
- ***Result:*** DC voltage measurement of 26 V

# Design: Voltage Regulation

- **Requirement:** Provide 1.8 V to 5.5 V for digital control, -15.8 V to -14.0 V for negative rail and 14.0 V to 15.8 V for positive rail for analog blocks
- **Verification:** Measure voltage with max load (14 relays on)
- **Result:**

Desired Voltage	5 V	15 V	-15 V
Measured Voltage	5.07 V	14.87 V	-15.01 V

# Design: Compression

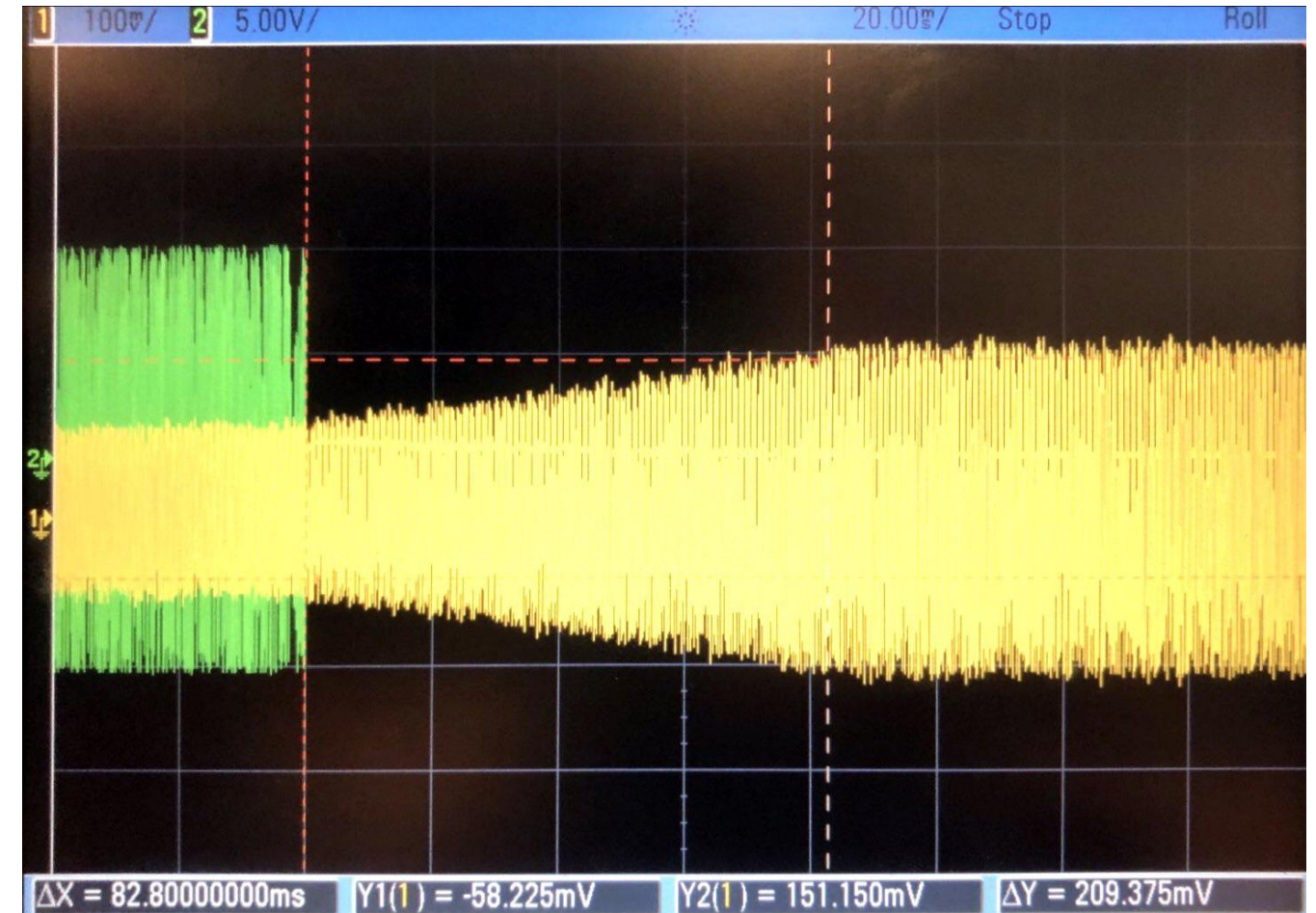
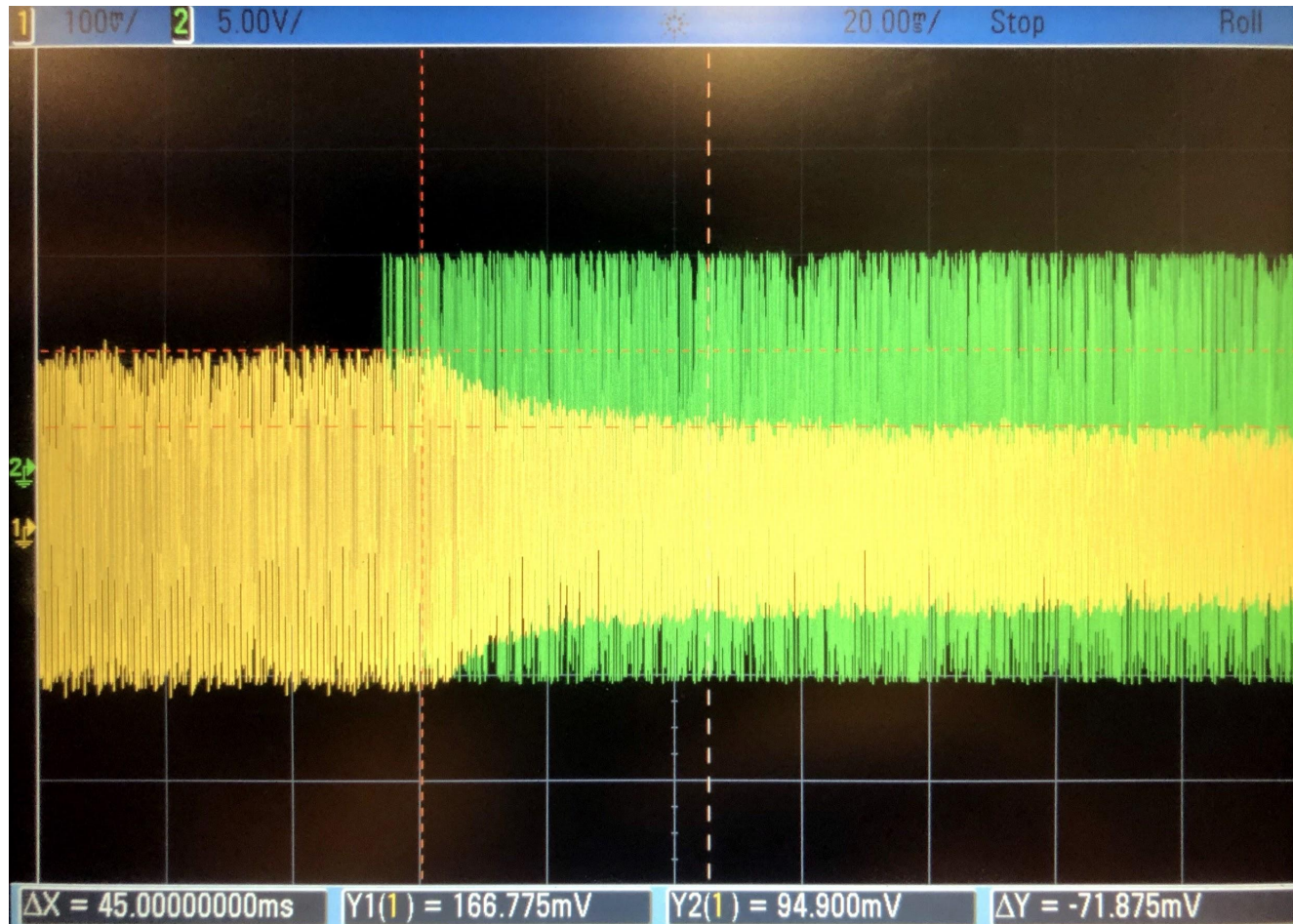
- ***Requirement:*** Provide 20 dB gain reduction
- ***Verification:*** Input 1 kHz sine wave and measure gain reduction
- ***Result:*** 20.3 dB gain reduction

# Design: Compression

- **Requirement:** Provide 100 ms response time
- **Verification:** Input signal signal over threshold on ch 2 and measure the response on 1 kHz sine wave on ch 1
- **Result:**
  - 45.0 ms attack
  - 82.8 ms release



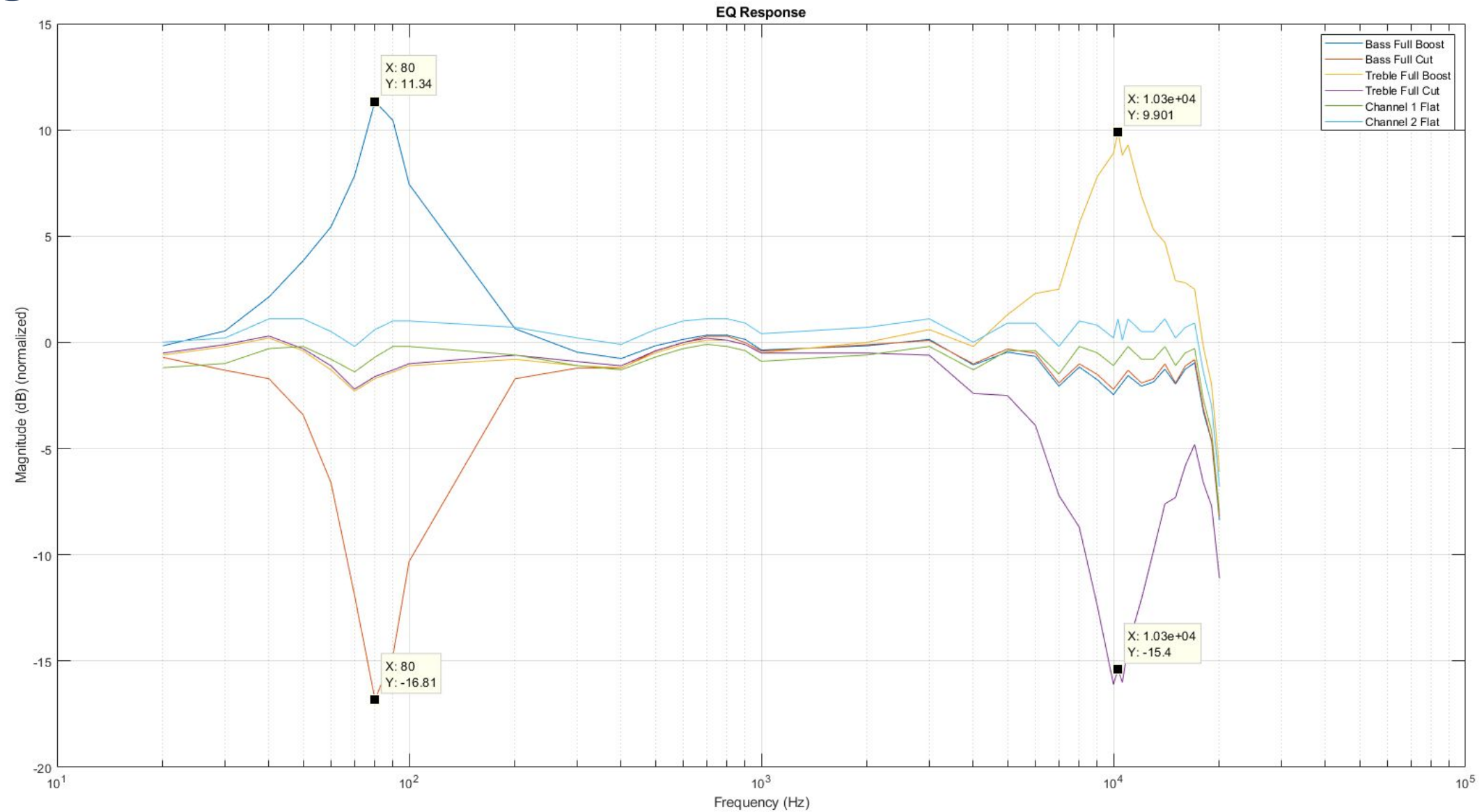
# Design: Compression



# Design: Equalization

- ***Requirement:*** Bands in the region of 70-90 Hz / 9-11 kHz
- ***Verification:*** Sweep input from 20 Hz - 20 kHz
- ***Result:***
  - Low Band Center Frequency of 80 Hz
  - High Band Center Frequency of 10.3 kHz

# Design: Equalization





# Design: Saturation

- **Requirement:** Contribute 0-10% total harmonic distortion
- **Verification:** Input 3 kHz input and measure harmonics
- **Result:** With full drive/level

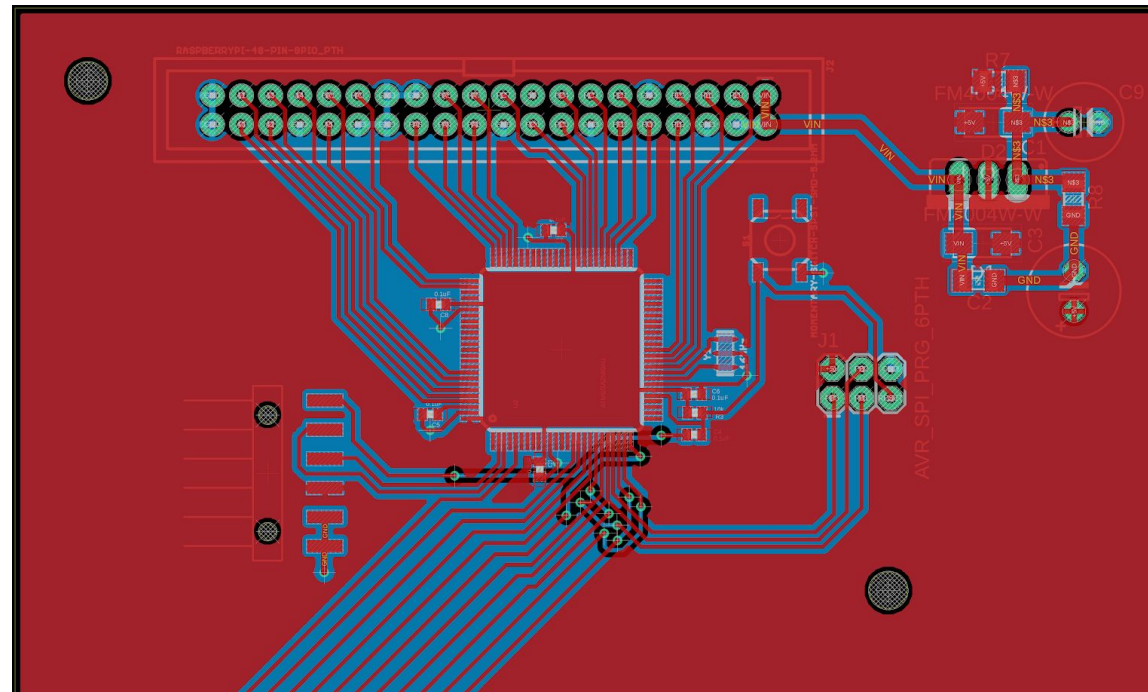
$$\text{THD (percent)} = \frac{\text{total power of all harmonics above fundamental}}{\text{total output power of signal}}$$

$$\text{THD} = 0.1186 \%$$

Harmonic	1st	2nd	3rd	4th	5th	6th
Frequency	3 kHz	6 kHz	9 kHz	12 kHz	15 kHz	18 kHz
Gain (normalized)	0 dBm	-39.3 dBm	-30.6 dBm	-44.3 dBm	-37.9 dBm	N/A

# Design: Microcontroller

- **Requirement:** 20 output, 5 input, SPI, non-volatile memory
- **Verification:** Refer to datasheet and count pins
- **Result:** ATmega-1280 had all required pins

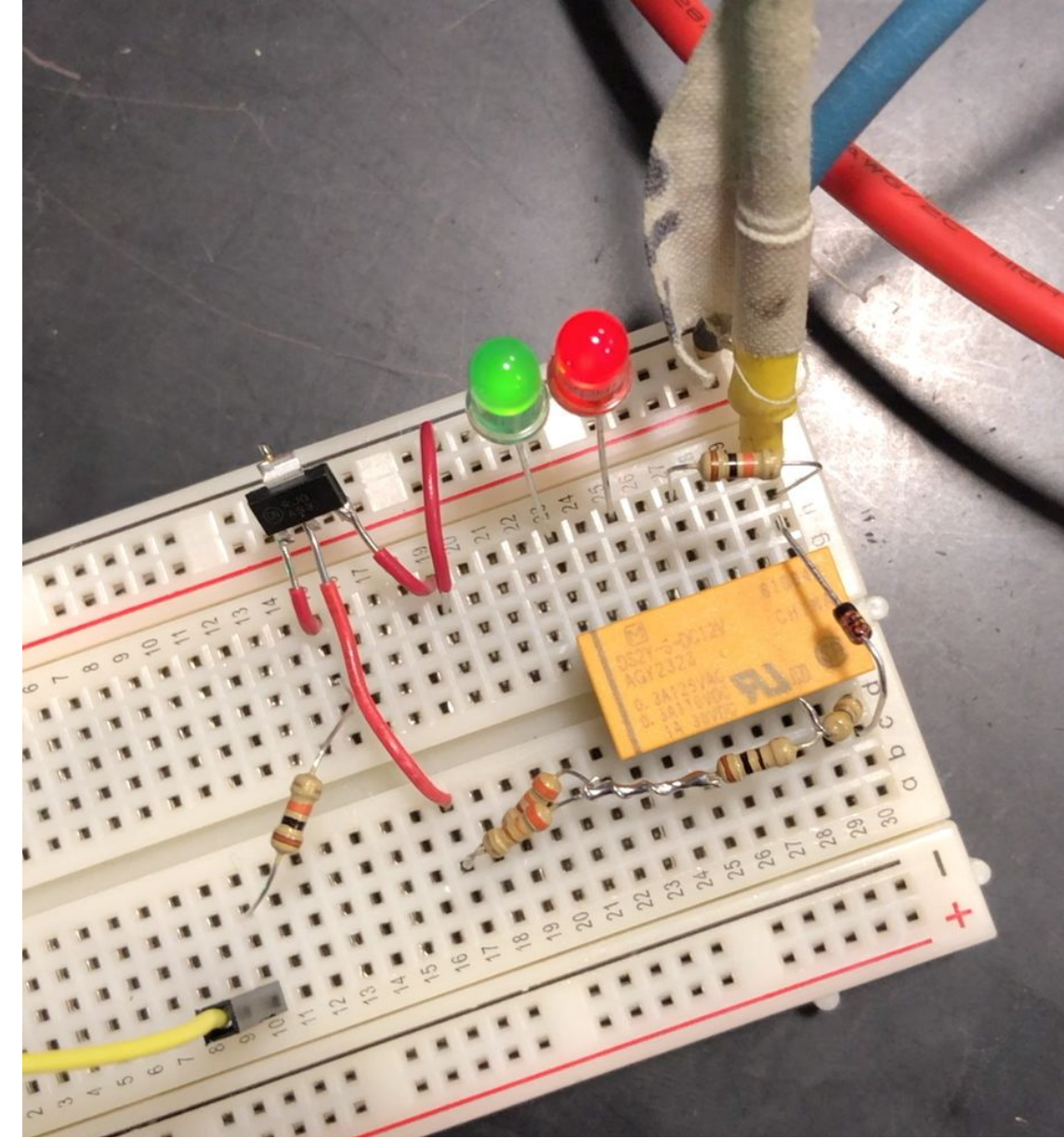
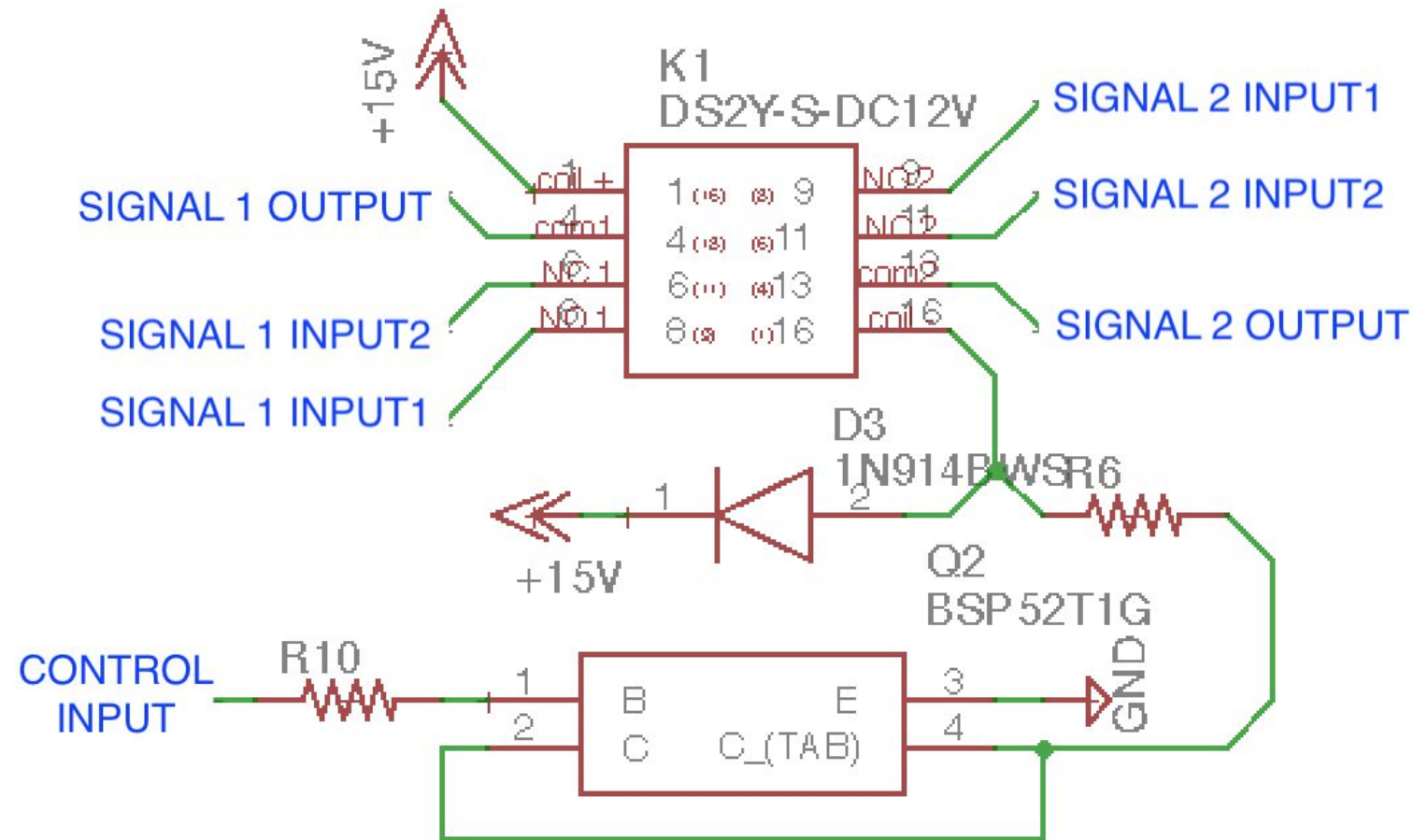




# Design: Switch Control

- **Requirement:** Less than 40 mA per line, 200 mA total
- **Verification:** Create test circuit and measure input current
- **Result:** Control line current of 0.371 mA
  - worst case of 14 relays on → 5.194 mA total

# Design: Switch Control

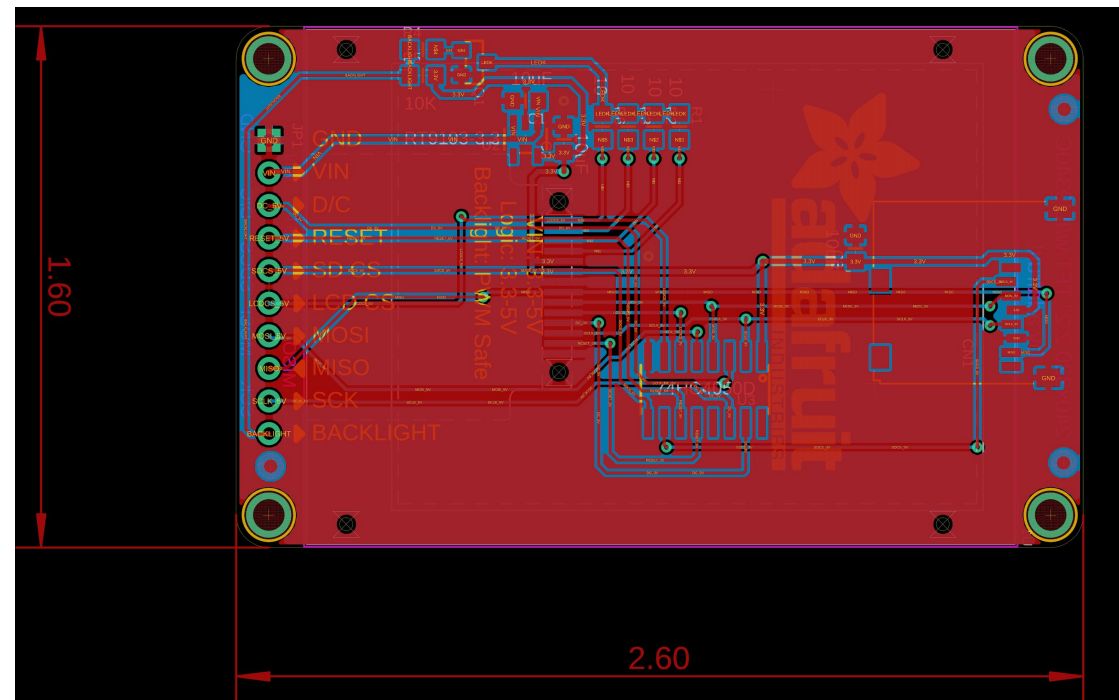


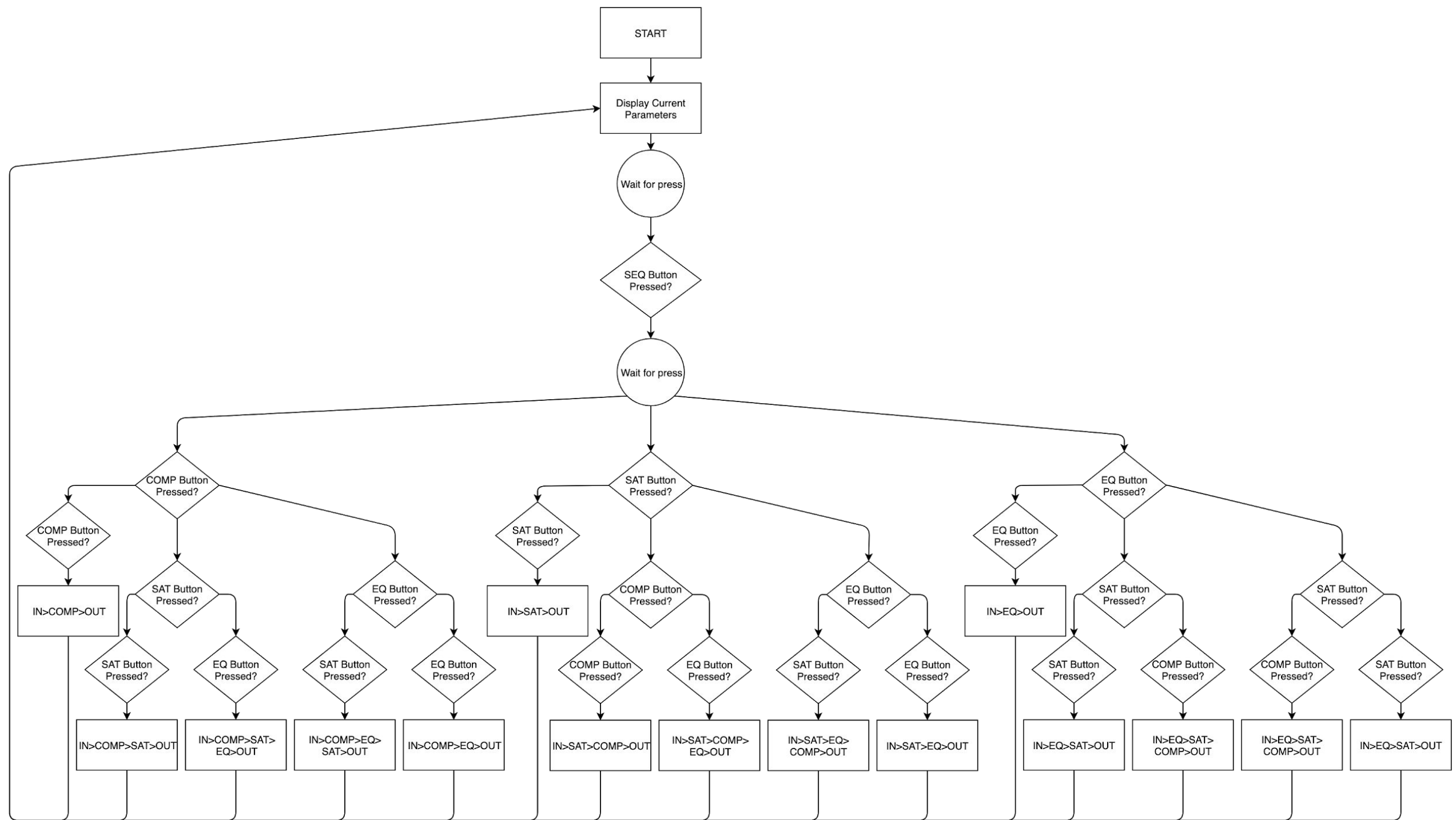
# Design: Switch Control

- ***Requirement:*** Must have less than 0.01% distortion
- ***Verification:*** Use max hold to measure distortion on frequency analyzer
- ***Result:*** No measurable distortion was detected

# Design: LCD Display

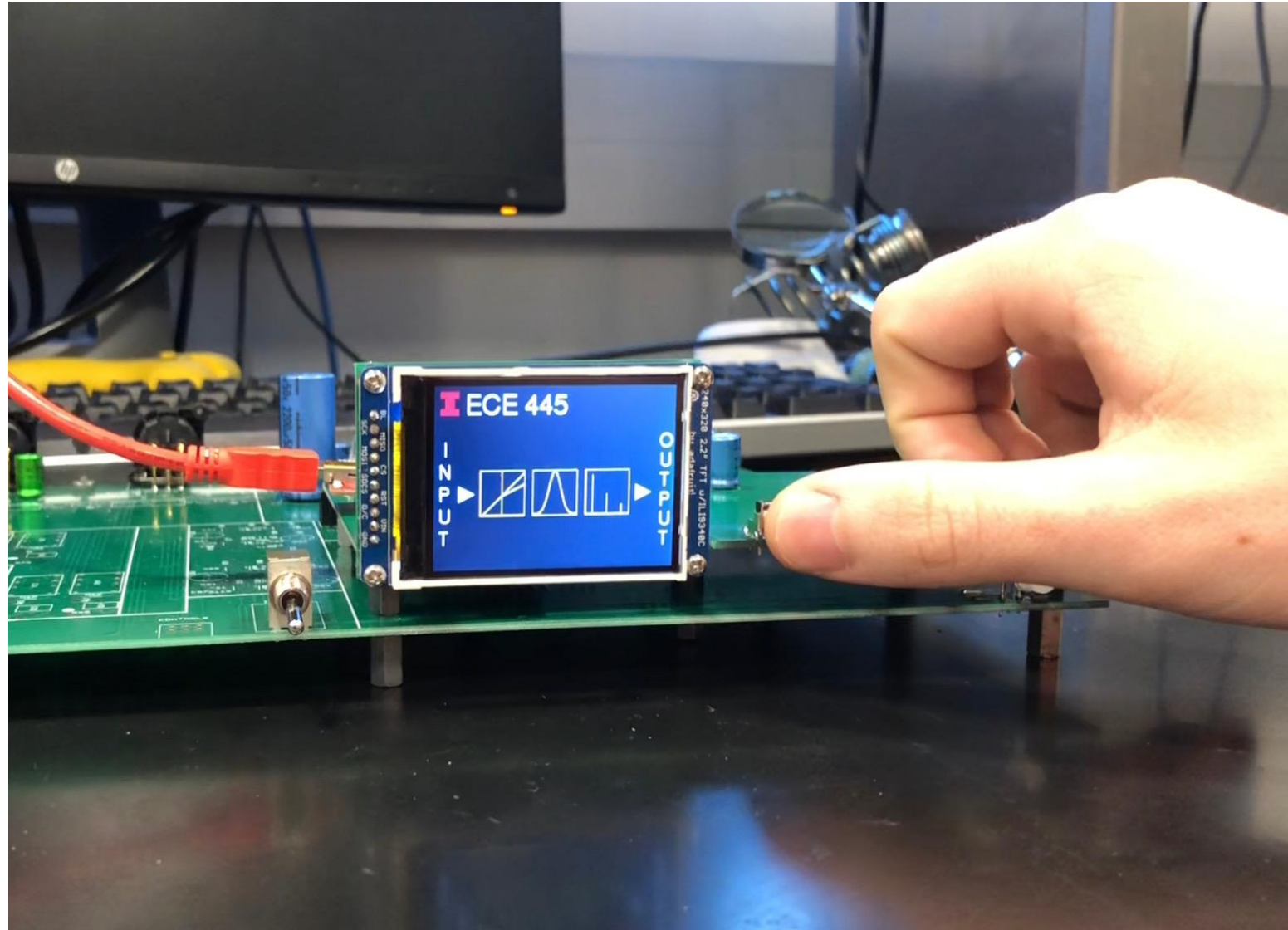
- **Requirement:** Must fit in a 1U space (1.75" tall)
- **Verification:** Use cad drawing to measure height
- **Result:** Measured height of 1.6" tall







# Design: UI



# Conclusion

- Requirements have been satisfied for all blocks!

## Future Work

- Monitoring and DSP functions
- Knob Recall
- Chassis
- Upgraded Processing Blocks

