Master Bus Processor

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ECE 445 - TA: Zhen Qin
Introduction

- Why Analog?
  - Many Musicians and Audiophiles find it “much deeper and fuller”
  - Reduces the number of digital/analog conversions
- Existing Product → Rupert Neve Portico II
  - Too Expensive → $4000
  - Not Flexible → Audio chain constant
- Want a Hybrid
  - Flexibility of Digital Control
  - Fidelity of Analog Processing
  - Breakdown Cost Barrier
    - leverage modern design techniques
Objective

- **Affordability**
  - Sub $2500 price point → prototype has $500 in parts

- **Performance**
  - *Compression*: automatic gain control
  - *Equalization*: filter banks
  - *Saturation*: harmonics

- **Accessibility**
  - 2 knobs per analog block
  - 5 buttons total with LCD display
Design: Power Conversion and Rectification

- **Requirement:** Convert 120 V AC to 18-30 V DC
- **Verification:** Measure voltage with max load (14 relays on)
- **Result:** DC voltage measurement of 26 V
Design: Voltage Regulation

- **Requirement**: Provide 1.8 V to 5.5 V for digital control, -15.8 V to -14.0 V for negative rail and 14.0 V to 15.8 V for positive rail for analog blocks
- **Verification**: Measure voltage with max load (14 relays on)
- **Result**: 

<table>
<thead>
<tr>
<th>Desired Voltage</th>
<th>5 V</th>
<th>15 V</th>
<th>-15 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured Voltage</td>
<td>5.07 V</td>
<td>14.87 V</td>
<td>-15.01 V</td>
</tr>
</tbody>
</table>
Design: Compression

- **Requirement:** Provide 20 dB gain reduction
- **Verification:** Input 1 kHz sine wave and measure gain reduction
- **Result:** 20.3 dB gain reduction
Design: Compression

- **Requirement:** Provide 100 ms response time
- **Verification:** Input signal signal over threshold on ch 2 and measure the response on 1 kHz sine wave on ch 1
- **Result:**
  - 45.0 ms attack
  - 82.8 ms release
Design: Compression
Design: Equalization

- **Requirement:** Bands in the region of 70-90 Hz / 9-11 kHz
- **Verification:** Sweep input from 20 Hz - 20 kHz
- **Result:**
  - Low Band Center Frequency of 80 Hz
  - High Band Center Frequency of 10.3 kHz
Design: Equalization
Requirement: Contribute 0-10% total harmonic distortion
Verification: Input 3 kHz input and measure harmonics
Result: With full drive/level

$$\text{THD (percent)} = \frac{\text{total power of all harmonics above fundamental}}{\text{total output power of signal}}$$

<table>
<thead>
<tr>
<th>Harmonic</th>
<th>1st</th>
<th>2nd</th>
<th>3rd</th>
<th>4th</th>
<th>5th</th>
<th>6th</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>3 kHz</td>
<td>6 kHz</td>
<td>9 kHz</td>
<td>12 kHz</td>
<td>15 kHz</td>
<td>18 kHz</td>
</tr>
<tr>
<td>Gain (normalized)</td>
<td>0 dBm</td>
<td>-39.3 dBm</td>
<td>-30.6 dBm</td>
<td>-44.3 dBm</td>
<td>-37.9 dBm</td>
<td>N/A</td>
</tr>
</tbody>
</table>

THD = 0.1186 %
**Design: Microcontroller**

- **Requirement:** 20 output, 5 input, SPI, non-volatile memory
- **Verification:** Refer to datasheet and count pins
- **Result:** ATmega-1280 had all required pins
Design: Switch Control

- **Requirement:** Less than 40 mA per line, 200 mA total
- **Verification:** Create test circuit and measure input current
- **Result:** Control line current of 0.371 mA
  - worst case of 14 relays on → 5.194 mA total
Design: Switch Control
Design: Switch Control

- **Requirement:** Must have less than 0.01% distortion
- **Verification:** Use max hold to measure distortion on frequency analyzer
- **Result:** No measurable distortion was detected
Design: LCD Display

- **Requirement:** Must fit in a 1U space (1.75” tall)
- **Verification:** Use cad drawing to measure height
- **Result:** Measured height of 1.6” tall
Design: UI
Conclusion

- Requirements have been satisfied for all blocks!

Future Work

- Monitoring and DSP functions
- Knob Recall
- Chassis
- Upgraded Processing Blocks