ECE 445

SENIOR DESIGN LABORATORY

DESIGN DOCUMENT

LASSI POWER BOARD

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March 8, 2019

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1 Introduction

1.1 Objective

Our sponsor, the Laboratory for Advanced Space Systems at Illinois(LASSI) run by Professor Lembeck, is currently designing the Illini-Sat 3; their next generation model of CubeSats. We have been tasked with designing the power board for this satellite design. This power board must provide regulated voltages from the solar panels and battery and ensure the battery is in operational parameters. The power board needs to be able to measure the power system parameters for telemetry purposes. Additionally, it must provide control measures to energize or secure loads as required through the interface. The system will interface to the rest of the satellite over a controller area network (CAN-bus).

1.2 Background

The current power board used by the Illini-Sat 2 was developed for over a 2.5 year period and carried an impressive array of features[1]. Professor Lembeck wants the next generation board to have a more streamlined design such that it can be easily integrated into future systems. As a result, this new power board will be designed to be as reliable as possible. Since the rest of the satellite is still being developed, this power board design will serve as a baseline for future iterations. As this is the first design, we are aiming for a single channel design which can easily be scaled to meet the future requirements of the satellite; so additional modules can be added. Our board will serve as a test channel for the design and development of other modules.

1.3 High-level Requirements

1. From solar panels which output output a nominal voltage of 17 VDC which can range from 5.4 to 21.3 VDC, provide regulated DC bus power rails, at 7.6 VDC(nominal[1]) and 3.3 VDC (+/-.2V), to support on-board instrumentation as well as provide means for on-board battery charging.

[1]This voltage shall change based on the battery state of charge and will vary within a wide band.

2. Provide a control system which can read voltage and current readings from essential points on the power board and can communicate with the Control and Data Handling Board(C+DH) via CAN-bus protocol.

3. Provide protective features[2] for the system to maximize resiliency of the power supply in case of fault conditions. This will include a watchdog timer which can reset the controller in the event of a fault.

1.4 Modifications

1.4.1 Updates from the Illini-Sat2 Power Board

We have de-conflicted the role of the battery as a filtration device, by incorporating a more robust passive component scheme. Additionally, providing a means by which the battery can be utilized as an energy source only when required by the overall system conditions. This means that the battery is not required to run the satellite while it is illuminated. This ensures that satellite can operate with reduced functionality even if the battery fails.

1.4.2 Updates from Proposal

Through research of the capabilities of our micro-controller, we have found that we no longer need a multiplexer or a decoder. Our micro-controller has enough unused resources that it will be able to easily scale with future iterations of the Illini-Sat3 power board.

We have resolved the issue of constant battery utilization that was present in the Illini-Sat2 Power Board. We have gone from a Buck to a Buck/Boost Topology to accommodate any future configurations for CubeSat platforms.

[2]Full description of protective features is discussed in detail in the design portion of this document, qualitative requirements are discussed in great detail there.

2 Design

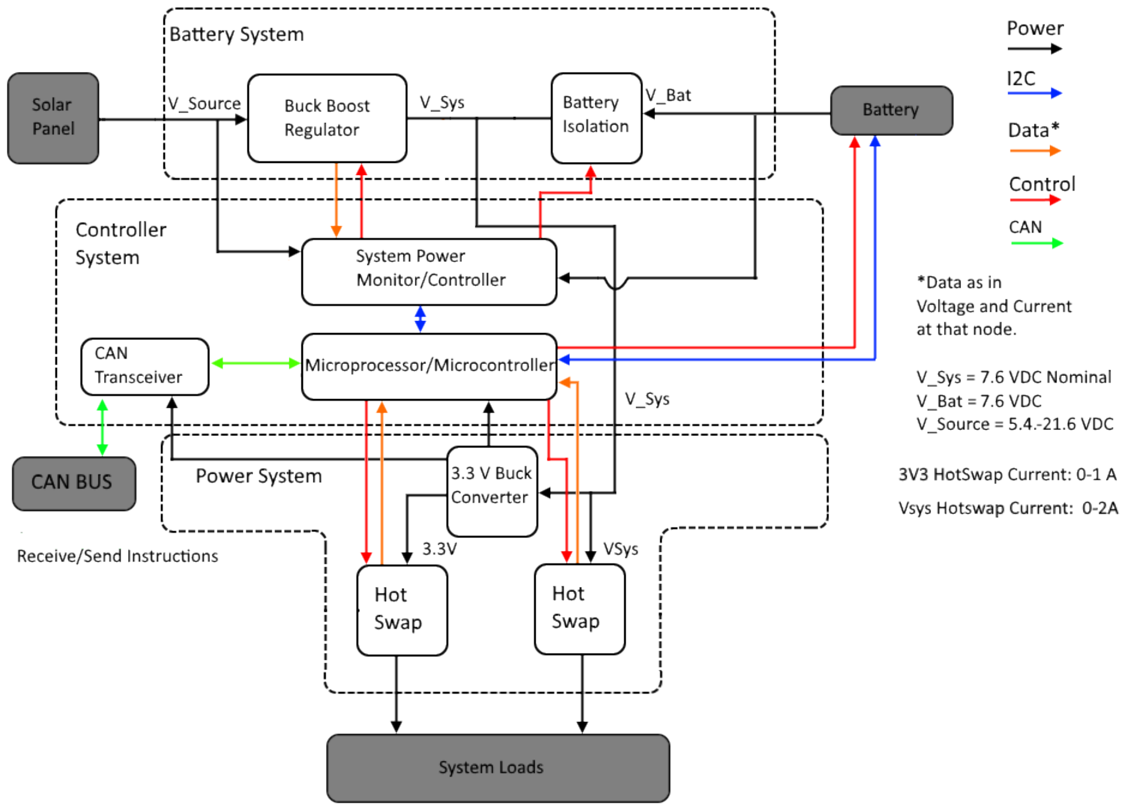

Figure 1: High Level Block Diagram.

2.1 Overall System Operation

Our overall system is composed of three subsystems: the Battery System, the Control System, and the Power System. The Battery system takes in an input voltage source from the solar cells, which can range from 5.4 to 21.6VDC. The exact value cannot be specified as different solar cell configurations will be used by different satellites. A Buck Boost Regulator will regulate the voltage on the V_{Sys} bus. The V_{Sys} and V_{Bat} bus operates between 6.144 to 8.4 VDC depending on the battery state of charge. The exact voltage will automatically be set by the Power Controller to facilitate proper battery charging. The Battery Isolation is a MOSFET which allows the battery to be electrically separated from the rest of the circuit if not required as it is also controlled by the Power Controller. It is important to note that the solar cells and the battery module are not within the scope of this power board and we will be using equipment provided by our sponsors for demonstration purposes.

The Control System interacts with the Battery System via the Power Controller. This controller will control the Buck Boost Regulator and the Battery Isolation MOSFET to ensure proper operation of the Battery Module. The Power Controller will send telemetry and receive instructions to the Micro-Controller module over the I2C bus. In addition, the Micro-Controller will communicate with the Battery Module off-board via and I2C bus to gather temperature readings. The Micro-Controller must be able to send single bit digital control signals to the heating element in the battery module and the two Hot-Swaps. The controller will also be able to make voltage readings of current sensors within the Hot-Swaps as well as measure the voltage of the 3v3 regulated bus. The Micro Controller will interact with the C+DH over a CAN bus through a CAN transceiver.

The Power System consists 3.3V Buck converter which will regulate the voltage of the 3v3 bus; even though V_{sys} can range from 6.144 to 8.4 VDC. The 3v3 bus will operate at 3.3 VDC nominal +/- 0.08V. The 3v3 Hot Swap will connect the the 3v3 bus to a regulated load. The V_{sys} Hot Swap which will connect the V_{sys} bus to an unregulated load as requested by our sponsor. The loads will be off board as they are outside the scope of our project.

2.2 System Power Monitor and Controller

The heart of the power board's design and functionality lies in the BQ25703.[2] This 4mm x 4mm chip provides means for controlling the majority of the control functions for the system's vital buses. It functions not only as the gate driver for all of the major power MOSFETS, but also implements a wide array of protective features which increases the reliability of the design.

2.2.1 Device Initialization

Upon energization, the power board is capable of self starting on battery or solar power. Meaning, in the unlikely event that the satellite's battery completely fails, it will still function whenever it is illuminated. The device will be configured such that it will automatically start all the system parameters pre-loaded to ensure operating tolerances will not be violated prior to the start-up of the system micro-controller. Once the mirco-controller is brought online, the optimal set-points will be provided through the I2C interface by the micro-processor, based on the current operating conditions.

Requirements and Verification

Initial Conditions for Solar Source	
Requirements	Verification
1) System can initialize and utilize solar source while the battery is disconnected from the system at 17.6 V +/- 3 V nominal. Solar source will	1) Isolate the battery from the system and have the simulated C+DH query the micro-controller. The return of system telemetry from the micro-controller will confirm this requirement has been met.

Initial Conditions for Battery Source	
Requirements	Verification
1) System can be energized from a battery source while solar cells are disconnected from the system.	1) Isolate the solar cells from the system and have the simulated C+DH query the micro-controller. The return of system telemetry from the micro-controller will confirm this requirement has been met.

The current iteration of the power board design is functionally incapable of operating without a battery. This device does not have this limitation and can run off of solar power alone due to the inclusion of a P-Mos isolation switch for the battery bus. The isolation will also provide a means in ensuring that the battery is never unintentionally discharged when the systems loads are being met by the solar source alone. As a result, this will significantly reduce the number of battery charge cycles, the average depth of battery discharge, and will also serve to extend the system's battery life.

Table 1: Average Power Generation and Payload Data

Configuration	Avg Bus Power Generated W	Avg Bus Power Required W	Avg Payload Power Allowed W
1.5U	2.85	1.5	1.35
2U	3.8	2	1.8
3U	6.65	2	4.65
6U	9.3	2.5	6.8

The system will however, be capable of immediately meeting power demand by supplementing with the battery, should this be necessary. Based on the data available for solar panel sizing vs. system demand, *Table 1* it is clear that the battery is only needed as a supplemental role.

2.2.2 Device Protection

1. WatchDog Timer

   The WatchDog Timer will open the battery MOSFET and terminate charging in the instance of loss of communications with the micro-controller. This ensures battery protection if the device control is lost. The Watchdog timer will be reset when communications are re-established with the micro-controller.

2. Input Over Voltage Protection

   Should the solar panels' input voltage rise above 23.5V, the chip will enter an over voltage condition. Here the switching regulator will be de-energized and system loads will be powered by the battery. If the battery is already disabled by another protection, this will disable the satellite.

3. Input Over Current Protection

   In the event of an over-current condition, defined as 125 percent of the input current set point, the switching regulator will be turned off for a set period of time. This will result in the system cycling power.

4. System Over Voltage Protection

In the event that System Bus Voltage (V_{sys}) exceeds 12 volts, the switching regulator will be turned off. The system bus will be powered by the battery, maintaining power continuity. The switching regulator will be re-enabled by the micro-processor.

Requirements and Verification Protections

WatchDog Timer	
Requirements	Verification
1) The WatchDog timer will time out when the BQ25703 does not receive the proper communication from the micro-controller.	1) Issue a halt command to the micro-controller to prevent it from issuing proper instructions; which will cause the WatchDog Timer to time out and securing battery charging. We will verify this by observing the gate drive voltage for the battery isolation MOSFET (pin 21 BQ25703A). The voltage will be driven high.

Input Over Voltage Protection	
Requirements	Verification
1) This protection will have the device go into over voltage protection when device exceeds the voltage set point. 2) We will accomplish this by decreasing the input over voltage set point to within the *normal operating band**, verifying the switching regulator has been de-energized by observing gate voltages for the four MOSFETs. This is a discrete test.	1) When the input rises above the setpoint the system will secure operations to the switching regulator. Subsequently, the regulator will remain de-energized until the voltage drops below the set point.

Input Over Current Protection	
Requirements	Verification
1) This protection will have the device to go into over-current protection mode when input current exceeds device's set point.	1) Decrease the input over current protection set point to within *normal operating band**. Observe that the switching regulator will de-energize by observing gate voltage. This is a discrete test.

System Over Voltage Protection	
Requirements	Verification
1) This protection will cause the system to go into over-voltage protection mode when the system's voltage exceeds system's set point.	1) Decrease the over voltage protection set point to within *normal operating band**. Observe that the switching regulator will be de-energized and not re-energize until a proper control signal is sent by the micro-controller. This can be verified by measuring gate voltage.

***Note**: Due to the nature of these protective features, we will not be testing protective features at their design set point and will be reducing the set point to a normal operating condition in order to cause these protection features to occur and verify that the protection action operates properly. We will be restoring design to the normal set points afterwards. Voltages will be measured with an oscilloscope with reference to board ground. Absolute over current will not be tested for device safety. If current exceeds 160% IMax, the device should be shut off. Testing this functionality unnecessarily jeopardizes the circuit and this potential destructive testing is not required nor desired.

2.2.3 Modes of Operation

1. System Voltage Regulation

   The battery MOSFET will be switched off, disconnecting the battery from the system bus. This will provide a regulated voltage to the system when power from the battery is not required or desired.

2. Battery Charging

The battery MOSFET will be switched on, allowing the system to charge the battery in constant current (CC) and constant voltage mode (CV) at 4.2 volts per cell.

3. Battery Power

   The battery MOSFET is configured such that if power to the loads from the solar cells is insufficient, the battery will begin to discharge to supplement the load. Additionally, in eclipse conditions, the switching regulator will be fully de-energized and all power will come from the battery.

4. Reverse Power Mode

   Due to the symmetrical nature of the 4-switch buck boost converter Topology, bi-directional power flow is functionally possible. However, this function will be prohibited by placing the EnOtg pin to ground [2].

Requirements and Verification

System Voltage Regulation	
Requirements	Verification
1) System regulates output voltage to the Vsys bus between 6.14V and 8.5V without the aid of the battery. System can initialize and utilize solar source while the battery is disconnected from the system.	1) Measure the average voltage reading using an oscilloscope. This test is intended to show the voltage regulation ability of the system with the battery disconnected. A DC power source will be applied to the input of the circuit and the V_{sys} output will be connected to a power resistor for constant load conditions. DC source will be swept from 5.4 volts to 20 volts in one volt increments. No data points shall be outside of the specified range.

Test Setup for Battery Charging Requirements and Verification: An electronic load will be connected to the battery terminals with a constant voltage of 17.6V at the input. The electronic load will be placed in constant voltage mode at the battery terminals. The voltage at the battery terminals will be varied in .5 volt increments starting at 4V and concluding at 10 volts.

Battery Charging	
Requirements	Verification
1) Utilizing a programmable load, the full charging sequence is demonstrable from LDO mode to constant current and constant voltage mode.	1) Simulating a battery, confirm the full operations of the BQ25703 charging operation cycle by using an oscilloscope to show the charging sequence is executed properly. [2] a) Prior to reaching 5V at the battery terminal, the BATFET shall be off and the current into the load should be zero. b) At the 5.5 volt level the battery will charge in LDO mode. This will be indicated by a charge current not to exceed 500mA. c) Constant current charging mode is verified between 6.5 and 8.0 V. At these data points current into the battery should be maintained at 1A (+/- 100mA). d) From 8.0 V to 9.0V, data points will be taken more frequently. At 8.2V (+/- .1V), the charger will enter constant voltage mode. This is demonstrated by current into the load decreasing over each subsequent voltage step until termination at 8.4 (+/- .1 V). e) At the point that current goes to zero, only one more test point will be required to verify the BATFET stays off when voltage is greater than 8.4(+/- .1 V).

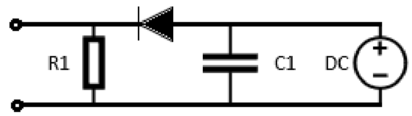

Figure 2: Battery simulation test setup for Battery Power RV.

Test Setup for Battery Power Requirements and Verification: This verification procedure requires two DC power supplies and an electronic load to perform. A DC power supply with a voltage setting of 10 V will be utilized at the solar panel input. A power supply connected to the battery terminal will be connected as seen in fig. 2. C1 is a $47\mu F$ capacitor. The diode is placed at this terminal such that the power supply will not become reverse powered by the DC power supply. The resistor is in place to ensure a path for current from either source when the electronic load is at a low current draw. The battery bus power supply will be operating such that voltage at the V_{bat} sensing node is at 8.4V (indicating a fully charged battery). An electronic load will be connected at the V_{sys} bus. This load will be set at a constant voltage value to match V_{bat}. Voltage will be read at V_{bat} and V_{sys}. Current will be measured using a hall-effect probe on the output of the battery power supply.

Battery Power	
Requirements	Verification
1) The battery will transition from System Voltage Regulation Mode, to Battery Supplement Mode, to Battery Only Mode.[2].	1) VR mode verification. Set the E-load voltage at 8.5 V constant voltage. Verify BATFET is off by observing the battery current output. Then slightly increase the system load and verify that BATFET does not turn on. 2) Supplement mode verification. Lower E-load voltage to match battery terminal voltage such that minimal current (charging or discharging) is less than 50mA. Set solar input current limit to 1.2 A and slowly increase E-load current until solar supply is current limited (simulating reduced power output for solar cells). The BATFET shall turn on and the battery will discharge to maintain load demand. 3) Battery only mode verification. The solar source supply will be deenergized and the battery shall begin to discharge.

Reverse Power Mode	
Requirements	Verification
1) During testing sequence, make sure that Reverse Power Mode will not occur or be triggered.	1) Make sure the bit that's sent to the Reverse Power Mode is low and that no other function can cause the bit to be high.

2.3 4-switch Buck/Boost Converter

The selection of the DC-DC Converter topology is not a trivial decision point. Due to the wide range of possible satellite configurations, the regulator must be capable of handling a wide range of inputs. The most common application will have a nominal input voltage of 17VDC from the solar panel, but we must be able to accommodate an input up to 21.6VDC (for a 8 solar cell 6U configuration at peak efficiency). The minimum voltage is assuming a 1.5U design with one of the cells on each side not in operation; therefore a 5.4V input (nominal cell voltage for the solar cells is 2.7V). With these input voltage limitations, our design is sufficient. The battery configuration is a 2S/2P (Two-series, Two-parallel) with a nominal voltage of 7.6V utilizing INR18650 MJ1 3500mAh Li-ion cells [3]. The circuit will not be configured to support more series cells due to the impact this would have on downstream buck converter sizing. However, minimal rework would be required to redesign these portions of the board to accommodate more series batteries (up to four).

Table 2: 4-Switch Buck/Boost Switching Strategy Overview

	Buck	Buck/Boost	Boost
Q1	Switching	Switching	on
Q2	Switching	Switching	off
Q3	off	Switching	Switching
Q4	on	Switching	Switching
Vo/Vi	D	D/(1-D)	1/(1-D)

In order to accomplish a switching regulator capable of stepping up or down voltage, a 4-Switch Buck-Boost topology was chosen. This topology *Fig.3* operates either in buck mode, buck-boost mode, or boost mode based on the voltage transfer characteristic. As V_{in} approaches V_{out} from above or below, the converter will transition to a Buck-Boost switching strategy. This is to ensure a smooth transition from one voltage level to the other. However, it will cause the device to incur more switching losses due to the increased number of switches. Therefore as soon as the device is operating clearly as a buck or a boost, it will automatically enter into the appropriate mode to optimize efficiency. The output voltage of the converters will be based on the duty ratio of the high-side MOSFETS. *Please refer to Table 2 for an overview.* The Buck and Boost modes were also chosen to be synchronous in order to minimize the size of the inductor needed in the circuit while precluding discontinuous conduction mode under light loads.

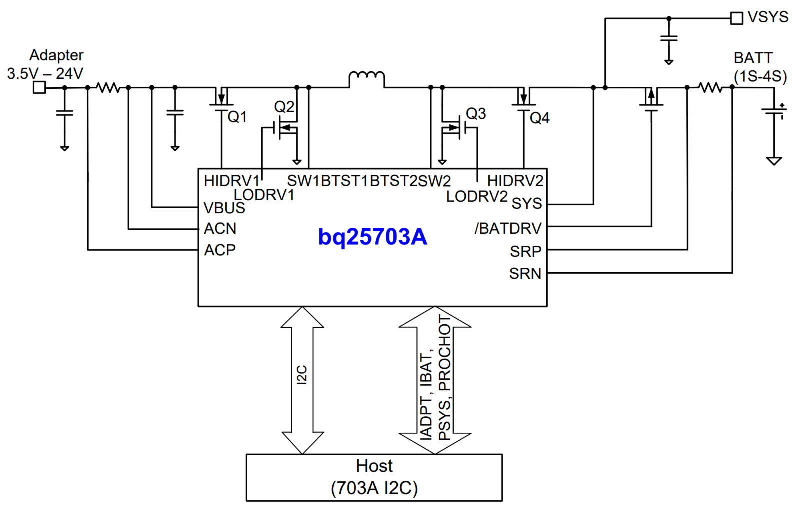

Figure 3: Application diagram from BQ25703 Data sheet[4].

The inductor for the buck-boost is a Wurth-Electronics[5] 2.2μF with a self resonance of 24MHz. An inductor should be operated at a frequency well below its self-resonance because beyond this point it will act like a capacitor. Hence this inductor is suitable for the switching frequency of 1.2 MHz. Additionally, it has a saturation current of 15.5 A which is greater than the rating of our solar panels. Additionally the foot print for this device is quite small (9.2mm x 8.5 mm) with a maximum height of 3.0mm.

The switching MOSFETs utilized are CSD17551Q3A [6] n-channel MOSFETs with a voltage rating of 30V and max current of 48A both in excess of what is required with a significant safety margin. Additionally the R_{dson} (Resistance drain-source) is minimal at less than $10m\Omega$ leading to low energy dissipation in the MOSFETs. These MOSFETs are additionally well matched for the gate driving current of the BQ25703A.

Requirements and Verification

4-switch Buck/Boost Converter
*The 4-switch Buck/Boost Converter operates in tandem with the System Power Monitor and Controller. The requirements of the Buck/Boost Converter are met by the verification steps for the System Power Monitor and Controller.

2.4 Step Down DC Voltage Regulator

The DC-DC Stepdown converter is implemented with a monolithic design. The TPS53515 is an integrated MOSFET synchronous Buck converter with a footprint of only $26mm^2$. The passive components around the Buck are sized to accommodate up to 10A drawn with an output ripple of less than 10mV when its supply rail is at 8.3V or 4.15V / cell. This ripple specification is in order to be well within the requirements of the on board micro-controller; supplied off of the 3V3 rail as well as to supply system 3V3 loads. As of yet, the number and size of 3V3 loads has not been decided for any future projects. Therefore this buck converter is intentionally overrated in order to test the limitations of the battery and solar converter at high loads. In order to accommodate a 10A load, while switching at a frequency of 416kHz, an output capacitive filter of $242\mu F$ will be constructed. In order to accomplish this without utilizing electrolytic capacitors, an unacceptable [1] practice for space applications, eleven $22\mu F$ ceramic capacitors will be used in parallel. This parallel arrangement will minimize the effect of the equivalent series resistance (ESR) of the capacitors. A $2.2\mu H$ inductor [7] was chosen to provide proper average forward current and current ripple sufficient to guarantee the voltage ripple specifications previously mentioned. This Coilcraft inductor is shielded to minimize leakage flux and interference and has core characteristics satisfactory for operation at 416kHz. Additionally it is shown that this inductor will not saturate at the maximum anticipated current of 10A.

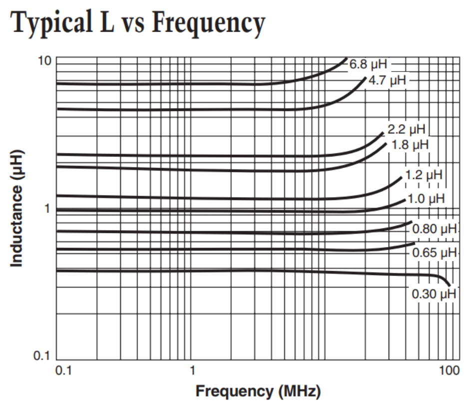

Figure 4: From Coilcraft data sheet[7]. Showing proper inductance at switching frequency for application

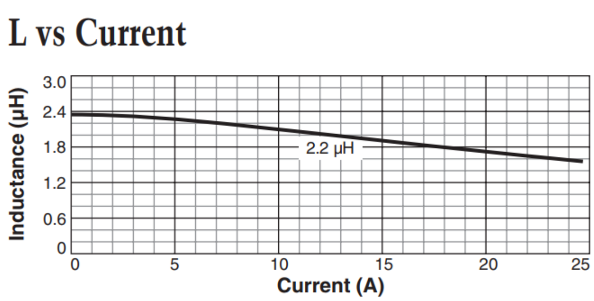

Figure 5: From Coilcraft data sheet[7]. Showing proper inductance at rated current for application

Requirements and Verification

Step Down DC Voltage Regulator	
Requirements	Verification
1) Average Voltage: Shall maintain output voltage at 3.3VDC average (+/-) 80 mV. Satisfies requirement for CAN-transceiver. 2) Voltage peak to peak shall not exceed 5%.	1) Will observe average voltage output over operating range of 3V3 hot-swap with an oscilloscope and verify condition is not violated. 2) Will be performed in conjunction with the average voltage test.

2.5 Hot-Swaps

The design of this power board is fitted with two TPS2420[8] hot-swap controllers. One controller will provide an unregulated V_{sys} supply while the other is for the 3v3 bus. The next generation of Illinois CubeSats is in the early stages of development therefore the board will simply produce two controlled outputs for demonstration and testing purposes. Both of the Hot-Swaps will have a 19.45mSec fault delay in case of a transient over-current condition. This value was determined to be sufficient for testing by our Sponsor. Setting the time delay is as simple as using eqn. 1. In this case we have chosen a .5uF capacitor to set the appropriate fault delay.

$$C_{ct} = \frac{T_{fault}}{38.9e3} \tag{1}$$

The design the V_{sys} hot-swap required an over-current (OC) of 3A[1]. Therefore a $65.5k\Omega$ resistor is connected per eqn 2. This is the absolute OC set point for the device. I_{fault} is transient set point and will occur after a time delay of approximately 20mSec as previously discussed. This was set at 1A less the absolute max setpoint to facilitate testing per eqn 3. This gives a resistance value of $100K\Omega$.

$$R_{Imax} = \frac{201K\Omega}{I_{max}} \tag{2}$$

$$R_{Ifault} = \frac{200K\Omega}{I_{fault}} \tag{3}$$

The 3V3 hot-swap was designed in the same fashion except that the max current set point is 2A and the transient set point is at 1A. This gives $R_{Imax} = 100K\Omega$ and $R_{Ifault} = 200K\Omega$.

Requirements and Verification

Hot-Swaps	
Requirements	Verification
1) Transient Over-Current: Shall secure power to the load if the transient over current setpoint is exceeded within 40mSec. 2) Imax Over-Current: Shall secure power to the load within 40mSec and not allow current to exceed the absolute limit 2A for the 3V3 hot-swap and 3A for the Vsys hot-swap. 3) Both hot-swaps will be energized and secured with control from the micro-controller.	1) For both hot-swaps, this functionality will be tested by adjusting current to 1.5A for the 3V3 hot-swap and 2.5A for the Vsys hot-swap. The load will be simulated with a variable load. The resistance will be lowered raising the current. The current will be calculated using Ohm's law and by measuring the voltage drop across the load. 2) Repeat part 1 but adjust the current to 2.5A for the 3V3 hot-swap and 3.5A for the V_{sys} hot-swap. 3) This verification is met in the micro-controller verification section.

2.6 Micro-Controller

In order to coordinate the various components of the power board, we need a micro-controller that is capable of communicating through I2C and CAN bus protocols, has an internal WatchDog timer, and at least 6 General Input and Output Pins(GPIO) which are capable of Analog to Digital conversion(ADC). As such, the control system on the power board will be run by a STMicroelectronics STM32F072RB micro-controller[9]. We have coordinated with our sponsor and have agreed that this micro-controller is the best fit, as it fulfills all of our requirements. In addition, the STMicroelectronics controllers have a good track record at a reasonable cost.

The controller will directly interface with the various components on the board. *fig. 10* Our implementation leaves many of the resources of the controller open; which will allow future groups to easily scale up the size of the power system. This meets one of the high level requirements of the project as there are 9 remaining Analog to Digital Pins as well as 29 remaining Digital I/O pins.

Upon energization, the micro-controller will execute an initialization sequence. Here the micro-controller will set the required parameters of the Power Controller. Then it will establish contact and alert C+DH to notify that system has been reinitialized. After the initialization sequence, the micro-controller will enter the main sequence of operation. First, the controller will check to see if it has received instructions from the C+DH and carry out the instructions accordingly. In our implementation, the C+DH will only instruct the micro-controller to set the Hot-Swaps, change the parameters of the Power Controller, or to test the WatchDog timer. Normally, after every operation our micro-controller will reset its internal WatchDog timer. However, in this test function we will set the micro-controller in an infinite loop until the timer re-initializes the micro-controller. This function will be included for testing purposes only. Second, if there are no instructions from the C+DH, the micro-controller will gather all the necessary system telemetry data from the Power Controller as well as reset the Power Controller's WatchDog Timer. If the Power Controller's System Over Voltage Protection has been activated, the micro-controller will clear this condition. Third, the micro-controller will check the internal temperature of battery and set the heating coil accordingly. Fourth, the micro-controller will check the voltage and current of the hot-swaps. Finally, after all the system data has been gathered, the micro-controller will transmit this information to the C+DH before repeating the main sequence of operation. *fig. 11*

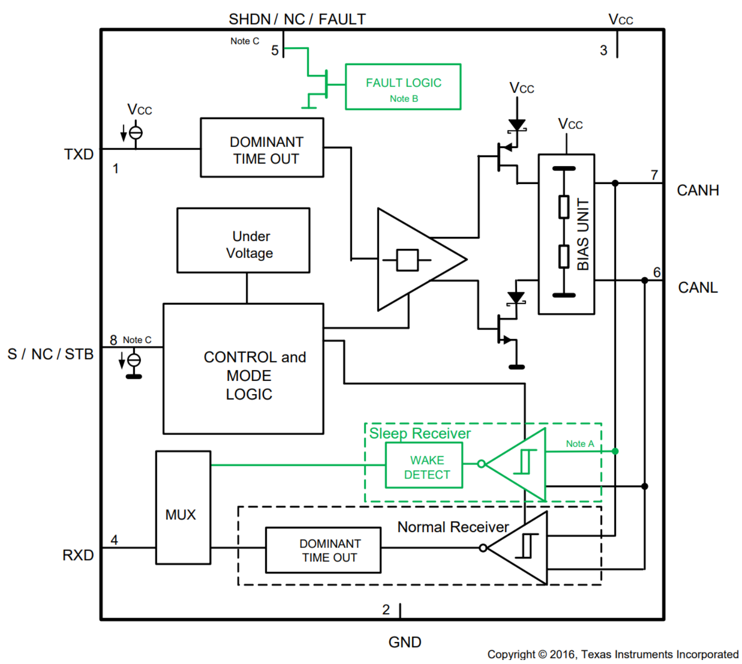

Figure 6: Can Transceiver Block Diagram [10]

Requirements and Verification

I2C Communication with Power Control Module	
Requirements	Verification
1) Our micro-controller must be able to send instructions to the Power Controller over the I2C bus, which will run I2C standard protocols. 2) Our micro-controller must be able to receive data from the Power Controller over the I2C bus.	1) Upon energization, the Power Controller does not engage in normal operations without presets from the micro-controller. As such, proper initialization of the Power Controller, as described by its requirements and verification, will show instructions has been successfully sent by the micro-controller via I2C. 2) The micro-controller will send the telemetry from the Power Controller to the C+DH. This telemetry will be displayed on a monitor. The displayed result will confirm this requirement has been met.

I2C Communication and Control of Battery	
Requirements	Verification
1) The micro-controller must be able to receive data from the battery over an I2C bus. The battery will report its current temperature to the micro-controller. This will allow our system to keep the battery within optimal temperatures. 2) The micro-controller can send a one bit digital signal to the battery to control the heating element within the battery module.	1) LASSI currently does not have additional battery packs to lend us for our project. With this in mind, the Battery Pack will be simulated with a simple I2C temperature sensor to be provided by our sponsor. This will allow us to simulate temperature readings. These readings be read by our micro-controller and sent to the C+DH. The display of the temperature readings on the monitor will confirm this requirement has been met. 2) The single digital bit signal will control a LED to confirm when the heating element signal is active. This signal will turn on/off when the temperature rises/fall above/below a set threshold. The actual temperature constraints of the battery are outside of what we can realistically simulate in lab. As such, we will set the threshold temperature to roughly 10 degrees F above room temperature. This will ensure that the heating element is active. We will then raise the temperature of the sensor above the threshold and will set the signal to low and turn the LED off. We will then let the sensor cool and the LED will turn on again. This will confirm that this requirement has been met.

Voltage Measurement of 3v3 Hot-Swap	
Requirements	Verification
1) Our micro-controller must be able to make voltage measurements at the node of the 3v3 Hot-Swap. We will require an accurate reading to +/- 0.1V. We will not need to make voltage measurements directly off the V_{sys} Hot-Swap as the Power Controller will provide our processor with this information.	1) We will connect an ADC pin on our micro-controller to the 3v3 bus node. The micro-controller will make measurements of this node every second. The telemetry will be returned to the simulated C+DH and be read off of a monitor. This will be confirmed by measuring the node voltage directly with an oscilloscope.

Current Measurement of both Hot-Swaps	
Requirements	Verification
1) Our micro-control must be able to make current measurements at each of the Hot-Swaps. Our Hot-Swaps have a built-in current sensor that outputs a DC voltage signal proportional to the current passing through the Hot-Swap. Our micro-controller will measure this voltage signal with an ADC pin in the same way it will measure the 3v3 Hot-Swap voltage. Our processor can then calculate the current. Our sponsor did not give us quantitative requirements concerning the accuracy of this measurement. We have chosen an accuracy of +/- 5 percent.	1) Our micro-controller will measure this voltage signal and use it to calculate the current passing through the Hot-Swaps and be relayed back to the C+DH and display it on a monitor. We can confirm this by directly measuring the voltage across the simulated load which will be a variable resistor. We can use Ohm's law to calculate the current.

Direct Control of Hot-Swaps	
Requirements	Verification
1) Our micro-controller must be able to activate and deactivate the Hot-Swaps at will; which will allow us to control the current flow through the Hot-Swaps. This will be done with a single bit signal to each of the Hot-Swaps.	1) We will have our simulated C+DH instruct our micro-controller to turn each Hot-Swap on and off. We can confirm this as by measuring the voltage across our simulated loads with an oscilloscope. The voltage across the loads will essentially drop to zero. This is a discrete process.

2.7 CAN Transceiver

The CAN bus protocol requires that we transmit a differential output signal onto the physical bus. This gives the CAN bus noise immunity, which is why our Sponsor requires CAN bus communications with the micro-controller. Our micro-controller is not able to perform this task. A 3.3V CAN transceiver will allow communication between the on board micro-processor and the C+DH. *fig. 10*

There were few requirements given for this component by our sponsor. We simply needed a CAN transceiver that will operate at 3.3V. This particular device can operate within a tolerance of 3.0 to 3.6V, which will be met by the requirements of our Buck Converter. The transceivers maximum data rate is 5 Mbps; which is larger than our micro-processor's 1 Mbps data transmission rate over CAN protocols. The Texas Instruments TCAN330D was chosen due to its low cost[10].

Requirements and Verification

CAN Bus Communication with C+DH	
Requirements	Verification
1) The micro-controller must be able to send telemetry to the C+DH over a CAN Bus through CAN Bus protocols. This telemetry will be sent once per second. 2) The micro-controller must be able to immediately send notifications to the C+DH in case of potential unexpected changes in operation of the power system such as a fault. 3) The micro-controller must be able to receive and execute instructions passed by the C+DH.	1) Since the C+DH has not yet been designed by LASSI, we will simulate the C+DH on a development board. The development board will interface with our personal computer. The simulated C+DH will display the telemetry on a monitor. This will confirm that the first requirement has been met. 2) While verifying the over current protection of the HotSwaps, the micro-processor will alert the C+DH that the HotSwap has opened. The reception of the signal will demonstrate that the signal is sent immediately to C+DH. 3) We will give an instruction to turn the HotSwaps on/off and this will be confirmed through direct measurements (This will be a discrete process). This will demonstrate that the micro-controller is able to execute and receive instructions from the C+DH.

Create Differential Signal on CAN Bus	
Requirements	Verification
1) Create a differential signal so that our micro-processor can communicate with other micro-processors through a CAN bus interface.	1) We will connect the transceiver on our power board to another one-off board. We will be using a micro-processor development board to simulate the C+DH. When communications are established between the two micro-processors, we will have verified that this part is working.

Independent Watchdog Timer	
Requirements	Verification
1) Our micro-controller must have an independent watchdog timer that can restart in the event of an internal error. Our micro-processor has a 12-bit internal watchdog timer on an independent 40 kHz clock. [1] This means if the timer is not reset through software every 0.1024 seconds the micro-controller will restart.	1) In normal operation, our micro-controller will reset the watchdog timer after every major task. However, since we cannot count on an internal error for demonstration, our simulated C+DH will give our micro-controller the command to enter an infinite loop; where the WatchDog timer will not be reset. When the timer finished counting down, it will restart our controller and the C+DH will receive the restart message from the micro-controller. This will verify that the Watchdog timer is working.

3 Tolerance Analysis

3.1 Sensor Tolerance

3.1.1 ADC Sensitivity

In order to provide accurate telemetry to the C+DH, our micro-controller must measure the current and voltage off of the hot-swaps with a high degree of precision. This will be performed with the micro-controller's ADC pins. The the main source of error within our micro-controller is due to gain error within the device.[11] The gain error for our micro-controller is described by the equation below.4 We can see that at worst case the V_{DDA} is 3.6 VDC. This means the error is +/- 0.88mV. This is well within the acceptable error due to the ripple spec of the bus which is +/- 15mV.

$$V_{error} = \frac{V_{DDA}}{4096} \tag{4}$$

3.1.2 Current Sensing

To measure the current flowing through our hot-swaps our micro-controller will measure the I_{mon} voltage signal.9 This measurement's precision is largely based off of the R_{Imon} resistor value at each of the hot-swaps. The resistor value is selected from the equation below.5 We found the 3v3 R_{Imon} must be 127 kΩ and Vsys R_{Imon} must be 84.5 kΩ. We can see that the error in the current measurement will be proportional to the error within the the resistor. With this in mind we will ensure these resistors are within +/- 1% tolerance to ensure a reading that is within the required +/- 2.5% precision.

$$R_{Imon} = \frac{63k\Omega * V_{ADCmax}}{I_{LoadMax}} \tag{5}$$

3.2 Regulated Bus Tolerance

With respect to the step-down dc regulator a tolerance of 5% was assumed for passive components. The voltage ripple is dependant on the current ripple (inductor size) and the capacitor sizing. Assuming worst case inductor performance $2.09\mu H$ vice nominal $2.2\mu H$ I_{ripple} will increase by .1145A per eqn 6.

$$V = L\frac{di}{dt} \rightarrow \Delta I = \frac{VDT}{L} \tag{6}$$

$$C = \frac{\Delta Q_c}{\Delta V} \rightarrow C = \frac{\frac{1}{2}\frac{T}{2}\frac{\Delta I}{2}}{\Delta V} \rightarrow V_{ripple} \propto \frac{\Delta I}{C} \tag{7}$$

Plugging this into eqn 7 with a worst case 2.29 capacitance yields a V_{ripple} of 2.987mV. As a conservative estimation this value is added to the maximum computer simulated ripple of 7.543mV, yielding an error of +/- 10.53mV. This is well below our requirement of 5% ripple.

4 Cost Analysis

4.1 Cost of Parts

Table 3: Estimated Cost

Description	Part number	qty	Cost	Available
Power management eval board	BQ25703EVM	1	149.99	TI.com
Power management controller	BQ25703	1	5.28	digikey.com
Hot-Swap controller	TPS2420	2	5.88	digikey.com
Integrated Buck Converter	TPS53515	1	6.49	digikey.com
CoilCraft 2.2 uH Inductor	XAL7070-222MEB	1	3.14	mouser.com
Wurth Electronics	74437356022	1	2.08	mouser.com
CAN-Transceiver	TCAN330DR	1	2.37	digikey.com
Micro-Controller	STM32F072RB	1	3.84	mouser.com
Passives	numerous	1	10	digikey.com
Micro-controller dev board	NUCLEO-F072RB	2	20.66	mouser.com
Total			**209.73**	

4.2 Cost of Labor

The average hourly salary of an ECE graduate from the University of Illinois is \$34.20 an hour. We have three people in our group and expect to work an estimated 15 hours a week per person. Given the 13 weeks of design implementation in this course, we would expect labor to cost \$16,929. This number was multiplied by a factor of 2.5 to account for unforseen overhead costs. This brings the total cost to approximately \$42,322 See the equations below.

$$\frac{\$71,166}{1yr} * \frac{1yr}{2080hr} = \$34.20/hr$$

$$\$34.20/hr * 3 * 15hr * 13 * 2.5 = \$42,322$$

5 Schedule

Week	Andrew	Chris	Dan
2/18/19	Write Design Document	Write Design Document	Write Design Document
2/25/19	Master Module Schematic and Board Layout	Program the micro-controller to establish CAN bus communications	Program the micro-controller to establish I2C communications
3/4/19	Develop Power Control Board Layout	Finish micro-controller to establish CAN bus protocols, finalize CAN-grammar	Establish I2C communications with the Power Controller on development boards
3/11/19	Finalize Power Control Board Layout	Write code to simulate the battery pack on I2C and simulate C+DH on CAN bus	Write code for micro-controller. Focus on analog and 1 bit control signals
3/18/19	Spring Break	Spring Break	Spring Break
3/25/19	Soldering Power Controller Components onto the PCB	Soldering Power Controller Components onto the PCB	Soldering micro-controller onto to PCB
4/1/19	Soldering Power Controller Components onto the PCB, test operation	Soldering Power Controller Components onto the PCB, test operation.	Soldering micro-controller onto to PCB, test operation.
4/8/19	Testing Power Components, Troubleshooting	Testing micro-controller operation, troubleshooting, refine simulated systems.	Testing micro-controller operation, troubleshooting, refine simulated systems.
4/15/19	Demonstration Refinement	Demonstration Refinement	Demonstration Refinement
4/22/19	Write Report	Write Report	Write Report
4/29/19	Write Report	Write Report	Write Report

6 Safety and Ethics

Prior to any testing performed in the accomplishment of this design, specific safety briefings will be held regarding the testing procedures and hazards present. Additionally, all operating limits of the equipment have been verified and will be observed during testing.

When testing the protective features of the System Power Monitor and Controller, we will be moving set points to within the normal operating range of the circuit and verifying proper response. This will be done in order to prevent subjecting components to possibly destructive levels of energy while verifying proper operation of the protective circuitry.

The Illini-Sat 2 battery module has an array of protective features required to utilize Li-Ion cells. Unfortunately, our sponsor is unable to provided us with a battery module and will not have any available for our use this semester. In accordance with principle 1.2 the ACM Codes of Ethical and Professional Conduct, "Avoid Harm" we will not be using unprotected cells[12]. As such we will be simulating the battery module with an electronic load to verify its functionality.

In addition to ensuring our safety and the safety of others, we are seeking to build a reliable Power Board for our sponsor. According to ethical principle 2.9, we must "Design and implement systems that are robustly and usably secure." This essentially is the purpose of our project; to design a power board which is more reliable and to ensure a better success rate with this new generation of satellites.

7 References and Acknowledgements

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8 Appendix

8.1 Schematic Diagrams

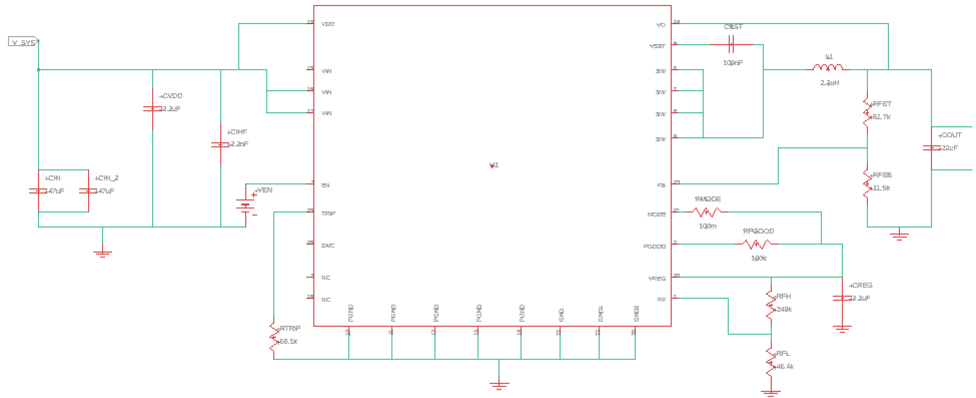

Figure 7: Eagle Schematic for 3.3 V DC step down regulator. ** note the output capacitance is 242uF implemented with 11 22μF capacitors vice the one shown in the diagram

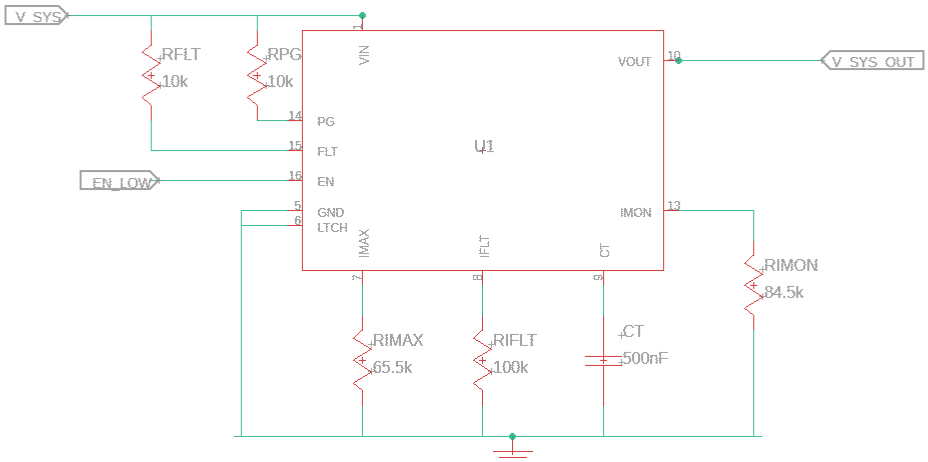

Figure 8: Eagle Schematic for VSys Hotswap controller.

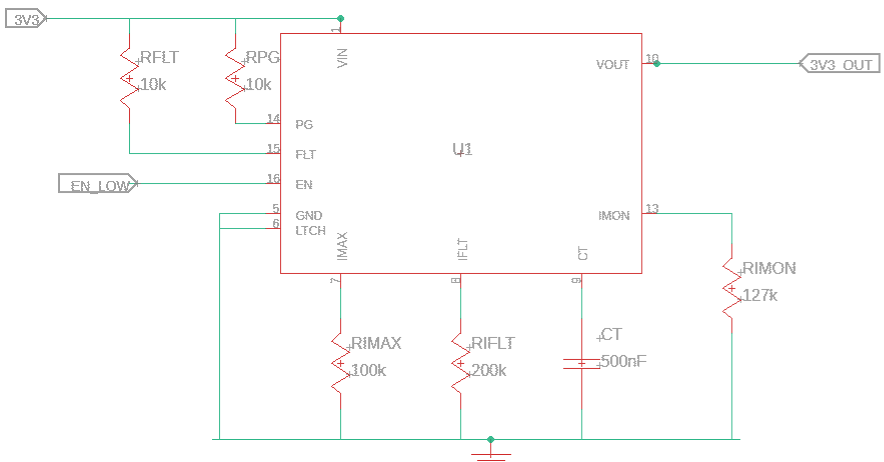

Figure 9: Eagle Schematic for 3v3 Hotswap controller.

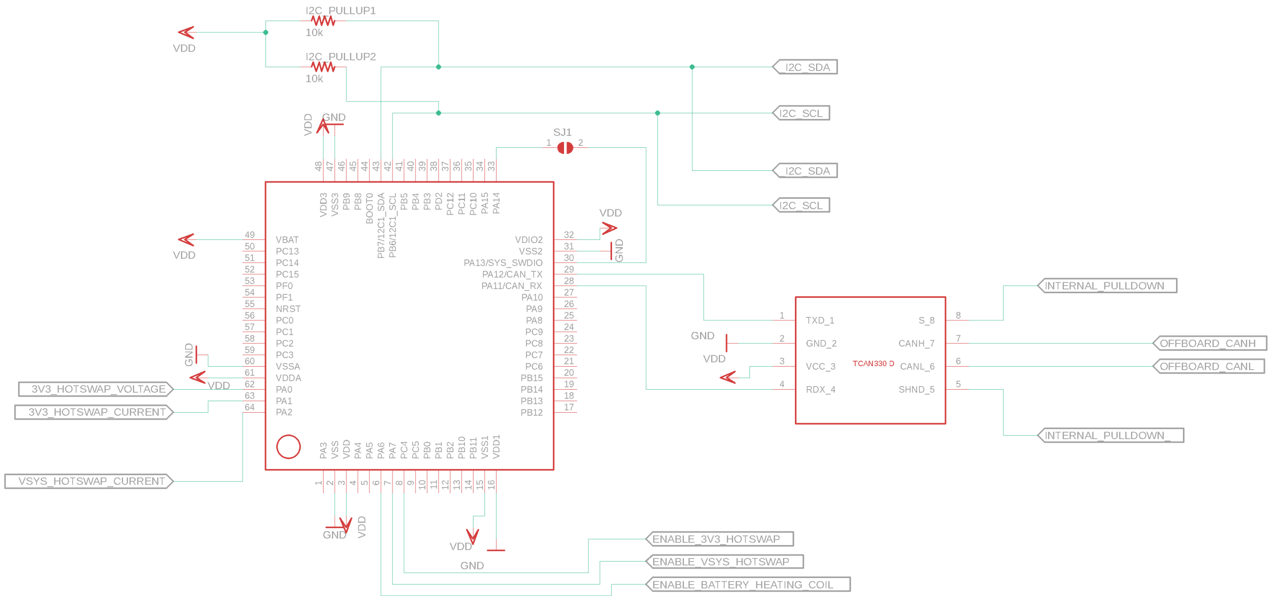

Figure 10: Eagle Schematic for Controller Circuit.

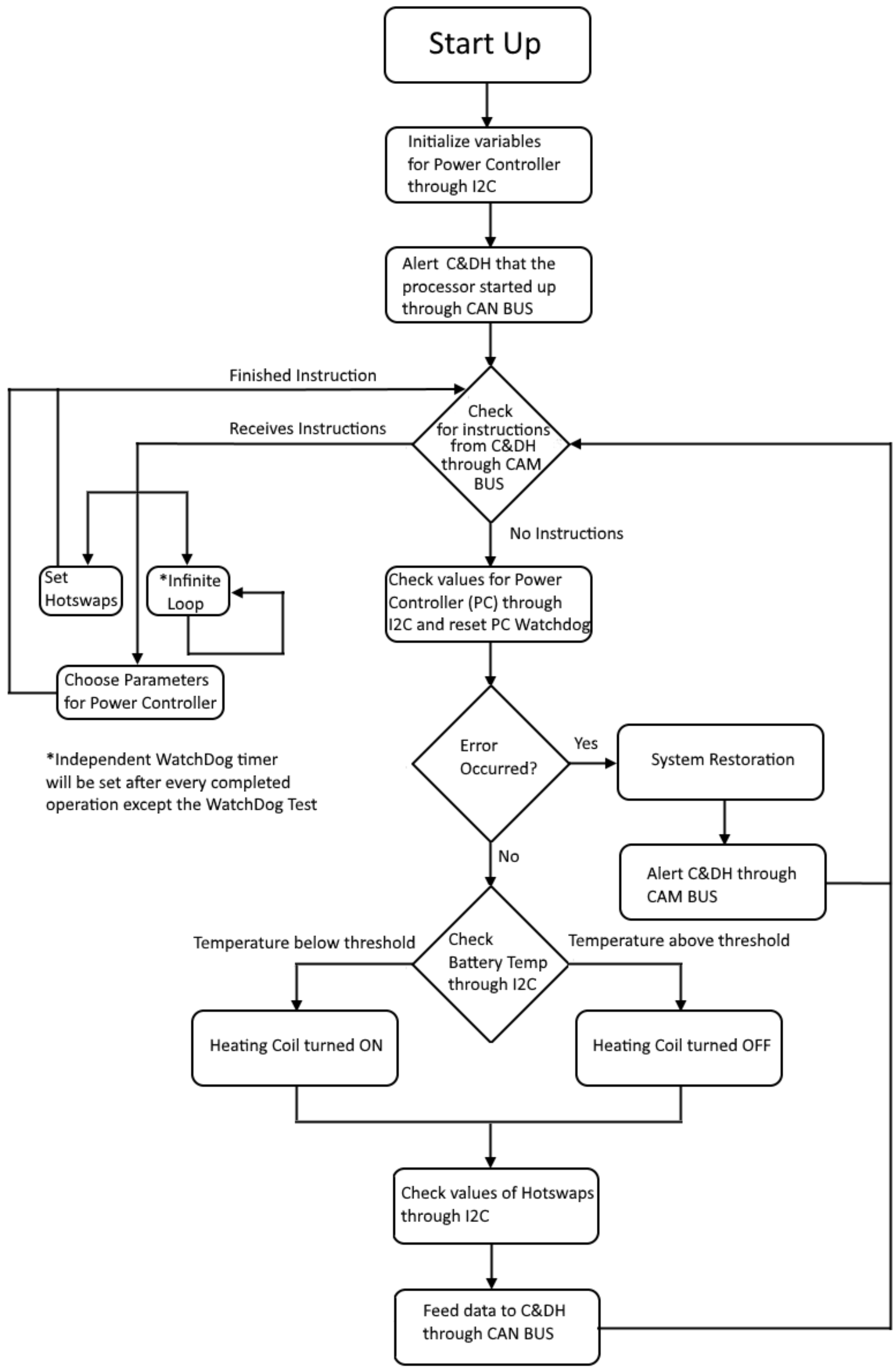

Figure 11: Software Block Diagram.