Master Bus Processor

Team 14 - ECE 445 - Spring 2019

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Design Document - TA: Zhen Qin

1. Introduction

1.1. Objective

A common issue facing aspiring musicians is the very high cost barrier to entry. Integrated and digital circuits have contributed to the increased popularity of home studios, however these digital processors force the user to miss out on the more traditional acoustic properties of formal analog processing equipment, which historically have been very costly and essentially made to order by manufacturers. This is not ideal for most musicians as they prefer to use analog processing over digital processing due to differences in how the sound is perceived by a listener. Currently, there is no affordable option designed for the home user, and certainly nothing that combines the performance of analog processing with the ease of digital control.

The objective of our Master Bus Processor is to create a solution tailored for a home user by offering an affordable product that is simple to use and understand. By combining analog audio processing with digital control, we can create a very flexible design which will keep costs down and maintain high-quality audio performance.

1.2. Background

The current offerings for Master Bus Processors are fairly limited, especially for a home studio user. There are two fundamental varieties, digital and analog. Our device will offer is a hybrid of the two. All audio processing circuits are strictly analog, however all controls are digital. The analog circuitry is so important because many musicians and audiophiles claim that analog audio sounds “much deeper and fuller”, and as a result is much more desirable [1]. Our Master Bus Processor will make use of digital control in order to provide ease of use to the user. Many of the products on the market have many different knobs and controls that are confusing and cumbersome to use during a live mix. By offering an Liquid Crystal screen as well as minimal knobs and buttons to control the device, we can make it much easier to use for a more casual user.

Specifically, what makes our product unique from others that are currently available is the use of digital controls on an analog circuit and the ability to rearrange the order of processing blocks. We also focused on simplifying circuits by use of SMD/SMT components, and lack of discrete channel control. When comparing to the Rupert Neve Portico II Master Buss Processor (MBP), there are many fundamental differences [2]. The Portico II MBP is entirely analog and consequently does not allow the user to change the order of processing blocks. Our design uses digital control to allow the user to select any order of compression, equalization, and saturation through a very simple button and screen interface. The Portico II MBP also has more complex audio processing blocks, allowing for features like discrete control of each channel on the bus. This leads to a cost of $4,000 which is cost prohibitive for most home studio users.

1.3. High-level requirements

A successful project will have balance between two main features, performance and accessibility. There will also be a focus on affordability with a projected price point under $2500.

1. *Performance:* Must be able to provide the non-linear audio response of analog processing. There should be proper implementation of:
    a. Compression with at least 20 dB gain reduction and 100 ms response.
    b. Equalization with at least 2 EQ bands centered at 70-90 Hz and 9-11 kHz
    c. Saturation with the ability to provide 0-10% total harmonic distortion to the mix.
2. *Accessibility:* Device controls should be intuitive and simple enough for an amature user. Controls should be limited to at most 2 knobs per analog block, 5 total buttons, and an LCD display with at most 4 menu screens.

2. Design

2.1. Block Diagram

Our solution consists of both digital and analog circuits to allow for the flexibility of digital control with the audio quality of analog processing. We will be using a microcontroller to control relays in the analog circuit that can change the orientation and exposure of different analog component blocks. This will allow the user to use a series of buttons and an LCD display to control circuit parameters such as the order of each analog block and the particular mode that each block performs its desired function. All audio processing will be performed using analog circuits and the user will be able to use knobs to adjust specific analog block parameters. An overview can be found in Figure 1.

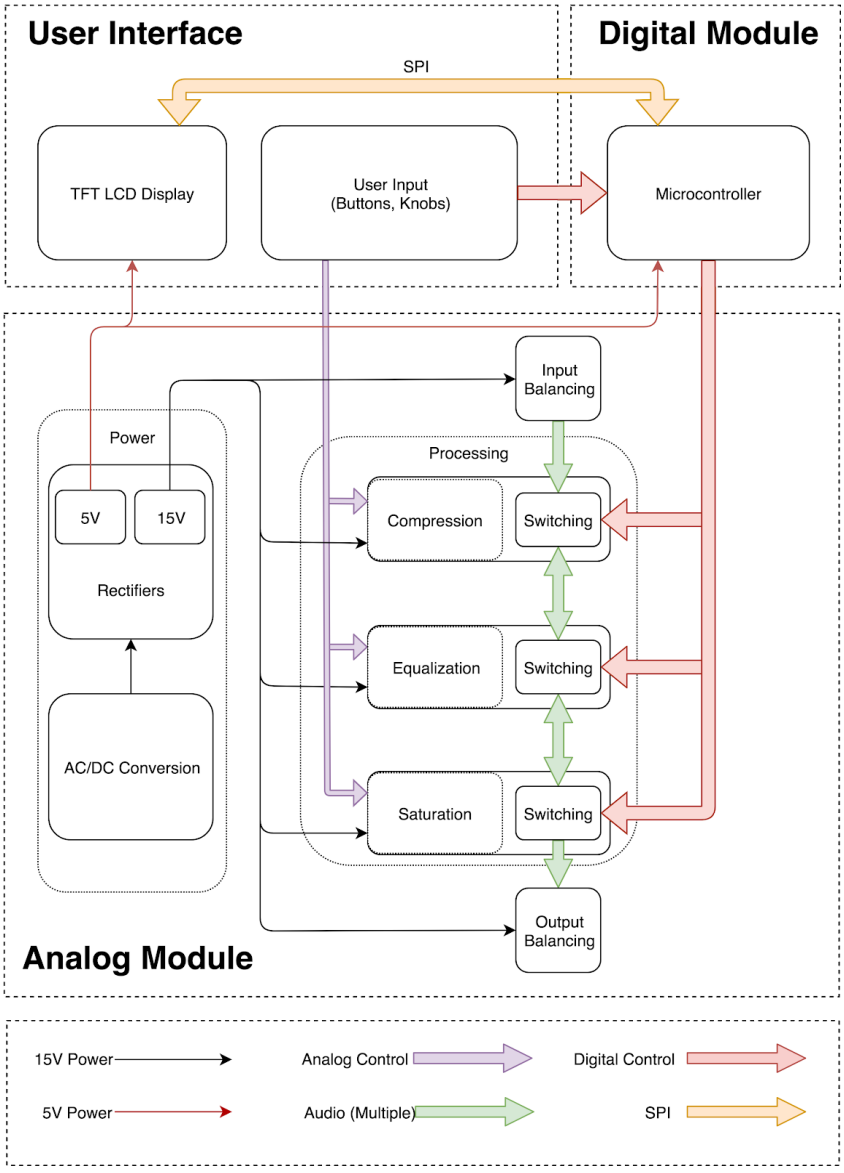

Figure 1. Master Bus Block Diagram

2.2. Physical Design

The Master Bus Processor (MBP) will be designed to fit inside an industry-standard 19” rackmount enclosure as found in Figure 2. The front control panel will occupy two rack-units (2U). As a reach goal we will design a custom 19” rackmount enclosure for the MBP.

Figure 2. Standard 2U Rackmount Enclosure - Amazon.com [3]

The User Interface--consisting of the LCD screen, selection buttons, and processor control knobs, will be mounted on the front panel of the enclosure. Inside the enclosure, the system will be divided into two separate printed-circuit-boards (PCBs) in order to reduce noise from interference. The power systems, analog processing blocks, I/O connections, and control knobs will be mounted on a large, base PCB. The digital controller will be housed on a separated PCB which will be mounted above the analog PCB. The two PCBs will exchange power and control signals through a central ribbon cable connection(pinout labeled in Figure 9). An overhead view is included in Figure 3.

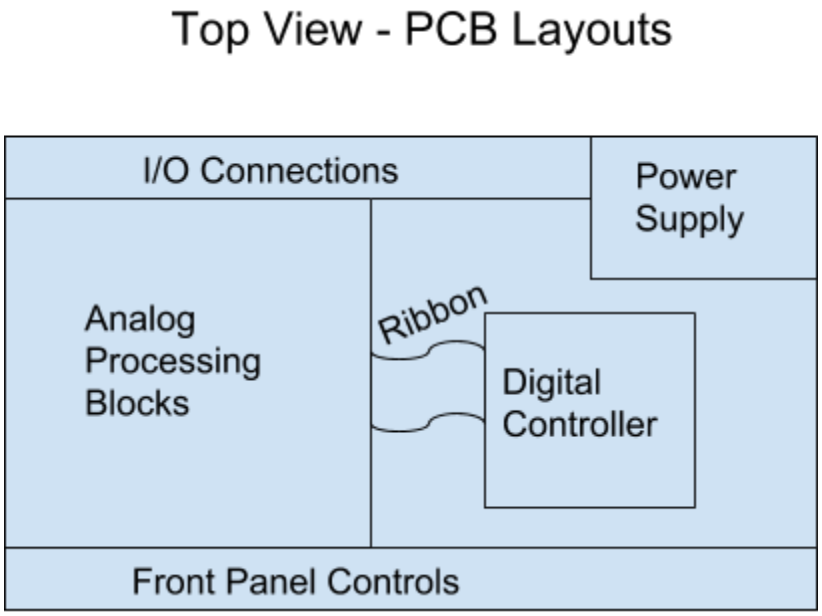

Figure 3. PCB Layouts

2.3. Block Design

In multiple blocks we have included reach goals. These are additional features that we will implement if and when our main design requirements are completed.

2.3.1. Analog

The schematic for the entire analog circuit can be found in Figures 6, and 23.

1. AC/DC Conversion and Regulators

The External "Line-Lump" Transformer will convert US AC wall mains power (120 V 60 Hz) to levels which are tolerable by the Voltage Regulators down-line. The AC input voltage provided by the External Transformer will be converted to DC by diode Rectifiers and smoothing capacitors in preparation to be received by non-switching Voltage Regulators down-line. Schematics for this block can be found in Figures 7, 24, and 25.

Requirement	Verification
Must convert 120 V AC to 20-24 V DC	Input 120 V AC and measure open-circuit voltage confirming below 24 V DC.

The Voltage Regulators will accept the smoothed positive and negative DC buses from the Rectifiers and output stable voltage buses to power the analog and digital systems.

Requirement	Verification
Must provide 4.9 - 5.1 V for the digital control system and safely provide 500 mA to 2 A current	- Measure open-circuit voltage and ensure that it is below 5.1 V. - Connect a resistive load until voltage reaches 4.9 V and ensure that at least 500 mA current available using an ammeter.
Must provide 14.0 - 15.8 V for the analog control system and safely provide 500 mA to 2 A current	- Measure open-circuit voltage and ensure that it is below 15.8 V. - Connect a resistive load until voltage reaches 14.0 V and ensure that at least 500 mA using an ammeter.

2. *Compression*

The Compressor is an automatic-gain-controller that is specialized for use with audio signals. When the audio signal at the input of the compressor exceeds a fixed threshold level, the Compressor will reduce its gain by a proportional amount until the signal has fallen below the threshold again. The output of the Compressor is then normalized so that the average amplitude of the audio signal has been increased. By this process, the Compressor is able to improve the perceived loudness of the audio signal. In order to reduce distortion and act as linearly as possible, the Compressor operates on a timescale that spans at least multiple low-frequency wave cycles. The Compressor can be connected in various places in the analog signal chain, where it will interact differently with the other analog processing blocks. As a reach goal, the Compressor will be able to switch into a "Limit" mode and act as a peak-limiter. The Compressor circuit is based on the THAT Corp 4305 Analog Engine standard application circuit [4] with adjustments to accommodate 2-channel operation. Schematics for this block can be found in Figures 13, 14, and 27.

Requirement	Verification
Must be able to provide at least 20 dB gain reduction without overloading its input	Input a 1 kHz sine wave. Record the input and output waveforms and verify at least 20 dB gain reduction at maximum setting in MATLAB. Verify stability of output using oscilloscope.
Must be able to engage full gain reduction within at least 100 ms	Input a 1 kHz sine wave. Record the input and output and verify response time in MATLAB.
Must be able fully disengage gain reduction in 1 s	Input a 1 kHz sine wave. Record the input and output and verify response time in MATLAB.

3. *Equalization*

The Equalizer will be series of high- and low-frequency focused filters that can be applied to the audio signal. The filters in the Equalizer block will allow the user to boost or cut certain bands of the audio spectrum in order to shape the overall tonal response of the Equalizer block. The Equalizer will utilize an operational amplifier (op-amp) gain stage with filters connected to the inverting and non-inverting inputs in order to achieve active equalization. The Equalizer can be connected in various places in the analog signal chain, where it will interact differently with the other analog processing blocks. As a reach goal, the Equalizer will be able to switch between "Shelving" and "Bell" modes so that the user can select different filter types in addition to controlling the frequency response. The Equalizer circuit is similar to a standard "graphic equalizer" layout, as described by Rod Elliott [5]. Each band of the Equalizer contains a resonant RLC circuit which allows the frequency bands to be boosted or attenuated by connecting the resonant circuits to the feedback network of an op-amp. Since it is impractical to include large, expensive inductors in this design, the resonant circuits contain sub-circuits called 'gyrators' which create simulated inductance values. Circuit level analysis of the simulated inductance from gyrators is described by Berndt D. F. Berndt and S. C. Dutta Roy [6]. Schematics for this block can be found in Figures 15, 16, and 28.

Requirement	Verification
One available band must be in the region of 70-90 Hz	Sweep input signal frequency from 20 Hz - 20 kHz, measure relative gain at 80 Hz
One available band must be in the region of 9-11 kHz	Sweep input signal frequency from 20 Hz - 20 kHz, measure relative gain at 10.3 kHz
must not introduce significant additional distortion below the voltage "headroom" clipping level (+/-14 V)	Input a 1 kHz sine wave. Set to maximum setting and record the input and output. Verify total harmonic distortion is within range using MATLAB, set to minimum setting and verify also within range

4. Saturation

The Saturator block will allow the user to enhance the harmonic content of the audio signal by mixing in small amounts of harmonic distortion. The Saturator will use an op-amp gain stage with diode-incorporated feedback network in order to provide non-linear gain. The output from this gain stage will then be added back to the original audio signal in small amounts by the user through a "blend" control circuit and summing amplifier stage. The Saturator can be connected in various places in the analog signal chain, where it will interact differently with the other analog processing blocks. As a reach goal, the Saturator will be able to switch between "Asymmetric" and "Symmetric" modes so that the user can choose between the different harmonic orders emphasized by each mode. The Saturator circuit is based on a standard soft-clipping "fuzz" circuit, as described by Rikupetteri Salminen [7]. The Saturator incorporates a diodes into the feedback network of an op-amp in order to produce highly non-linear gain. The output from this stage is then summed back with the original, unaffected signal at a very low level in order to give a subtle effect. Schematics for this block can be found in Figures 17, 18, and 29.

Requirement	Verification
Must be able to contribute 0-10% total harmonic distortion to the audio signal	Input a 1 kHz sine wave. Set to maximum setting and measure the input and output. Verify total harmonic distortion is within range using MATLAB, set to minimum setting and verify also within range

5. *Input/Output Balancing*

The I/O section will consist of the hardware connectors and electronic signal balancing circuits which allow the Master Bus Processor to be connected to other professional audio equipment. The I/O connections will use differential amplifiers receive and drive signals to and from other equipment and a user-selectable hardware bypass will be incorporated to directly connect the inputs and outputs of the MBP when necessary. The Inputs and Outputs utilize the THAT Corp 1200 and 1646 Line Receiver/Drivers and the recommended implementation circuits [8] [9], respectively. Schematics for this block can be found in Figures 11, 12, 19, 20, and 26.

Requirement	Verification
Must use ¼" TRS or three-pin XLR connectors	Confirm that connectors correspond to desired standards
must not overload at less than +/-14 V swing	Input a 1KHz sine wave with magnitude +14 V. Measure the input and output an oscilloscope and confirm stability using matlab

6. *Switch Control*

The switch control as seen in Figure 12, will take Boolean inputs from the microcontroller to orient and expose the different analog blocks. It will consist of a series of power transistors and double contact relays. This will allow the microcontroller to change the layout of the analog circuits based on what is inputted by the user. A fail-safe route will be provided in the case of a digital circuit failure (Figure 8). A test circuit like that of Figure 4 will be constructed to verify proper operation before the circuit is constructed on the PCB.

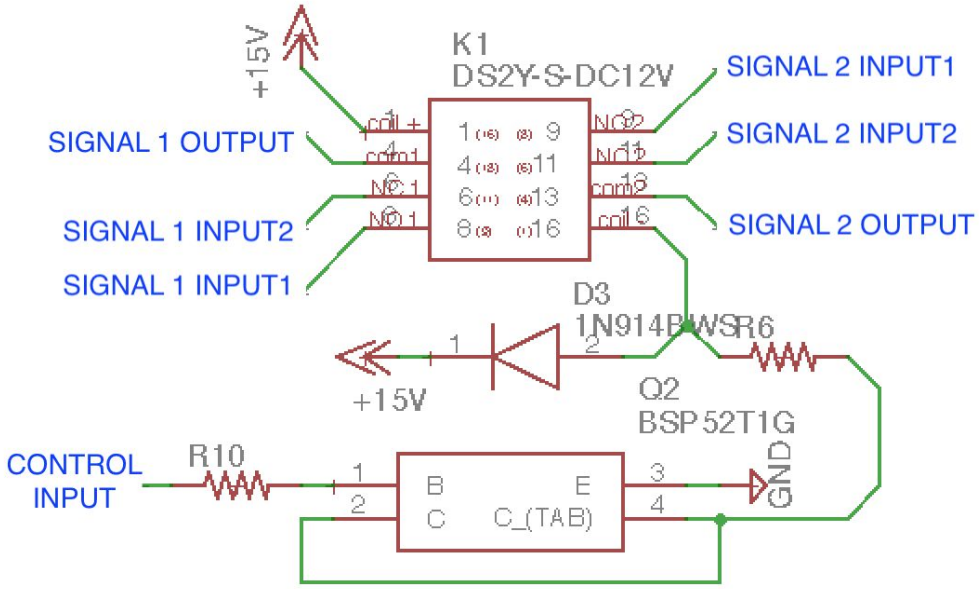

Figure 4. Switch Control Test Circuit

Requirement	Verification
Must have less than 0.01% distortion	The test circuit from Figure 4 will be built. Biased in the on position, input and output signals will be compared in MATLAB
Must not allow discharges onto the audio path when switching	The test circuit from Figure 4 will be built and connected to oscilloscope. Biased in the off position, output signals will tested for leakage
Must input less than 40 mA per control line, 200 mA total, from I/O pins on microcontroller	The test circuit from Figure 4 will be built and input control current will be measured at both logic high and low

2.3.2. Digital

The schematic for the entire digital circuit can be found in Figures 5, 21, and 22.

1. Microcontroller

The microcontroller will send Boolean output signals to the switch control to alter the layout of the analog signal blocks. It will also take input from the user using a series of hardware buttons on the front of the 2U case that allow the user to intuitively interface with the microcontroller. Feedback of these inputs will be displayed on the LCD display. As a reach goal, the microcontroller will perform elementary DSP functions to give some feedback of analog block performance as well as store contents of an onscreen manual for the user. A flowchart for the microcontroller is included in Figure 30.

Requirement	Verification
Must have at least 20 output pins for connection to switch control	Verify that pin-layout includes at least 20 output pins on chip schematic
Must have at least five input pins for connection from buttons	Verify that pin-layout includes at least five input pins on chip schematic
Must support SPI and have required pins for this standard	Verify that SPI is a supported protocol in peripheral features table
Must have non-volatile memory for program data (>10 kB)	Verify that non-volatile memory is included in product features table and that it includes more than 10kB
Must have at least 5 analog input pins for reading voltage ranges	Verify that pin-layout includes at least five analog input pins on chip schematic

2.3.3. User Interface

1. LCD Display

A display will allow the user to see the current settings of the digital controls including the order of the analog blocks, and their current mode. The display will communicate with the microcontroller using a SPI connection.

Requirement	Verification
Must fit in a 1U space (1.75” tall)	Measure height of display using ruler

2. User Interface

A series of buttons will allow the user to interface with the microcontroller. There will be buttons labeled: Sequence, Compression, Equalization, Saturation, and Enter. These buttons will allow the user to interact with the microcontroller to set circuit parameters.

Requirement	Verification
Must travel at least 2 mm to allow for easy feedback to user	Press button and measure travel using a ruler

A series of knobs(potentiometers) will be separated based on their corresponding analog processor block. They will allow the user to make circuit alterations in real time (Figure 10).

Requirement	Verification
Must maintain desired position	Turn knob and release. Measure voltage differential on leads using a voltmeter for consistency

2.3.4. Supporting Materials

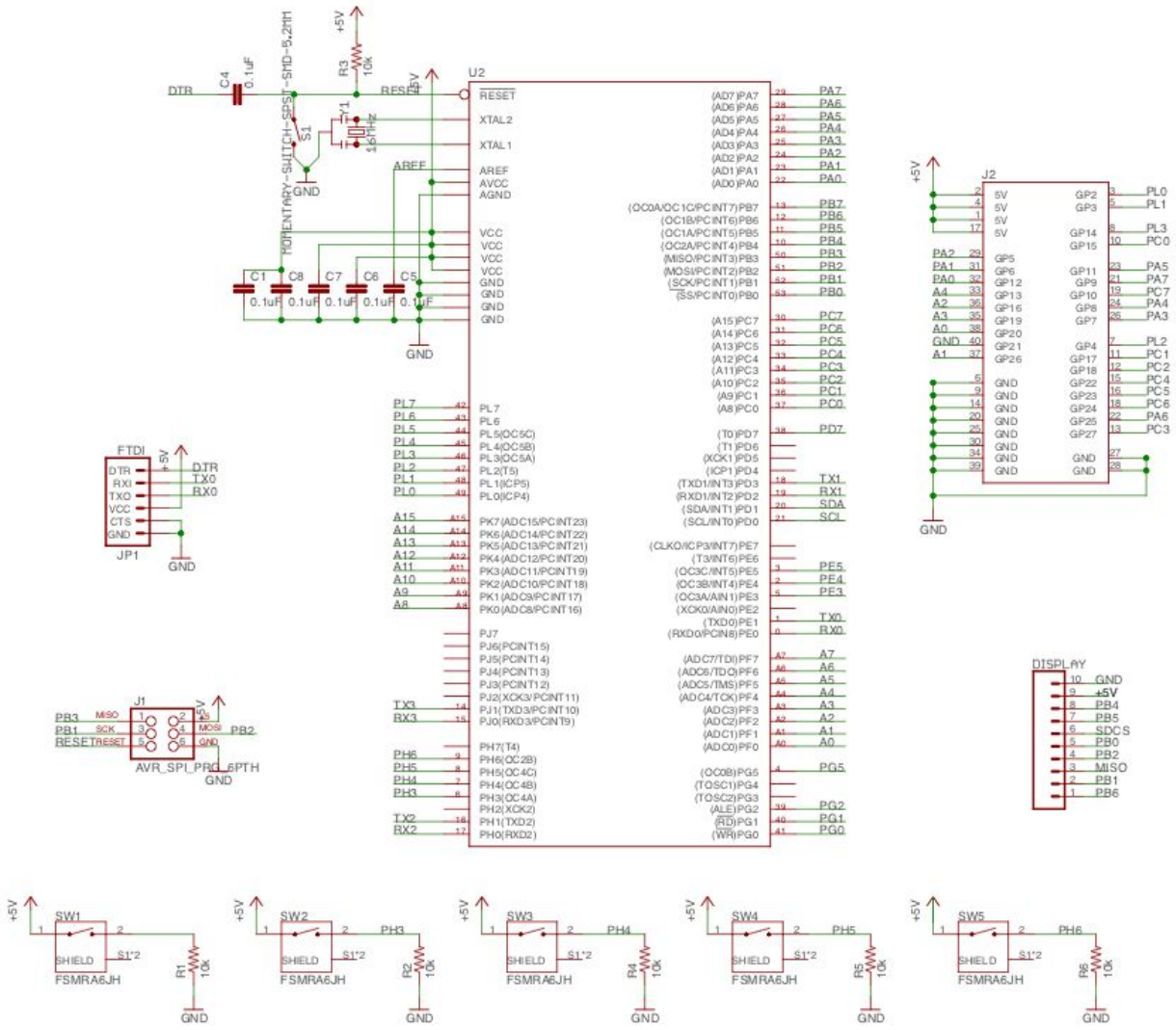

Figure 5. Digital Control Board Schematic

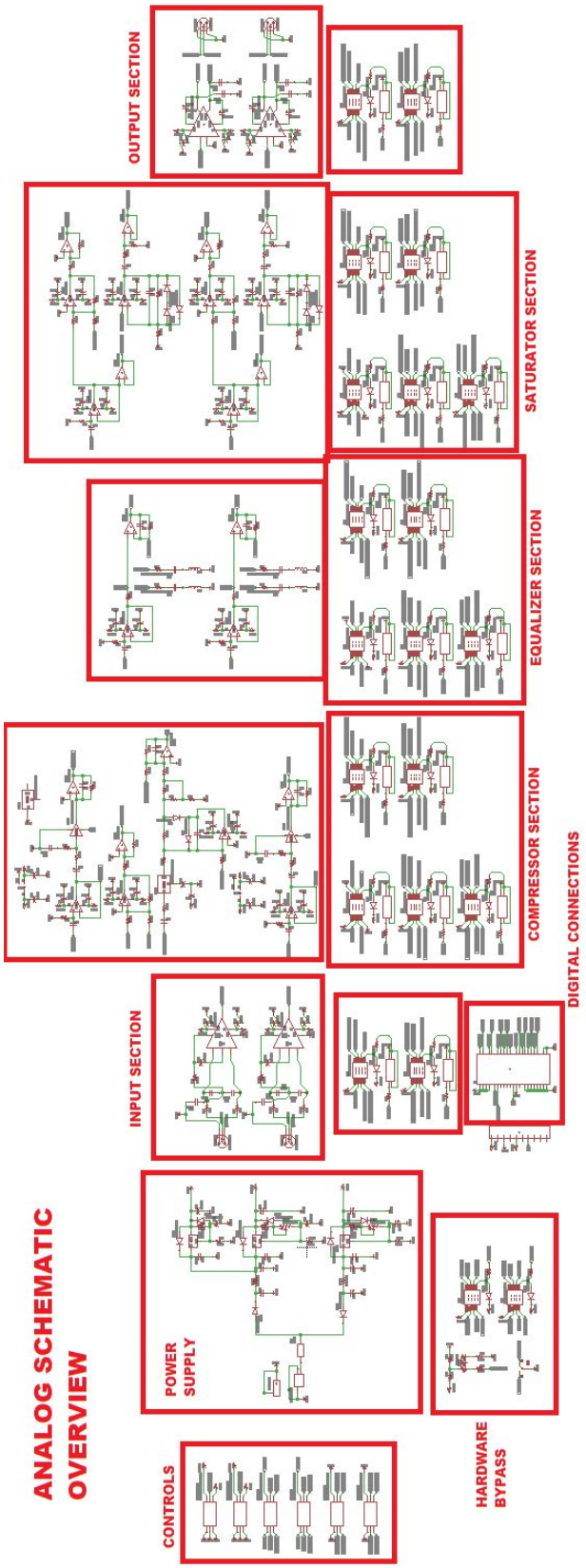

Figure 6. Analog Processing Schematic Overview

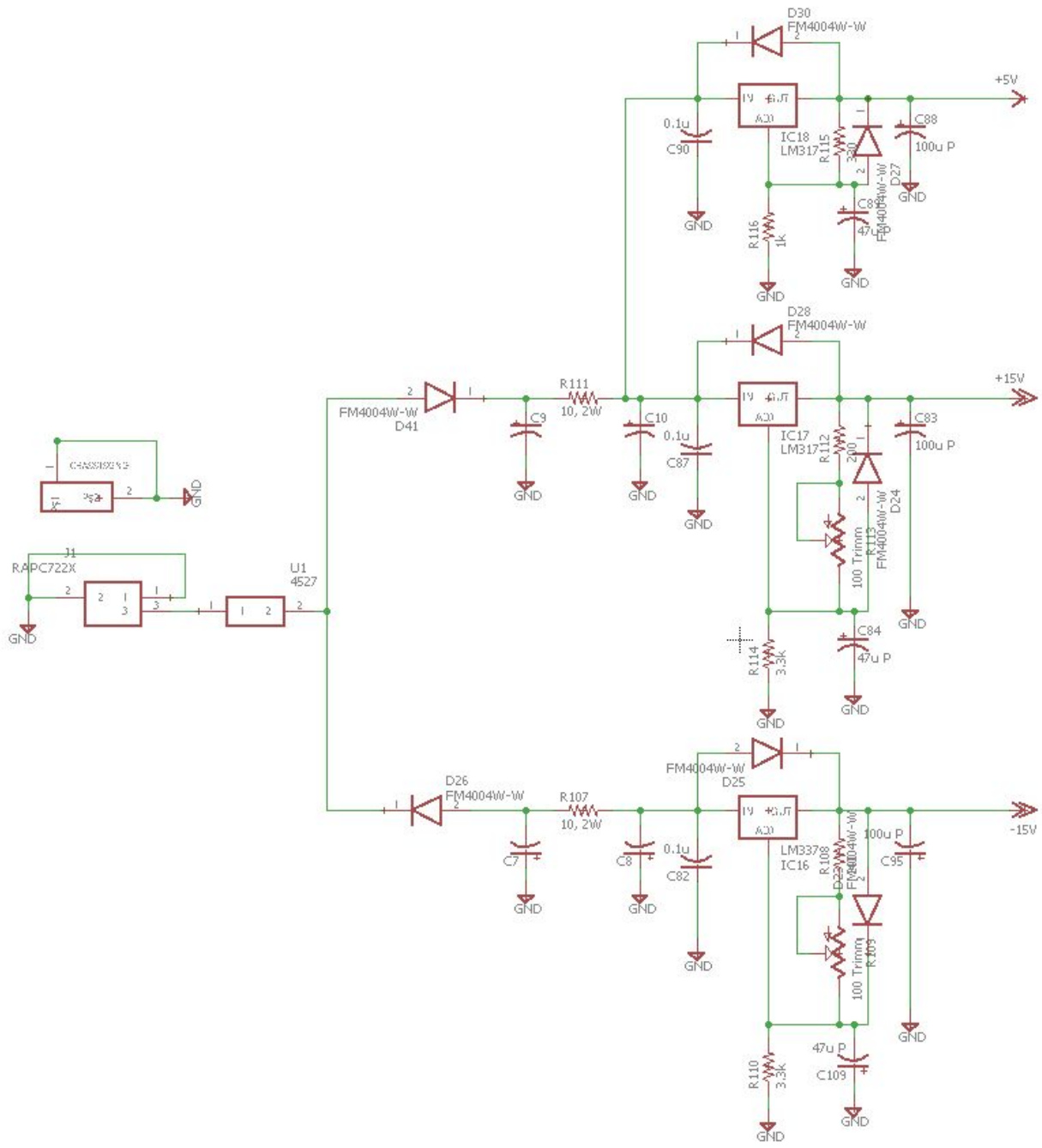

Figure 7. Analog Power Supply Schematic

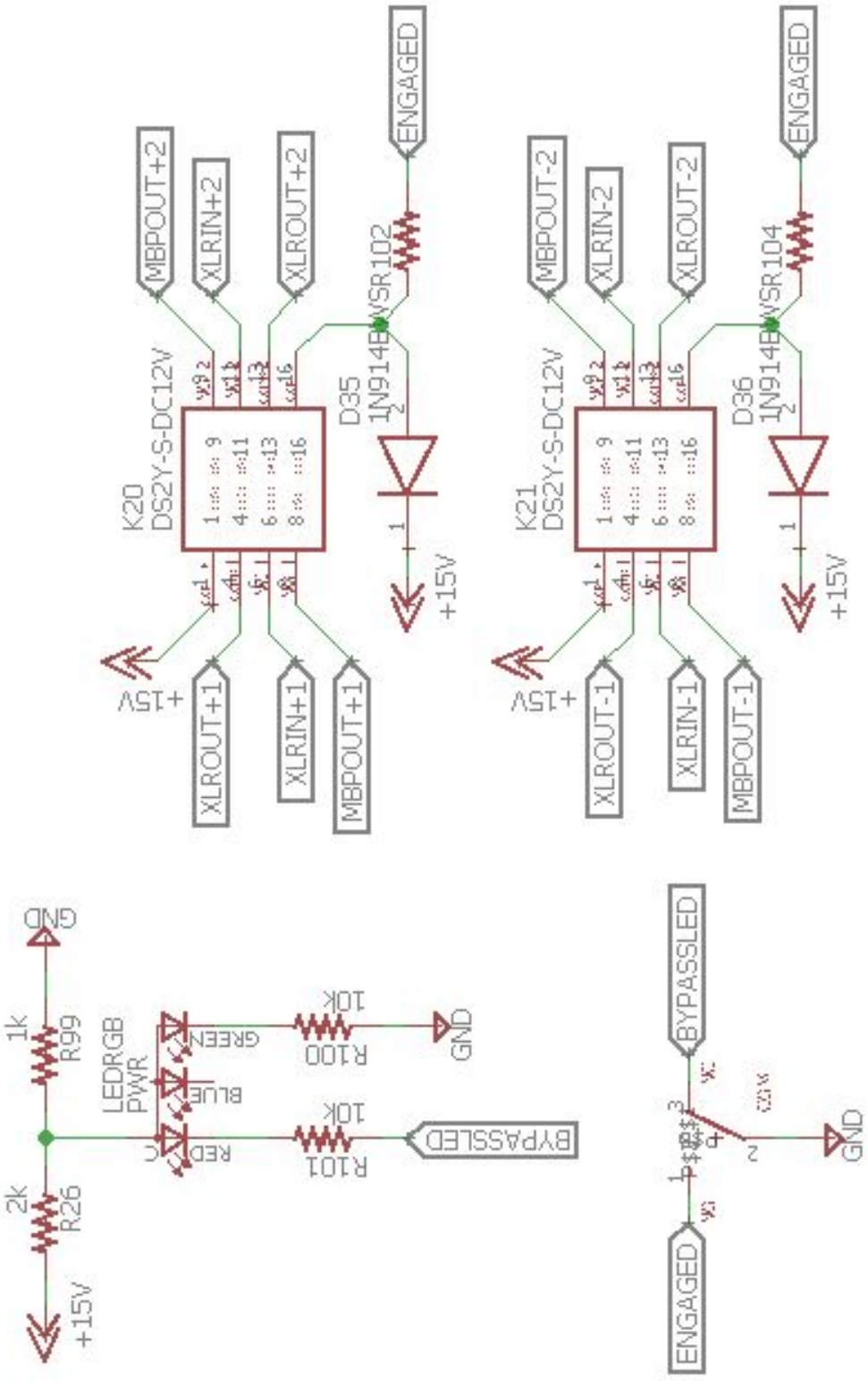

Figure 8. Analog Hardware-Bypass Schematic

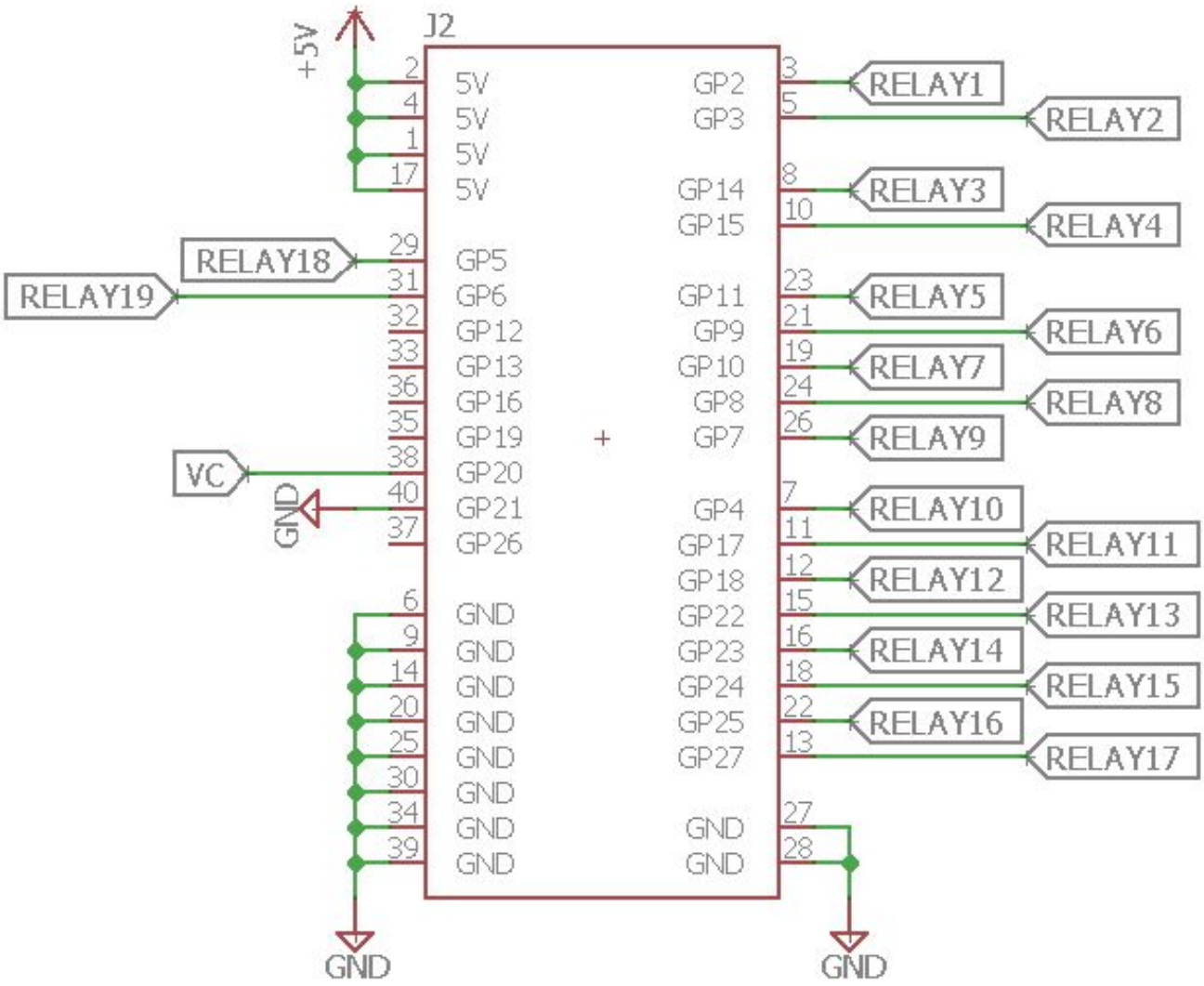

Figure 9. Analog Digital-Connector Schematic

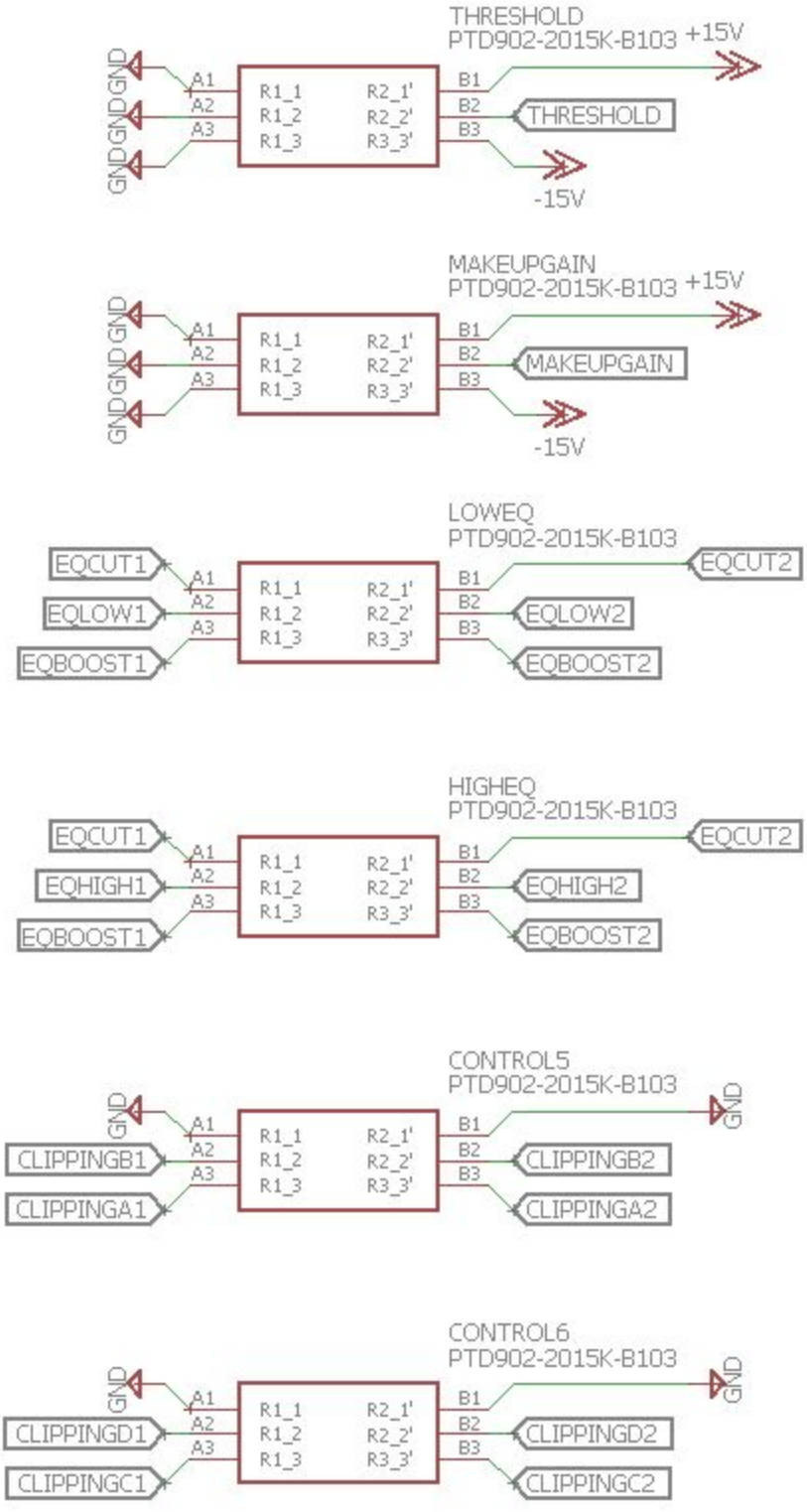

Figure 10. Analog Controls Schematic

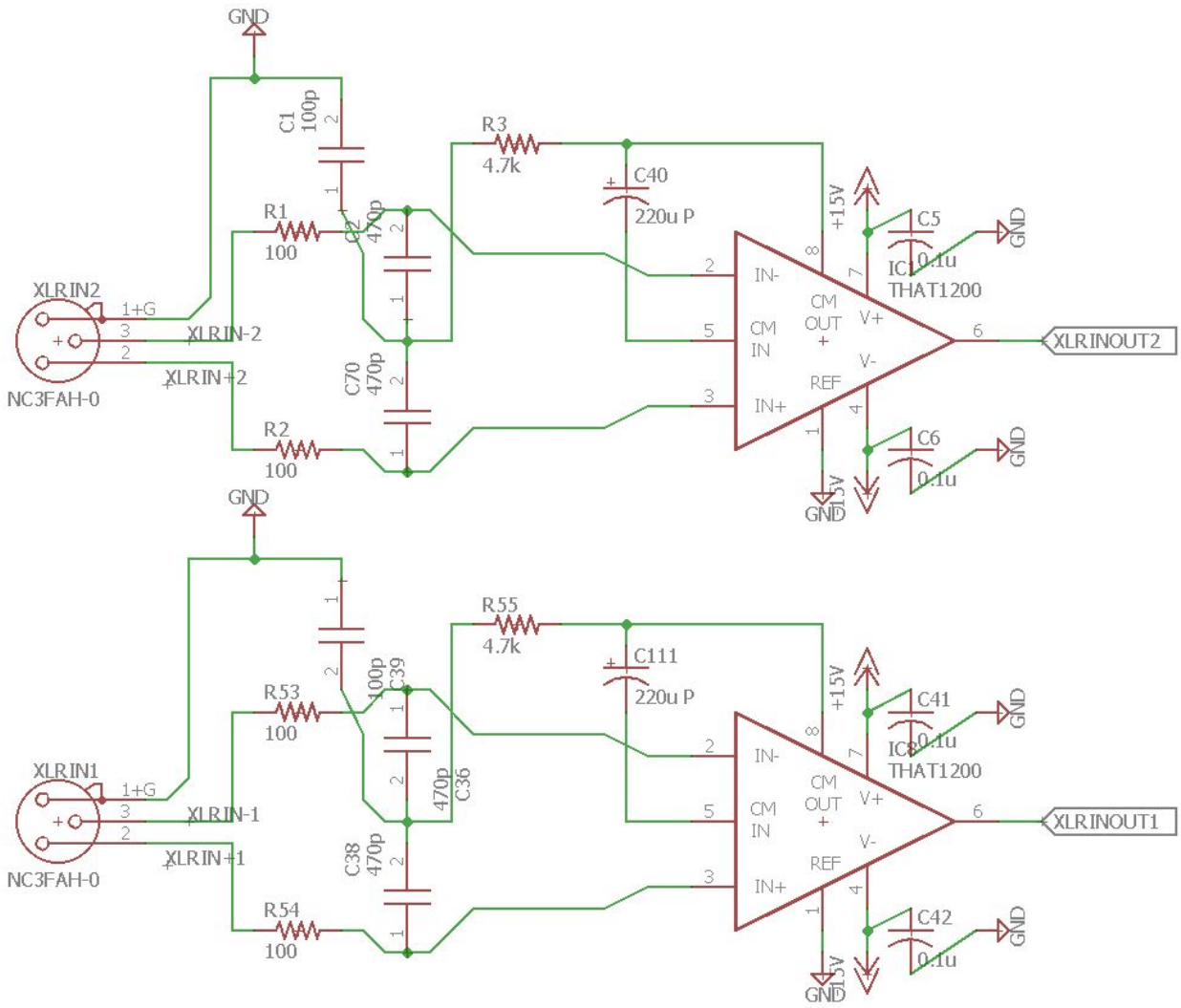

Figure 11. Analog Inputs Schematic

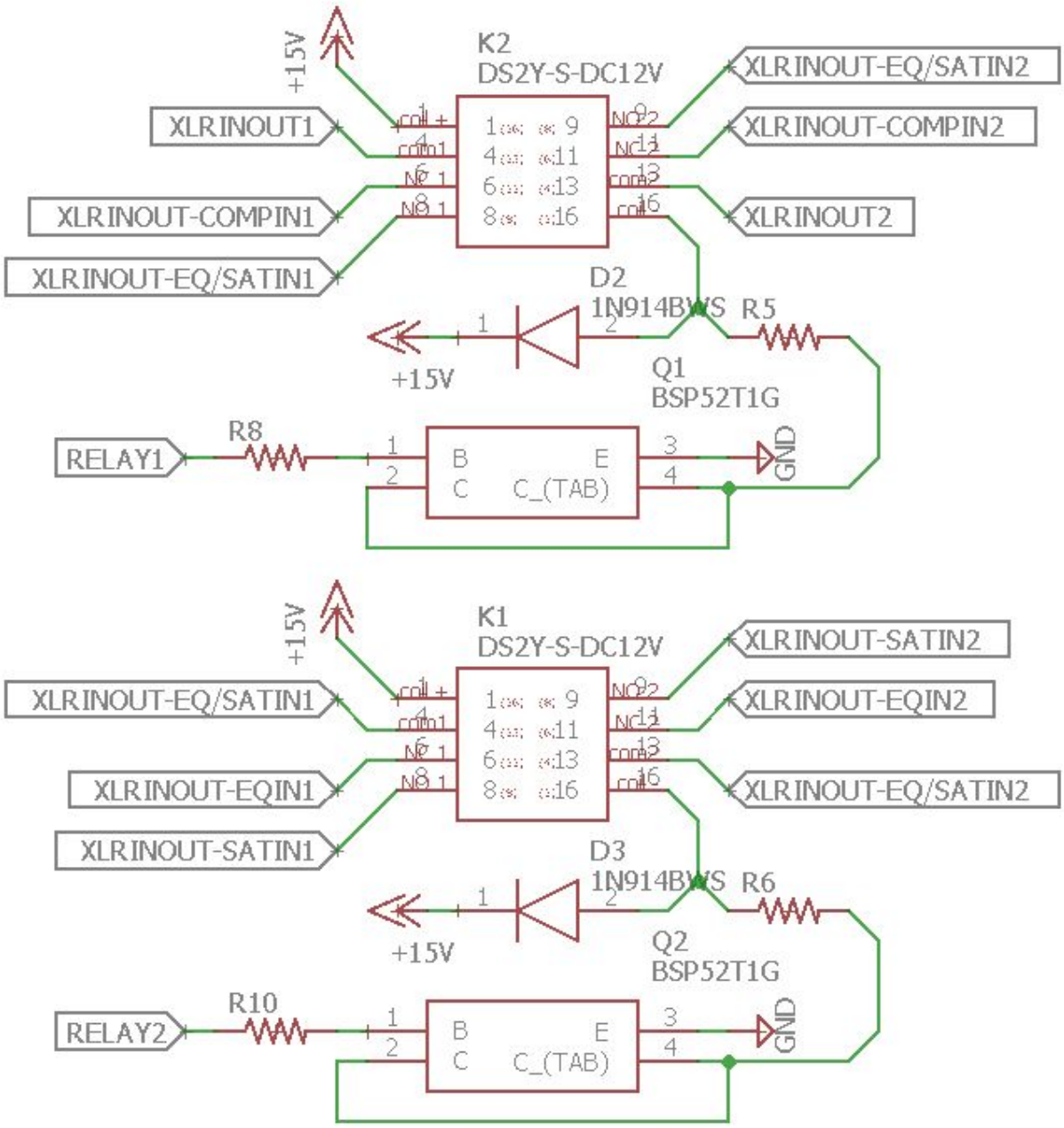

Figure 12. Analog Input Relays Schematic

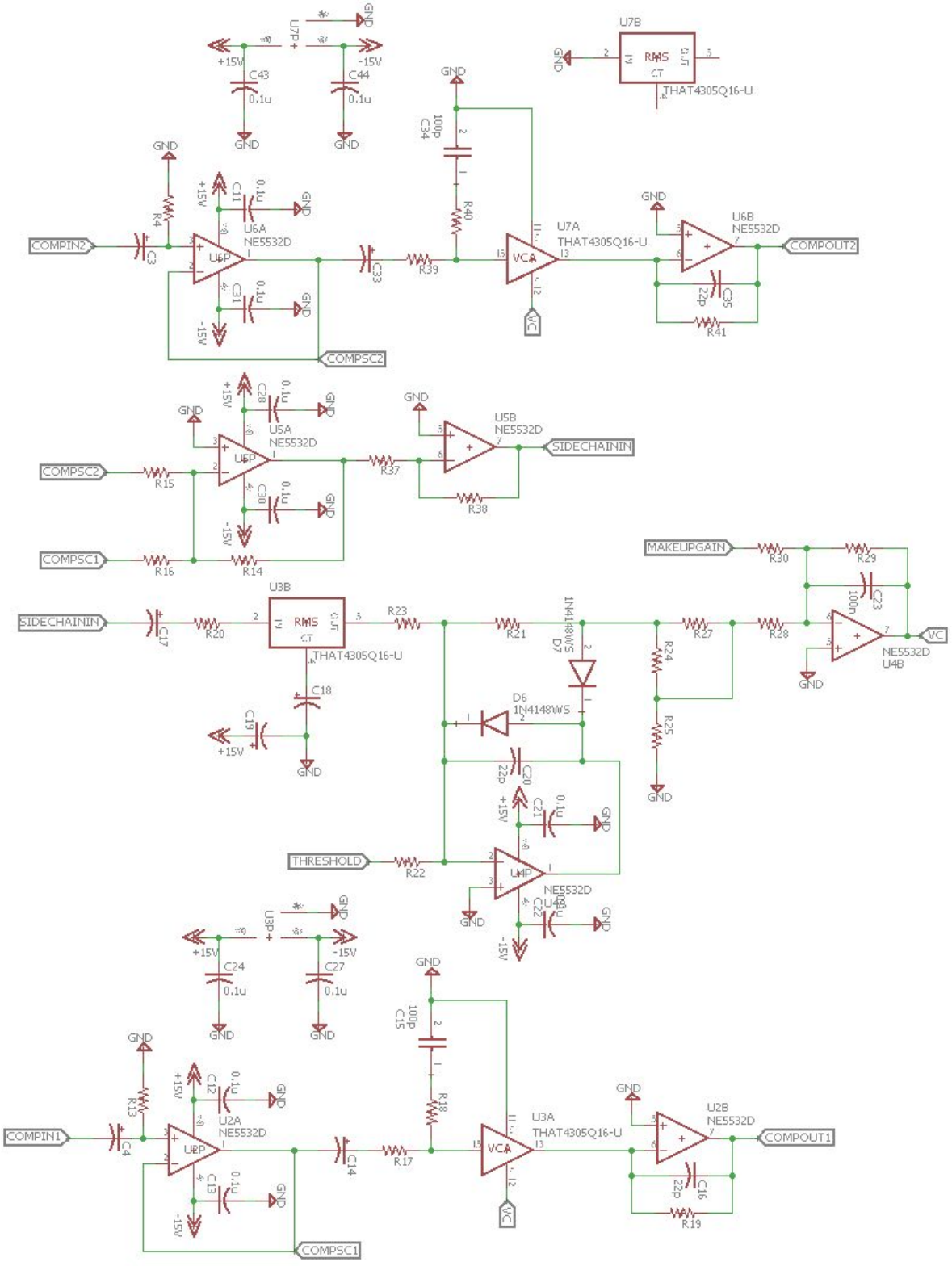

Figure 13. Analog Compressor Schematic

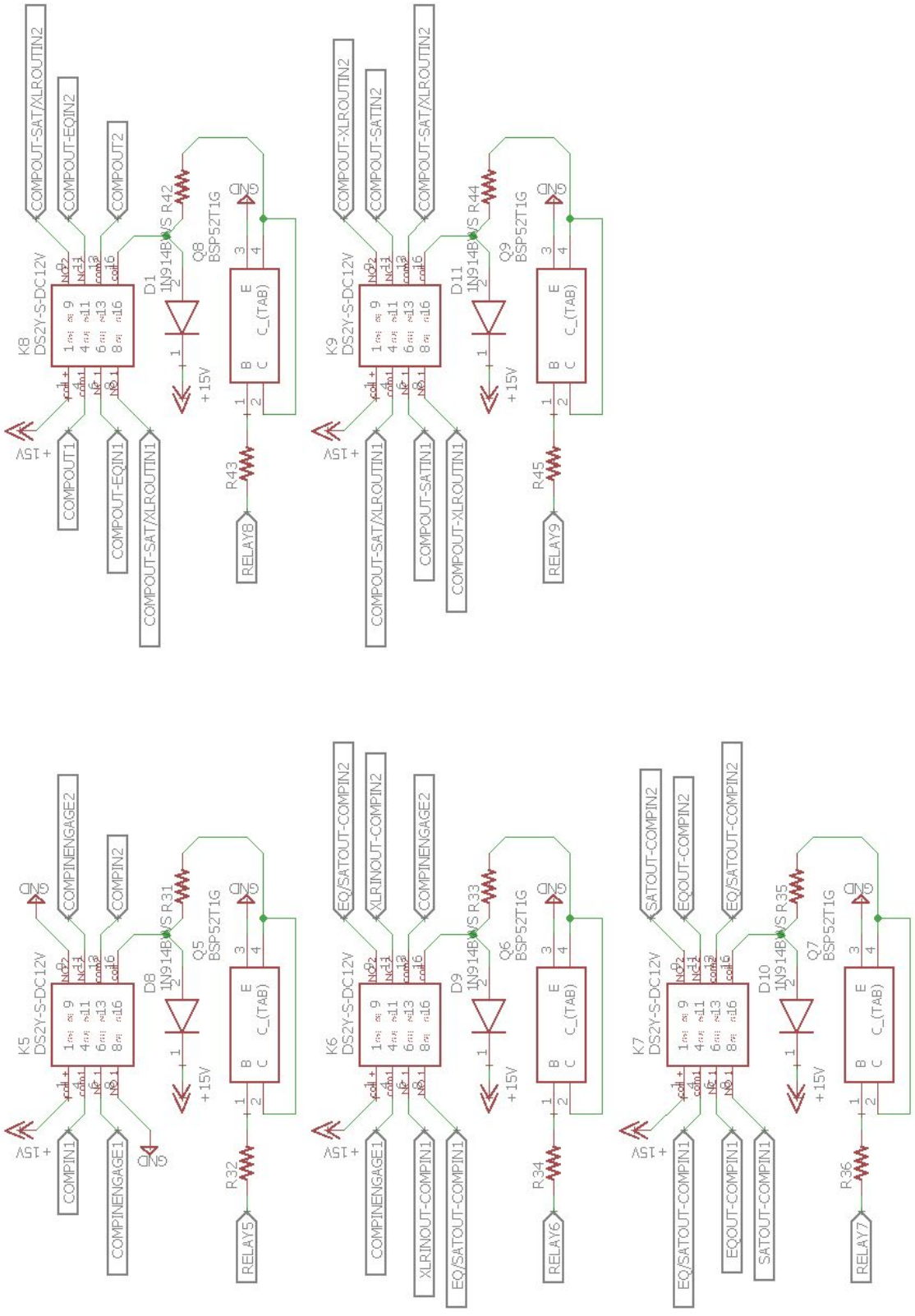

Figure 14. Analog Compressor Relays Schematic

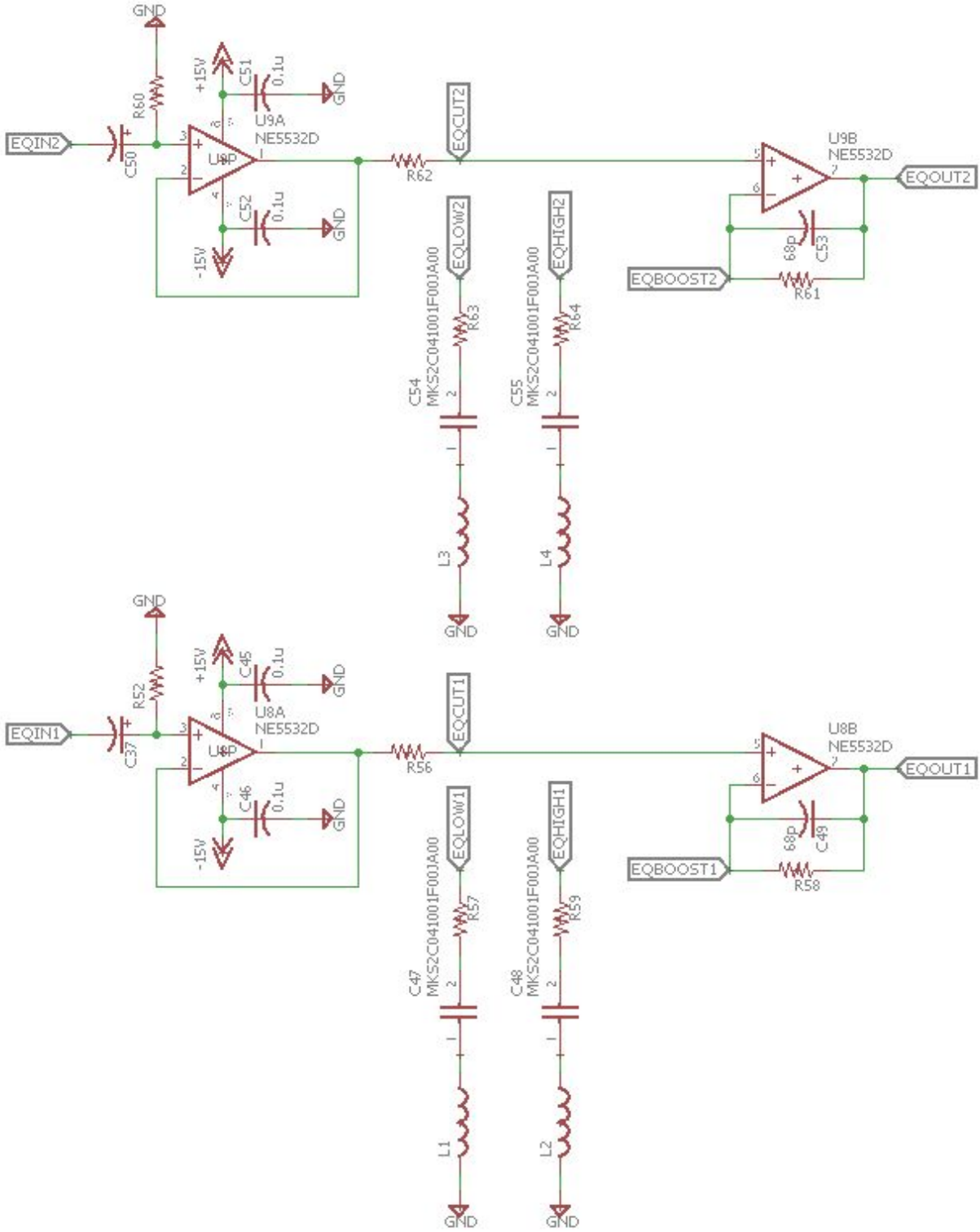

Figure 15. Analog Equalizer Schematic

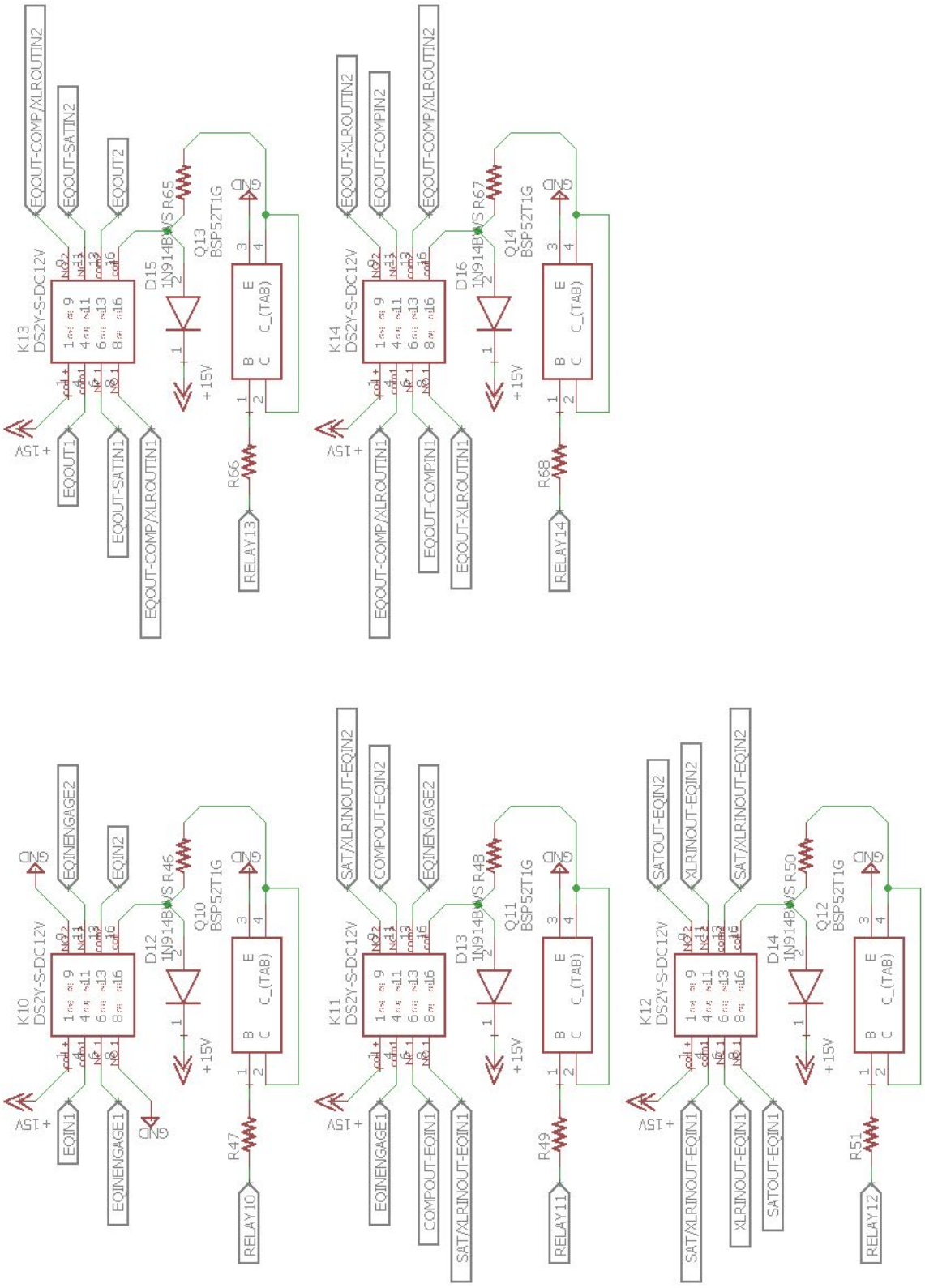

Figure 16. Analog Equalizer Relays Schematic

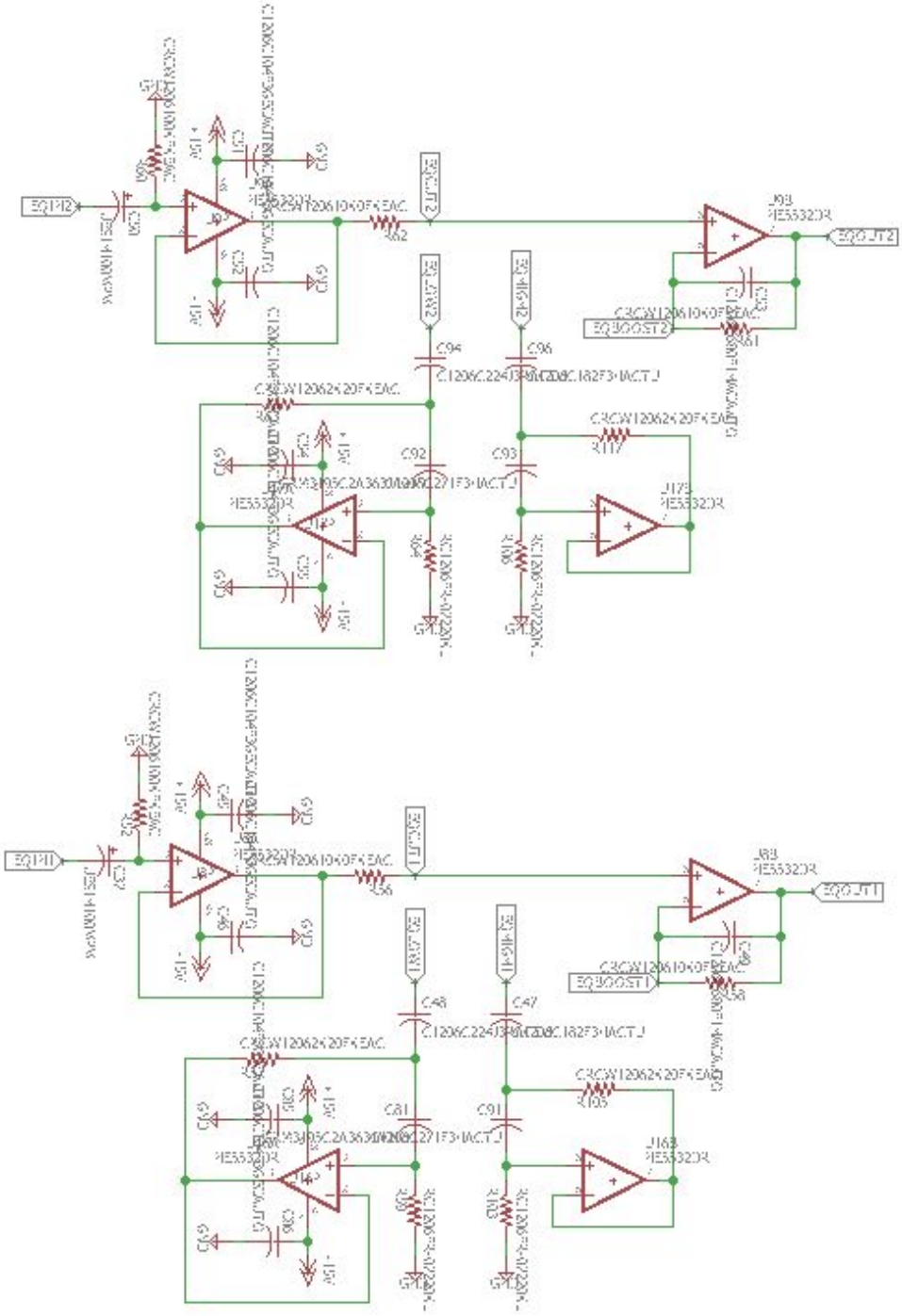

Figure 17. Analog Saturator Schematic

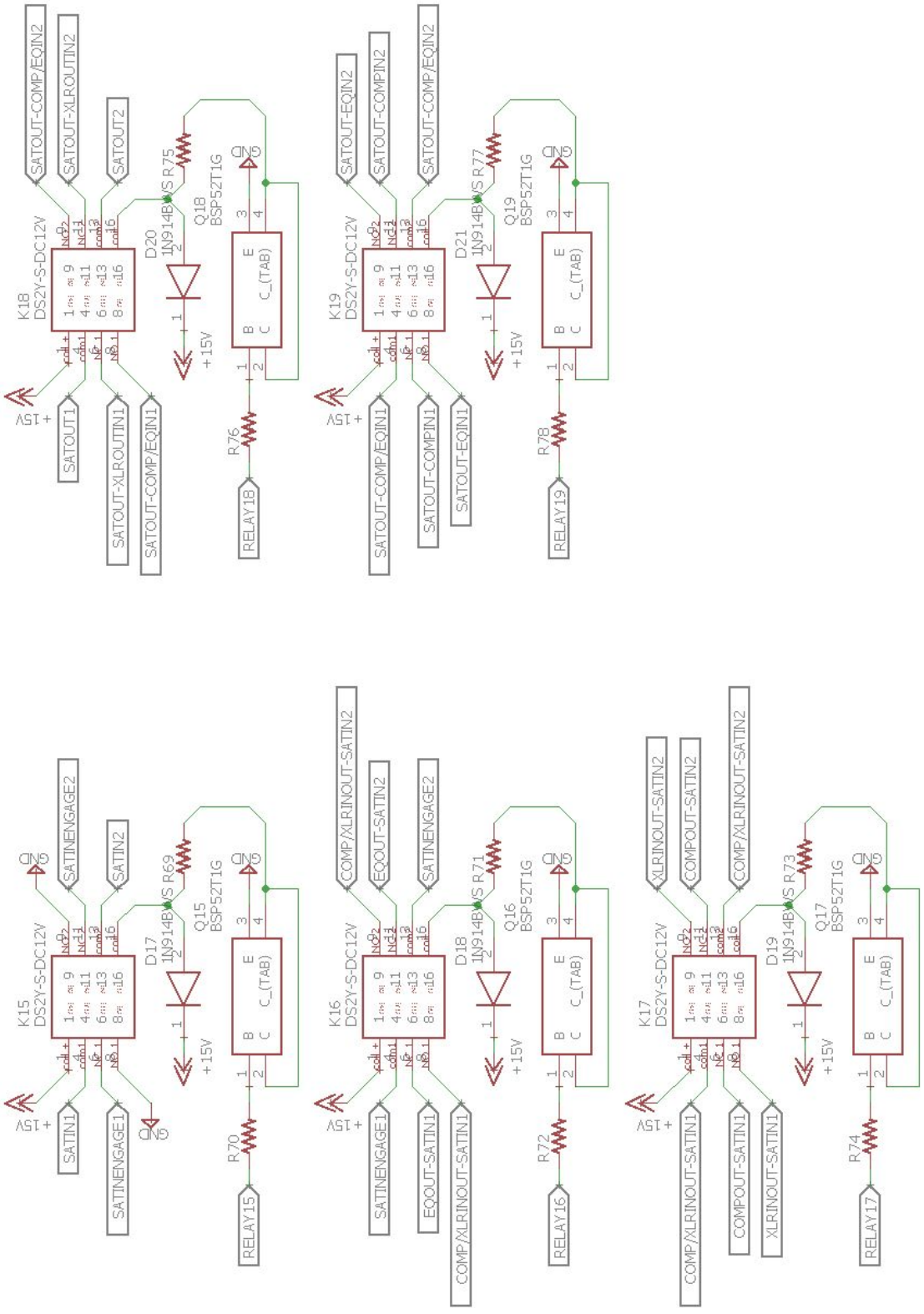

Figure 18. Analog Saturator Relays Schematic

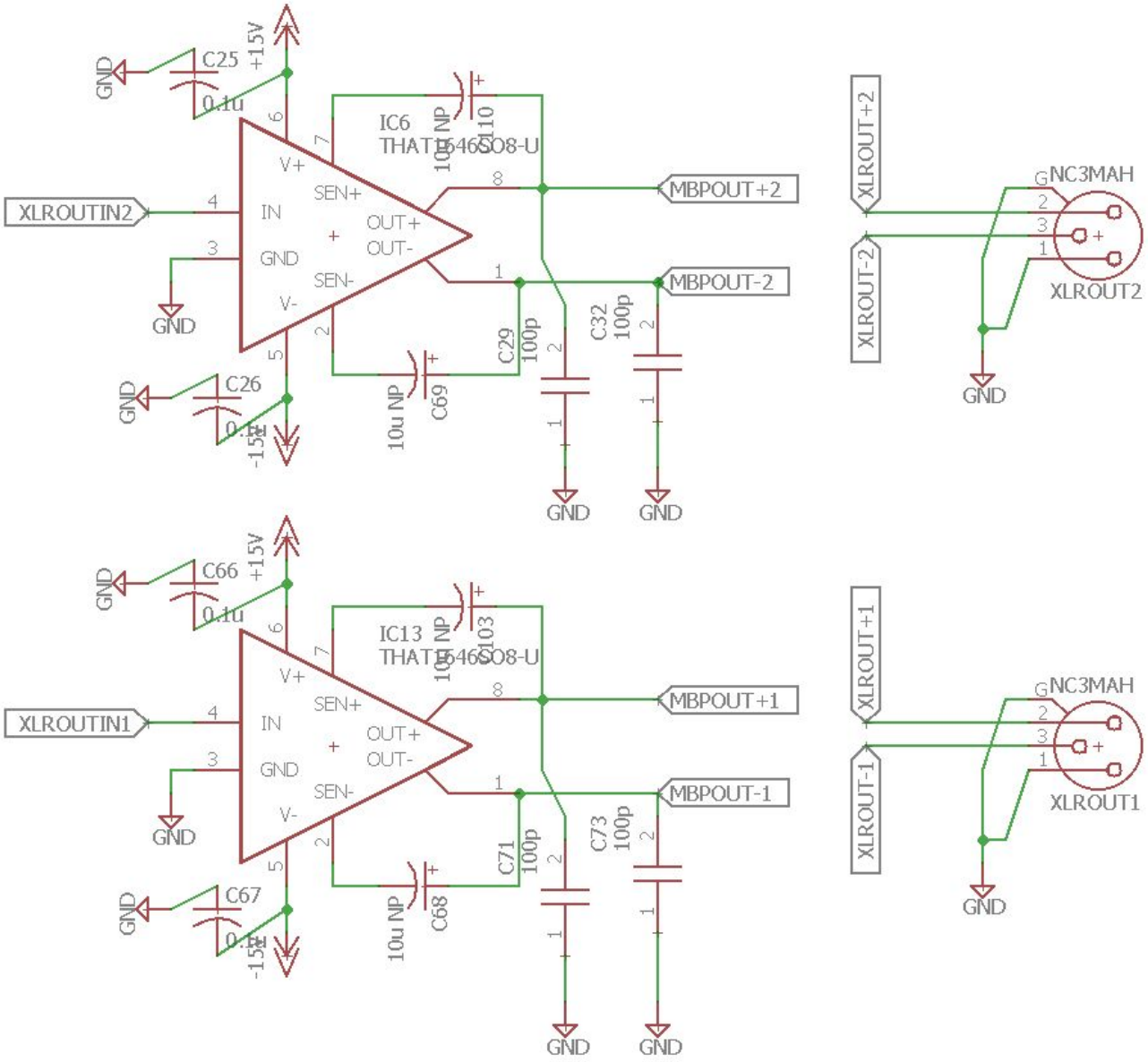

Figure 19. Analog Outputs Schematic

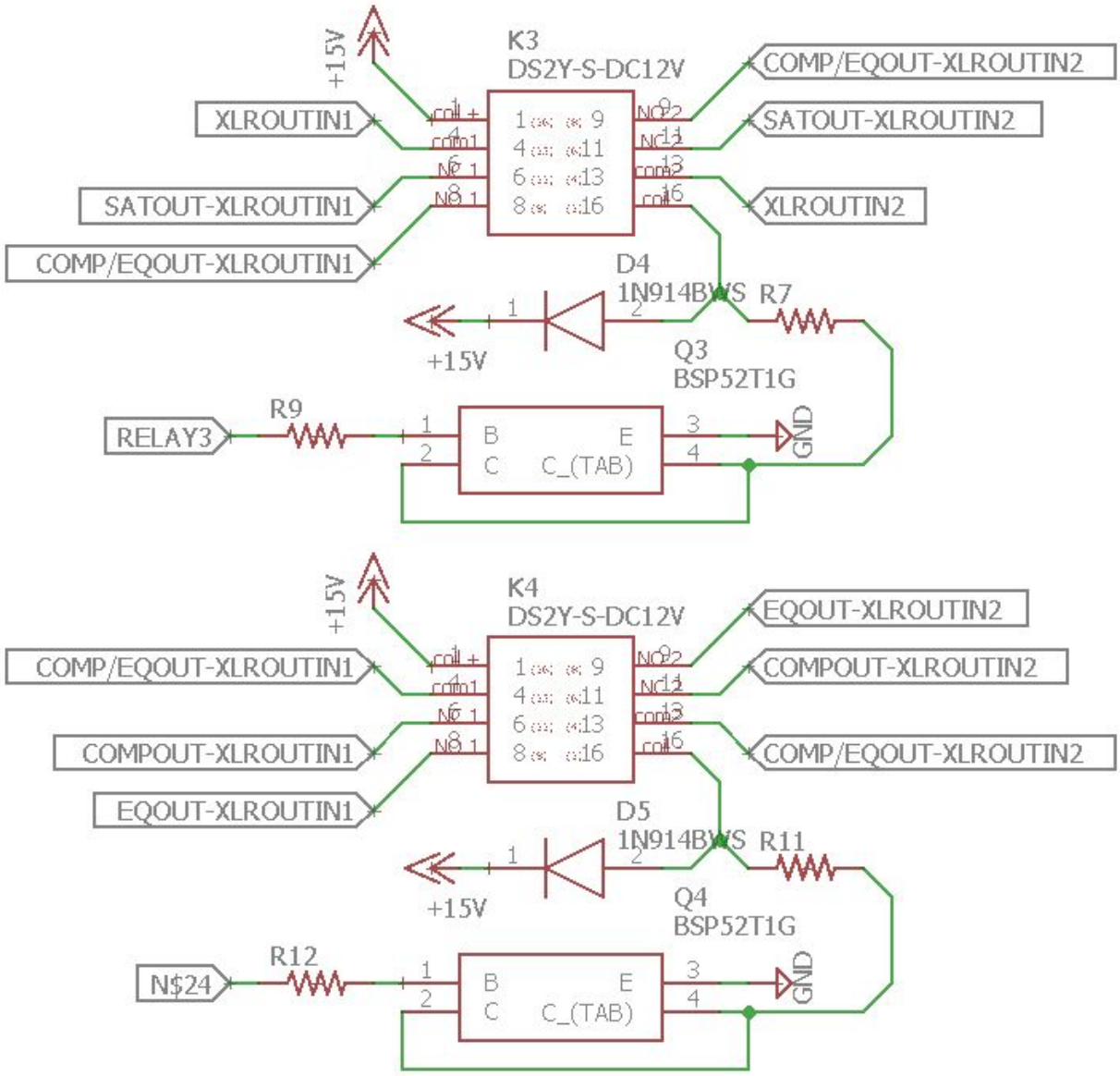

Figure 20. Analog Output Relays Schematic

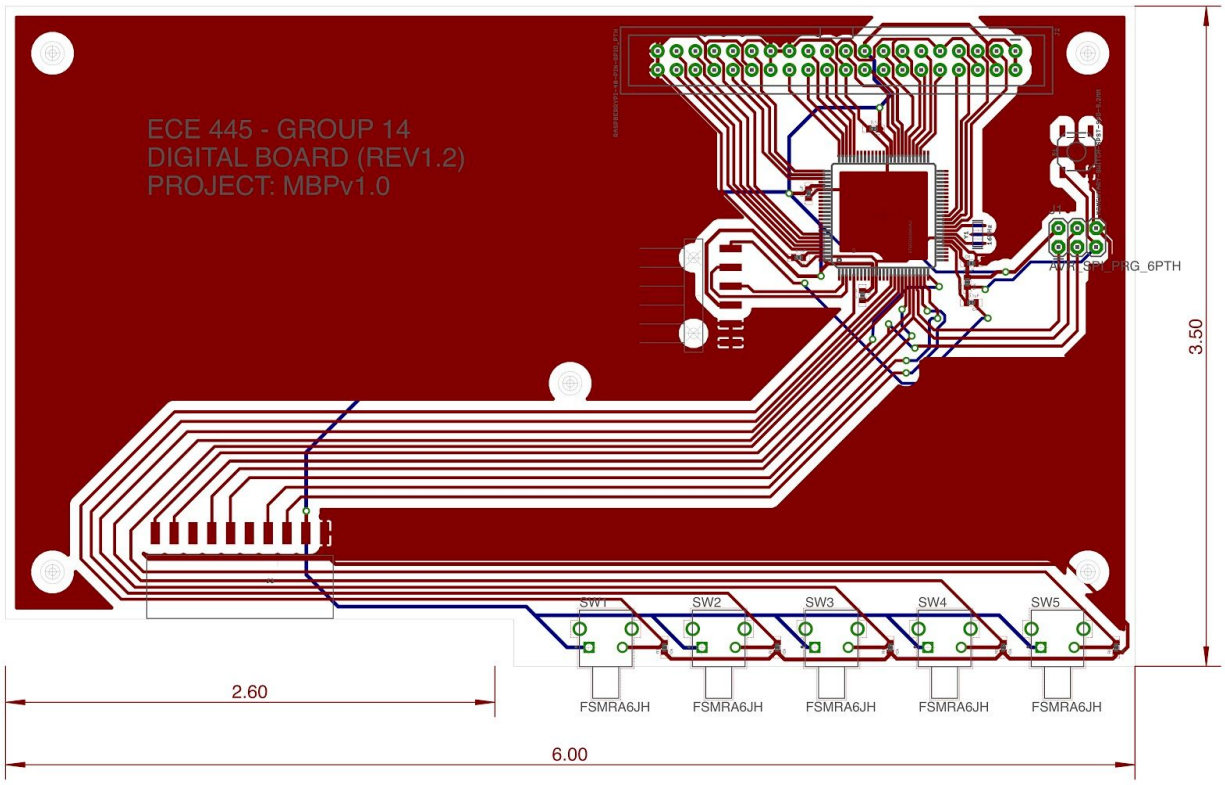

Figure 21. Digital Control Board PCB

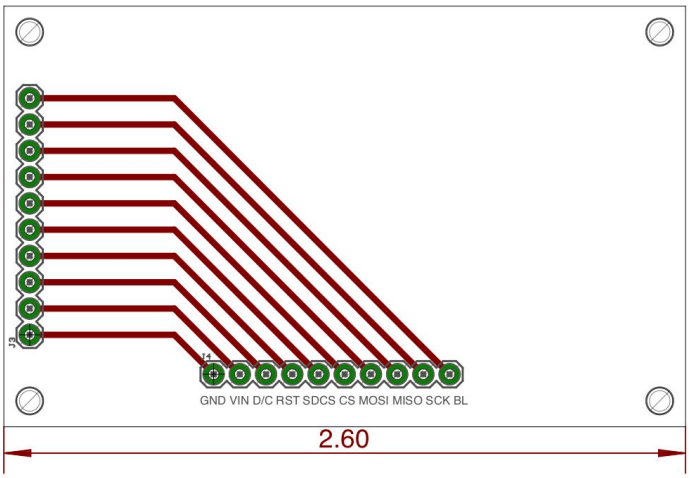

Figure 22. Display Adapter Board PCB

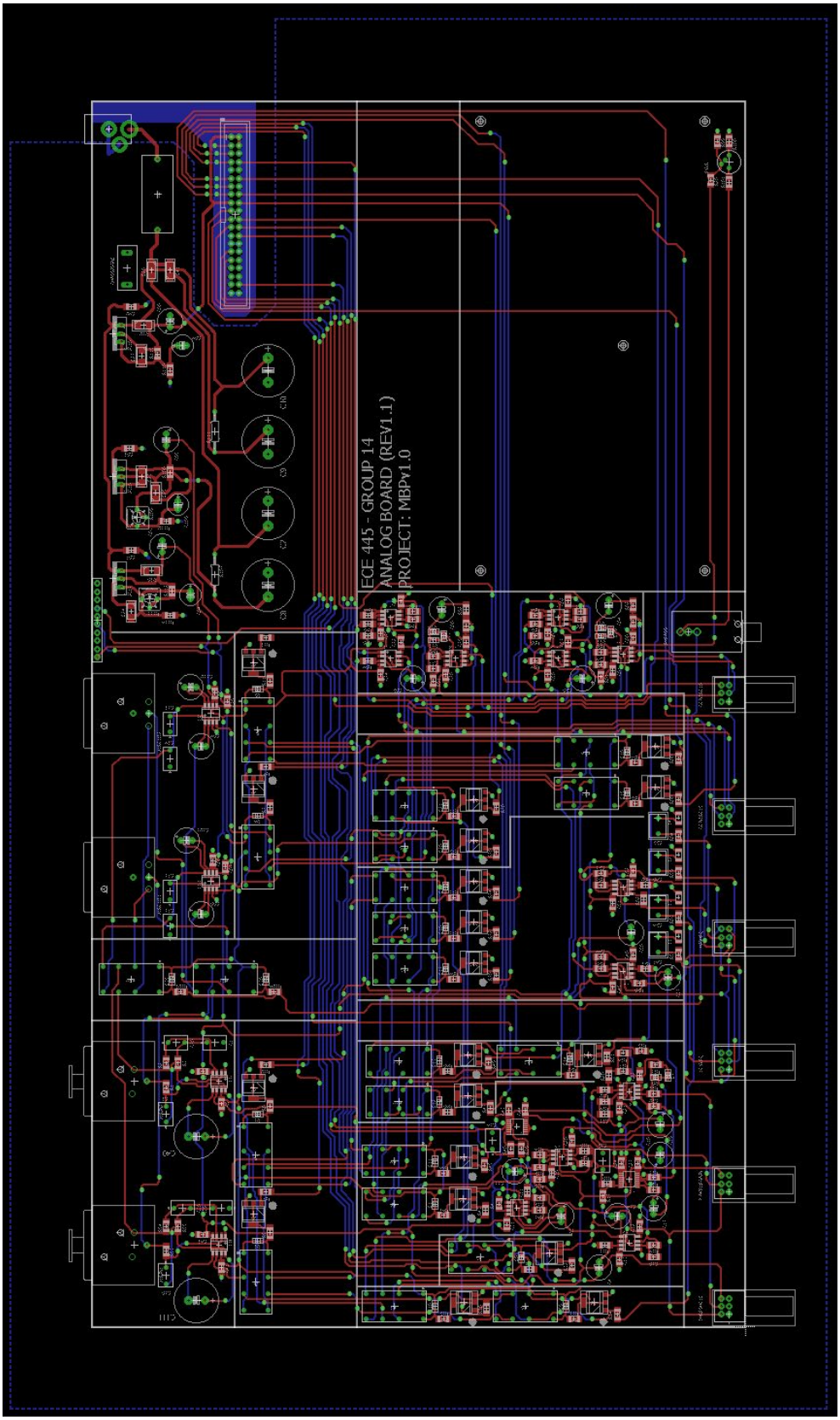

Figure 23. Analog Board PCB Overview

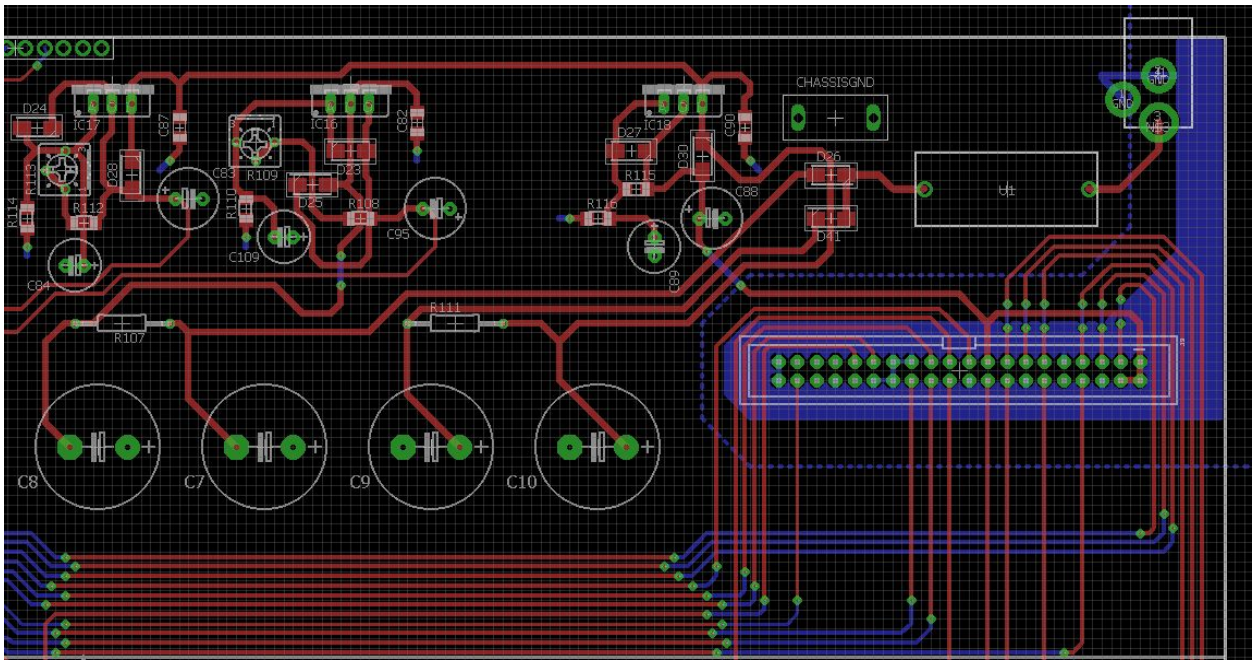

Figure 24. Analog Board: Power Supply Layout

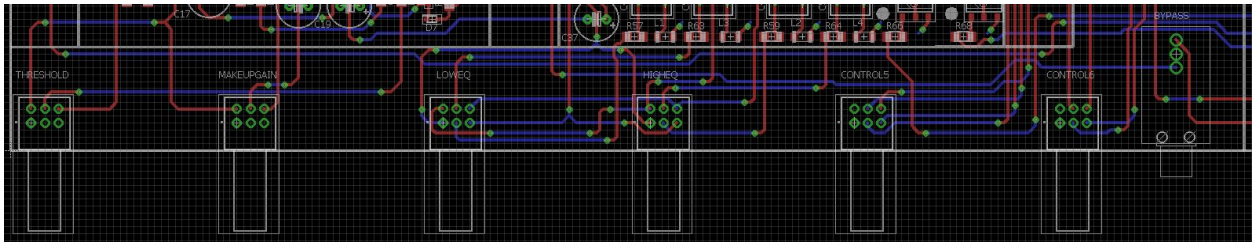

Figure 25. Analog Board: Analog Controls Layout

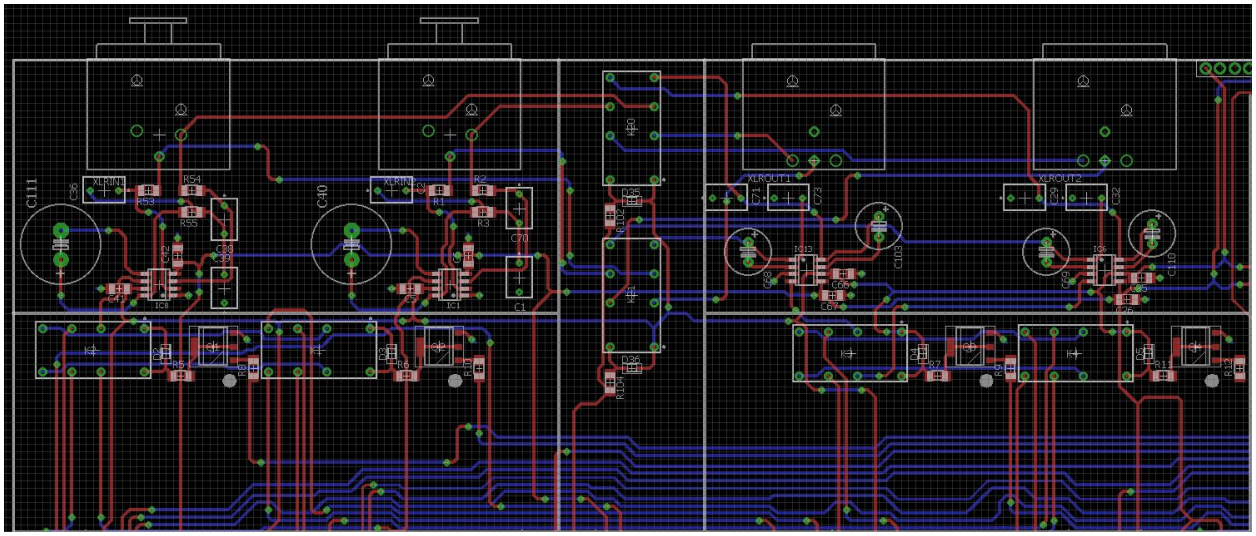

Figure 26. Analog Board: Input/Output Layout

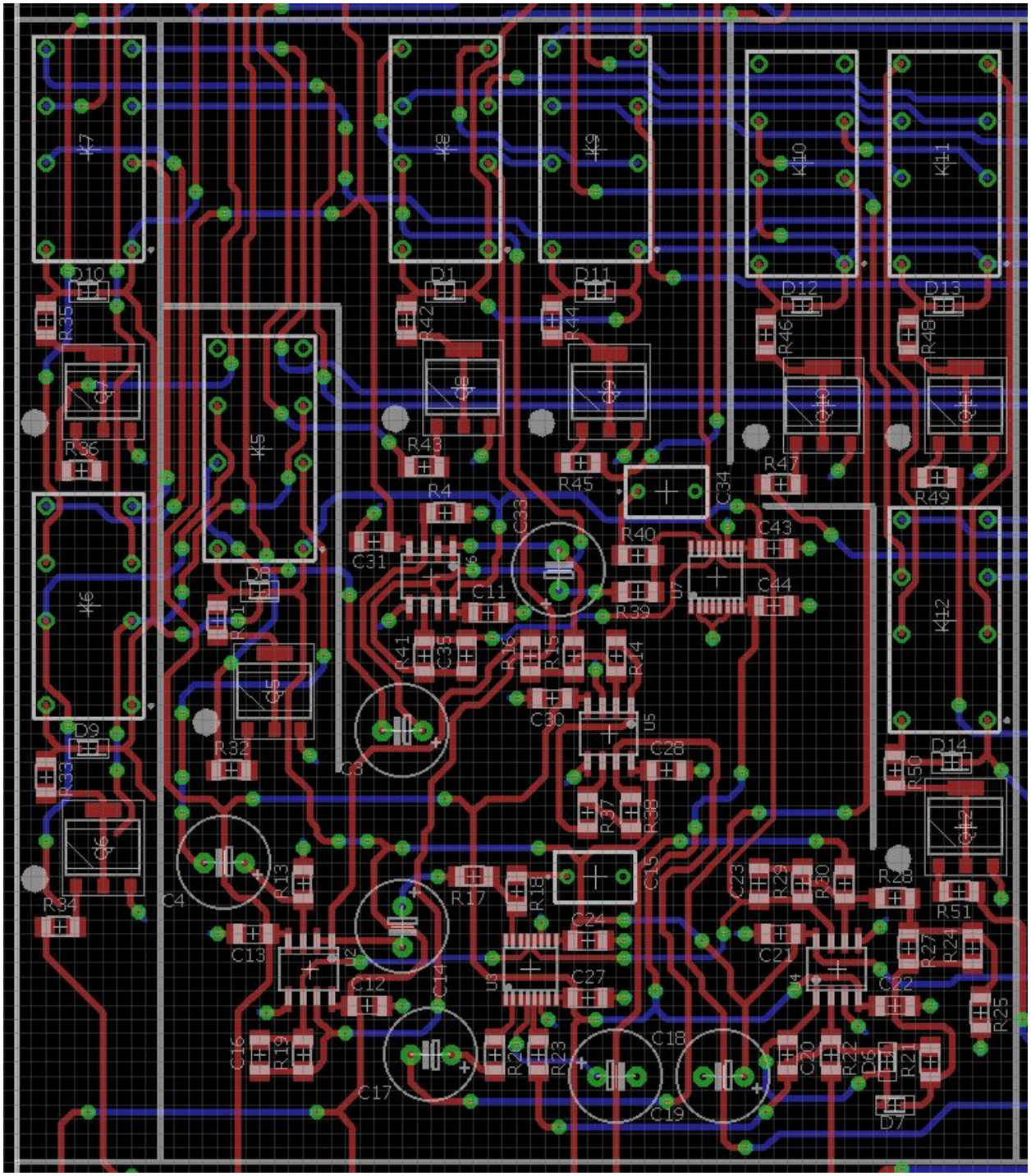

Figure 27. Analog Board: Compressor Layout

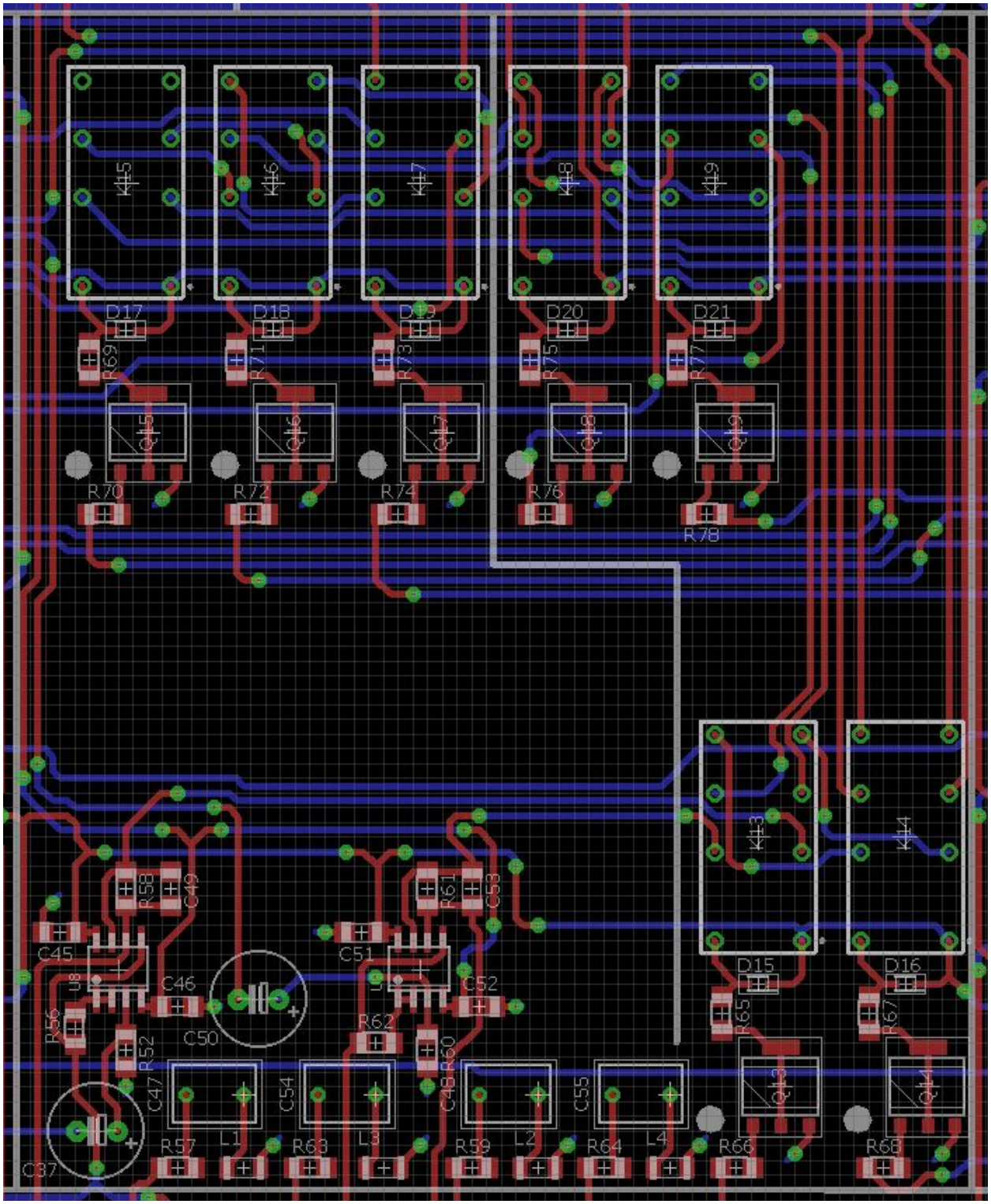

Figure 28. Analog Board: Equalizer Layout

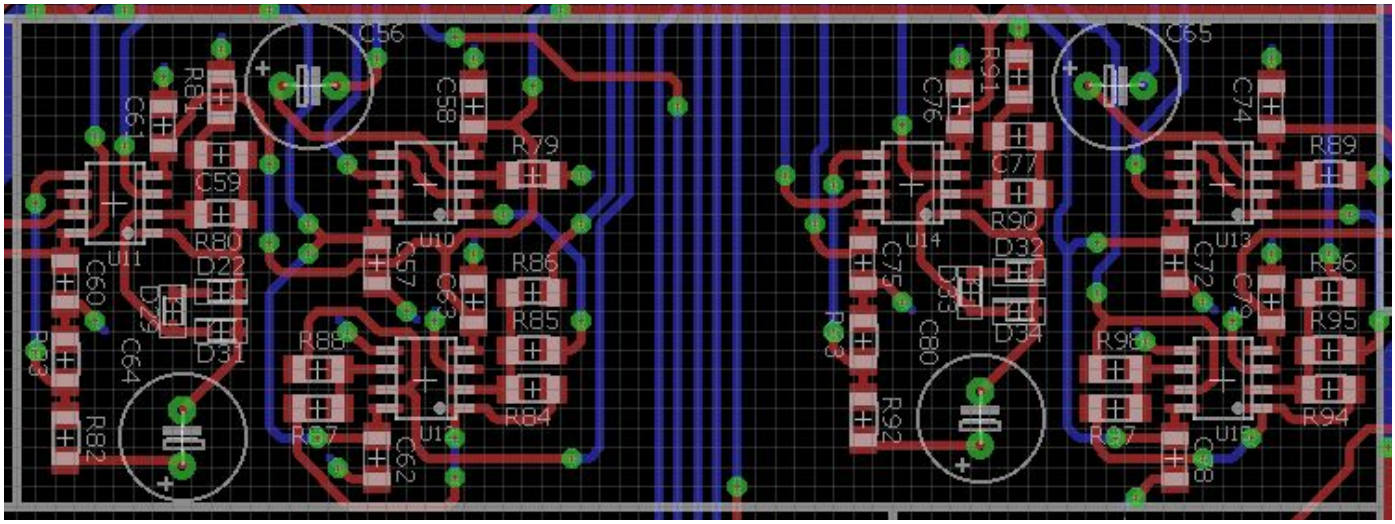

Figure 29. Analog Board: Saturator Layout

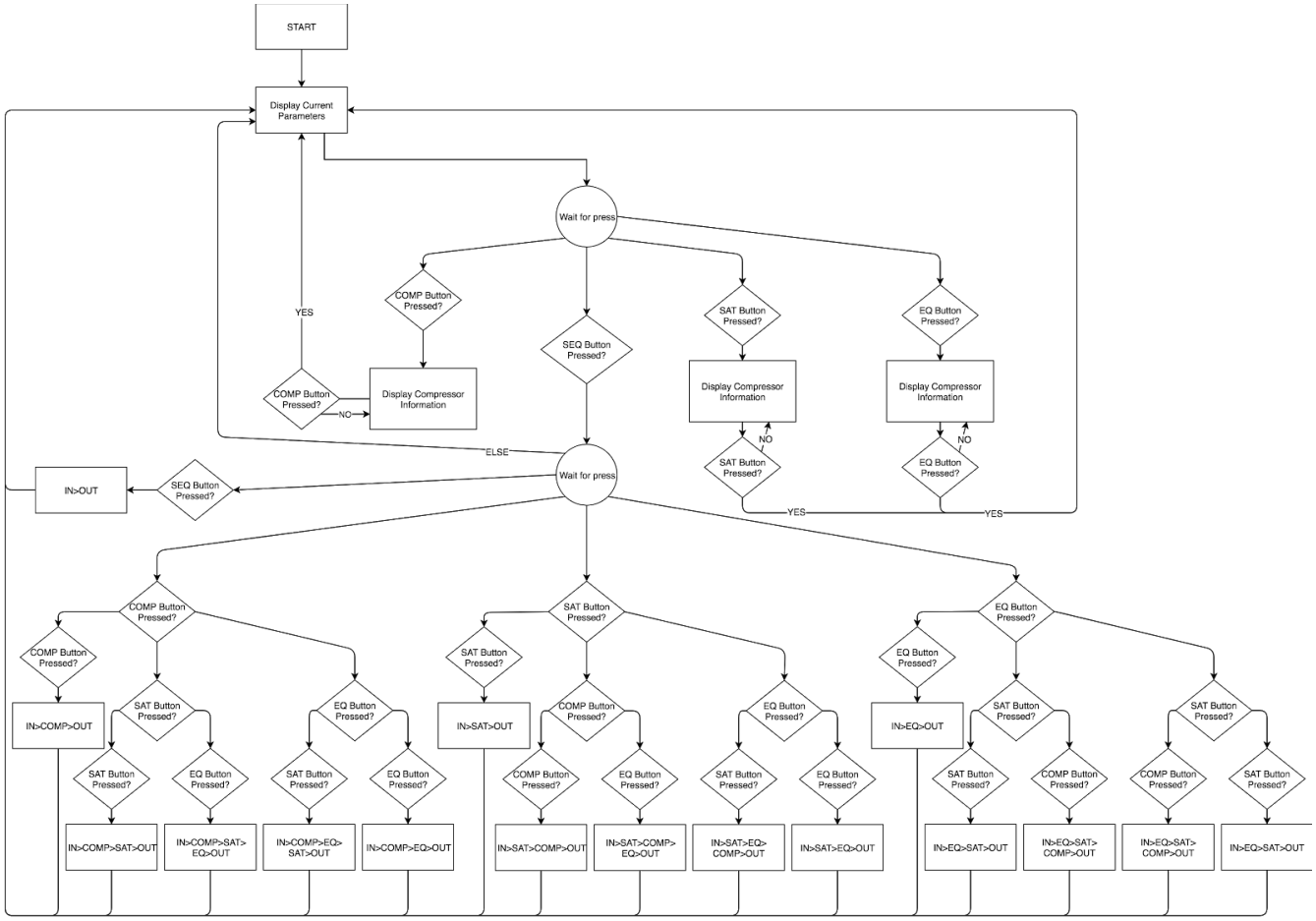

Figure 30. Microcontroller Software Flow Chart

2.4. Tolerance Analysis

2.4.1. Relay Tolerance Analysis

An important piece of our project is the switching logic, specifically the tolerances of acceptable voltages and currents to turn on and off the relays and transistors as described in Figure 10. The BSP52T1 transistor requires a minimum V_{be} turn-on-voltage of 1.9 V. The transistor has a minimum current gain of 1000. Because the relay will hold i_{ce} current at 16 mA, the i_{be} current will be around 16 uA. The maximum base resistor current can be expressed in Eqn 1.

$$\text{Eqn 1.} \quad R = \frac{5V - 1.9V}{16uA} = 185,629\ Ohms$$

Because the transistor has a maximum voltage of 80 V, we have no lower bound of resistance. However, we will include a relatively small 10,000 Ohm resistor to prevent a potential short circuit. Because this resistor has a tolerance of 1%, we will always be lower than the required base resistance. We must also look at the required series resistance to keep the relay to operating at its nominal voltage of 12 V, given a rail voltage of 15 V and a nominal current held constant at 16.7 mA. We calculate this resistance in Eqn 2.

$$\text{Eqn 2.} \quad 15V = 16.7mA \times (720 + R_{series})$$
$$R = 178 \approx 180\ Ohms$$

Using the value of 180 ohms, we can then determine what tolerance of the rail voltage. We hope to have our circuit tolerate $15 \pm 1\ V$, so we will use 16 and 14 as our theoretical edge case rail voltages. The relays have maximum allowed voltage of $1.1 \times 12 = 13.2\ V$, a minimum allowed voltage of $0.7 \times 12 = 8.4\ V$ and a current tolerance of $\pm$ 10% of the nominal current which gives a range of 15.03 mA to 18.37 mA. The series resistor has a tolerance of $\pm$ 1% of its given value of 180 Ohms, and the transistor saturation voltage, V_{ce} can range from 0 V to 1.3 V. Given this information, we can determine if our rail tolerances will allow the relay to operate correctly. If there is maximum theoretical rail value of 16 V and all lower bound worst case scenarios for other components in series, the relay voltage is given Eqn 3.

$$\text{Eqn 3.} \quad V_{rail,\,max} - (R_{series,min})(I_{min}) - V_{ce,min} = V_{relay}$$
$$16\ V - (178.2)(0.01503) - 0 = 13.3\ V$$

This value is only slightly above our desired maximum voltage so our new maximum allowed rail voltage can be expressed by Eqn 4.

$$\text{Eqn 4.}\quad V_{rail,max} - (V_{relay} - V_{relay,desired}) = V_{rail,max,new}$$
$$16 - (13.3 - 13.2) = 15.8\ V$$

We can do a similar calculation for the minimum allowed rail voltage. Assuming we fall within our desired range of 14 V - 15.8 V we obtain a theoretical minimum relay voltage in Eqn 5.

$$\text{Eqn 5.}\quad V_{rail,min} - (R_{series,max})(I_{max}) - V_{ce,max} = V_{relay}$$
$$14\ V - (181.8)(18.37) - 1.8 = 8.861\ V$$

Because we require a voltage of 8.4 V to turn on the relays, we can verify that 14 V is a tolerable minimum for our relay circuits to work. Given this information, there is a tolerance of ± 5% given a nominal rail voltage of 15 V to maintain functionality.

2.4.2. Equalizer Tolerance Analysis

The accuracy of the center frequencies of the filter bands which make up the Equalizer section is dependant on the tolerance of the resonant circuits which constitute each band. The center frequency of each band is determined by Eqn 6.

$$\text{Eqn 6.}\quad f_{center} = \frac{1}{2\pi\sqrt{LC}}$$

Each resonant circuit consists of a resistive load R_L, a capacitor C, and a simulated inductance L. While resistive load R_L and capacitor C depend only on their individual tolerances, the tolerance of the simulated inductance L is dependant on each component of the 'gyrator' sub-circuits which cause simulated inductance according to Eqn 7.

$$\text{Eqn 7.}\quad L_{simulated} = R_L R_{Gry} C_{Gyr}$$

By analyzing the maximum and minimum values of each passive component it and substituting these values into Eqn 6. And Eqn 7. it can be shown that the low frequency band ($f_{lowcenter}$ = 80 Hz) has a range of possible values from 76.67 Hz to 86.43 Hz. As a result, this design is tolerant to the +/-12.5% center frequency constraint of 70 Hz to 90 Hz set out in the design requirements. Similarly, it can be shown that the high frequency band ($f_{highcenter}$ = 10.3 kHz) has a range of possible values from 10.177 kHz to 10.58 kHz. As a result, this design is tolerant to the +/-9.67% center frequency constraint of 9 kHz to 10 kHz set out in the design requirements.

2.4.3. Saturation Tolerance Analysis

In order to ensure the total harmonic distortion contributed by the Saturator section is within the 10% constraint set out by the design requirements, a passive attenuator has been included in the Saturator circuit. While the unaffected signal is passed through the Saturator at unity gain, the affected signal is boosted by 20 dB--in order to achieve the correct harmonic saturation--and then attenuated by 40 dB. As a result, the harmonic distortion products from the Saturator will be at most 20 dB lower than the unaffected signal and comprise no more than 10% of the total signal.

3. Cost and Schedule

3.1. Cost Analysis

Labor:

We chose 40$/hour as an average hourly salary for an ECE graduate from UIUC. We estimated that we will work 15 hours/week over the course of the semester which is 16 weeks.

Eqn 8. (40$/hour) x (15 hours/week * 16 weeks) * 3 people = $28,800

Parts:

Item	Price
Digital Components	$51.61
Analog Components	$350.44
PCB Analog	$146
PCB Digital	$51
Total	$599.05

Table 1. Cost of Components

Eqn 9. Grand Total = $28,800 + $599.05 = $29399.05

3.2. **Schedule**

Week	Clay	Philip	Richard
2/25	Review Design Doc before Review	Prepare slides for Design Review	Prepare presentation for Review
3/4	Order and verify microcontroller for digital design	Write code for microcontroller logic	Build and verify AC/DC Conversion and regulators for PSU
3/11	Finalize Digital PCB designs for first round of orders	Build and verify switch control layout and logic	Finalize Analog PCB designs for first round of orders
3/18	SPRING BREAK (work on Individual Progress Reports)		
3/25	Revise Digital PCB designs for final round of orders	Order and integrate LCD screen	Revise Analog PCB designs for second round of orders
4/1	Order and implement buttons for screen/UI	Build and implement user interface	Build and verify compression circuit
4/8	Build and implement I/O interface	Physical design of circuit and button/knob layout	Build and verify equalization circuit
4/15	Organize and put design in rack mount	Final integration and verification of digital interface	Build and verify saturation circuit
4/22	Start final report	Prepare final presentation	Final design adjustments for final presentation
4/29	Finalize/edit report	Finalize/edit presentation	Prepare design for final presentation

Table 3. Weekly Schedule

4. Discussion of Ethics and Safety

Because our device will use wall power, it is important that all safety guidelines are adhered to in respect to the design of the power block of our device. Improper circuit design can damage other circuits in our device as well as other devices connected to the input and output connections. Most importantly, improper design can lead to injury of the user, due to electrocution. In the scope of this class, we plan to mitigate these concerns by following the direction of course supervisors for power supply design. In the case of an ultimate go-to-market strategy, UL certification will be obtained to inform potential clients that our product is safe to purchase and use.

A potential breach of ethics in our project stems from the use of open source hardware/software. In our project we will be using an ATmega microcontroller as well as the Arduino bootloader. Open source projects allow us greater flexibility, affordability, and reliability by using work that is not our own. Although this work is legal to use in the scope of our project, it is important that we follow proper ethics guidelines of the open source community. Specifically, it is important to not claim anyone else's work as your own work as this would violate IEEE Code of Ethics #7: "...to credit properly the contributions of others" [10]. To avoid this breach of ethics we will explicitly credit any contributions to our project from ATmega hardware and Arduino software and make sure that protected intellectual property is not copied without consent.

5. Citations

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