MP3

• Follow up of MP2
• Automated EDA tools to synthesize controller
• Logic Synthesis: compile your HDL
• Automatic Place & Route:
  – The synthesized network (control block)
  – Integrate Control and Datapath
• Deadline: Dec 14th at 11:59pm
Our ASIC Design Flow

MP2
- Standard Cell Library
- Cadence Virtuoso
- Datapath Schematic
- NC-Verilog
- Artist DRC
- Artist LVS
- Full Custom Design

MP3
- Behavioral HDL
- Synopsys Design Vision
- Synthesis
- Schematic Netlist
- Cadence Encounter
- Place & Route
- Controller Layout
- Am2901 Layout
MP3 Overview

• Datapath design: MP2
• **Control logic:** MP3
• Tools: load them *in order*
  – Module load Cadence
  – Module load Synopsys_x86-64

MP3: Synthesis, place & route. Automatically synthesized with CAD tools (c.f. full manual design in MP2)

MP2 part 1: Schematic, simulation
MP2 part 2: Layout, DRC, LVS
## Manual vs Automated Design

<table>
<thead>
<tr>
<th>Task</th>
<th>Human Engineer</th>
<th>Design Automation Tools</th>
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<tbody>
<tr>
<td>Logic optimization</td>
<td>Full knowledge of Boolean Algebra, plus you can go back and change the overall topology</td>
<td>Early days: Incremental optimization based on initial specification + “Guess and check.” Final results based on initial approximation</td>
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<td>Nowadays: Integrated optimization considering layout as well. It can outperform manual design in a big margin, especially if the design is large. It does not need to be incremental.</td>
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<tr>
<td>Cell Design</td>
<td>You know every instance of how every cell will be used, and design for one process.</td>
<td>Our MOSIS-based cell library is generalized for many manufacturers and for ease of use to tools</td>
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<tr>
<td>Integration &amp; Routing</td>
<td>Ability to discover physical realities, learn, and revise.</td>
<td>Early days: Designed for speed and generality. Placement is a best guess, routing cannot modify</td>
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<td>Nowadays: Automation can do a much better job when design is complex because both placement and routing are NP-hard problems. Multi-step, integrated optimization algorithms are developed to consider numerous objectives.</td>
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Part I. Synthesis

- **Logic Synthesis**: process by which an abstract form of desired circuit behavior, typically at RTL, is turned into a design implementation in terms of logic gates

- Tool: Synopsys Design Vision

- Input: controller.v (HDL from MP2)

- Technology node: tsmc250target.dc

- Timing constraints
  - All signal pins, especially `select_a, select_b`
  - Maximum rise/fall time: 275ps, 325ps
Part II. Place & Route (1)

- **Placement**: decides where to place all electronic components, circuitry, and logic elements in a generally limited amount of space.

- **Routing**: decides exact design of all the wires needed to connect the placed components.

- This step must follow rules, limitations of the manufacturing process.
Part II. Place & Route (2)

- Tool: Cadence Virtuoso, Encounter (P&R)
- Relative placement
  - Controller placed *above* the Datapath
  - Define approximate floorplan area boundary
- Routing setting
  - Set pin, routing blockage (not to interfere with datapath)
  - Fix control pin locations
  - Place power rails
- Place standard cells & Route
Verification & Analysis

• Check any DRC violation
• Additional verification (beyond this MP)
• Analyze final area of your controller
  – Check area effective utilization
• Based on your MP2 datapath design, your controller footprint, routing complexity will vary
Submissions

• Synthesis (constraint: rise/fall=275, 325)
  – Record controller area
  – Controller schematic

• Place & Route
  – Summary report

• Top-level layout
  – Complete AM2901: Datapath + Controller
  – Measure and calculate the total layout area
Simulation

• Ensure your design works properly
• Netlist (schematic), RTL (hand-written or synthesized), Stimulus (test inputs)
• Run the *test program* provided and compare the output with golden
• The output sequence should be 2, 9, 2, 7, 9, 4, 0, 4, 2, B
• The wave form should look like this...
Design Competition

• Goal: Minimize the final area (datapath + controller)
• Requirements: Correctly working design with design criteria met to participate competitions
  – No metal above metal 3
  – ptp/ntap for every cell
  – Transistor width: pmos $\geq 720$nm, nmos $\geq 360$nm
  – No poly routes longer than 10um
  – ...

• Bonus: points towards your final grade
  – 1st place: 3 points (1.5% of total grade)
  – 2nd place: 2 points (1% of total grade)
  – 3rd place: 1 point (0.5% of total grade)