Lecture 3: Circuits & Layout

Deming Chen

Slides based on the initial set from David Harris
Outline

- CMOS Gate Design
- Pass Transistors
- CMOS Latches & Flip-Flops
- Standard Cell Layouts
- Stick Diagrams

- Reading: 1.4.1-6, 1.5.3-5
Complementary CMOS

- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS

<table>
<thead>
<tr>
<th></th>
<th>Pull-up OFF</th>
<th>Pull-up ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-down OFF</td>
<td>Z (float)</td>
<td>1</td>
</tr>
<tr>
<td>Pull-down ON</td>
<td>0</td>
<td>X (crowbar)</td>
</tr>
</tbody>
</table>
Series and Parallel

- **nMOS**: 1 = ON
- **pMOS**: 0 = ON
- **Series**: both must be ON
- **Parallel**: either can be ON
Conduction Complement

- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS

- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel
Activity:
- Sketch a 4-input CMOS NOR gate

[Diagram showing a 4-input CMOS NOR gate with inputs A, B, C, D and output Y]
Compound Gates

- Compound gates can do any inverting function
- Ex: \( Y = A \cdot B + C \cdot D \) (AND-AND-OR-INVERT, AOI22)

(a) 

(b) 

(c) 

(d) 

(e) 

(f)
Example: O3AI

\[ Y = (A + B + C) \cdot D \]
Signal Strength

- Strength of signal
  - How close it approximates ideal voltage source
- V_{DD} and GND rails are strongest 1 and 0
- nMOS pass strong 0
  - But degraded or weak 1
- pMOS pass strong 1
  - But degraded or weak 0
- Thus nMOS are best for pull-down network
Pass Transistors

Transistors can be used as switches

\[ g = 0 \]
\[ s \rightarrow \neg \rightarrow d \]
\[ g = 1 \]
\[ s \rightarrow \rightarrow d \]

Input \( g = 1 \) Output
0 \( \rightarrow \rightarrow \) strong 0
1 \( \rightarrow \rightarrow \) degraded 1

Input \( g = 0 \) Output
0 \( \rightarrow \rightarrow \) degraded 0
1 \( \rightarrow \rightarrow \) strong 1
Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

\[ g = 0, \ gb = 1 \]
\[ g = 1, \ gb = 0 \]
\[ a \rightarrow b \]

Input | Output
--- | ---
\[ g = 1, \ gb = 0 \]
\[ 0 \rightarrow \text{strong 0} \] upper

\[ g = 1, \ gb = 0 \]
\[ 1 \rightarrow \text{strong 1} \] lower
Tristates

**Tristate buffer produces Z when not enabled**

<table>
<thead>
<tr>
<th>EN</th>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Nonrestoring Tristate

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y

\[ \text{EN} \]
\[ A \rightarrow Y \]
\[ \text{EN} \]
Tristate Inverter

- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output

\[ Y = \begin{cases} \text{Z} & \text{if EN} = 0 \\ \overline{A} & \text{if EN} = 1 \end{cases} \]
**Multiplexers**

- A 2:1 multiplexer chooses between two inputs.

<table>
<thead>
<tr>
<th>S</th>
<th>D1</th>
<th>D0</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
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<td>1</td>
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</table>

![Multiplexer Diagram]
Gate-Level Mux Design

- $Y = SD_1 + \bar{SD}_0$ (too many transistors)
- How many transistors are needed? 20
Transmission Gate Mux

- Nonrestoring mux uses two transmission gates
  - Only 4 transistors
Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter
4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates
D Latch

- When $CLK = 1$, latch is *transparent*
  - $D$ flows through to $Q$ like a buffer
- When $CLK = 0$, the latch is *opaque*
  - $Q$ holds its old value independent of $D$

*a.k.a. transparent latch or level-sensitive latch*
D Latch Design

- Multiplexer chooses D or old Q
D Latch Operation

CLK = 1

CLK = 0

D

Q

Q

D

Q

CLK

D

Q
D Flip-flop

- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. positive edge-triggered flip-flop, master-slave flip-flop

![D Flip-flop Diagram]
D Flip-flop Design

- Built from master and slave D latches
D Flip-flop Operation

CLK = 0

CLK = 1

CLK

D

Q
Race Condition

- Back-to-back flops can malfunction from clock skew
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*
Nonoverlapping Clocks

- Nonoverlapping clocks can prevent races
  - As long as nonoverlap exceeds clock skew
  - Industry manages skew more carefully

![Nonoverlapping Clocks Diagram](image-url)
Gate Layout

- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - $V_{DD}$ and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts
Example: Inverter

(a) 

(b) Substrate T
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 $V_{DD}$ rail at top
- Metal1 GND rail at bottom
- 32 $\lambda$ by 40 $\lambda$
Stick diagrams help plan layout quickly
- Need not be to scale
- Draw with color pencils or dry-erase markers

Stick Diagrams

\( V_{DD} \)

\[ \begin{align*}
A & \quad Y \\
\times & \quad \times \\
GND & \quad \text{INV}
\end{align*} \]

\( V_{DD} \)

\[ \begin{align*}
A & \quad B & \quad C \\
\times & \quad \times & \quad \times \\
\times & \quad \times & \quad \times \\
GND & \quad \text{NAND3}
\end{align*} \]

Legend:
- blue: metal1
- red: poly
- green: ndiff
- yellow: pdiff
- black: contact
A wiring track is the space required for a wire
- 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
Transistors also consume one wiring track
Well spacing

- Wells must surround transistors by 6 \( \lambda \)
  - Implies 12 \( \lambda \) between opposite transistor flavors
  - Leaves room for one wire track
Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in \( \text{mm} \)
Example: O3Al

Sketch a stick diagram for O3Al and estimate area

\[ Y = (A + B + C) \cdot D \]

Diagram:
- 6 tracks = 48
- 5 tracks = 40
Summary

- MOS Transistors are stack of gate, oxide, silicon
- Can be viewed as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

Next lecture:
- A simple MIPS Microprocessor
- Reading: 1.7-1.12