Lecture 3: Circuits & Layout

Slides courtesy of Deming Chen

Slides based on the initial set from David Harris
Outline

- CMOS Gate Design
- Pass Transistors
- CMOS Latches & Flip-Flops
- Standard Cell Layouts
- Stick Diagrams

- Reading: 1.4, 1.5.3-5
Complementary CMOS

- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS

<table>
<thead>
<tr>
<th></th>
<th>Pull-up OFF</th>
<th>Pull-up ON</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull-down OFF</td>
<td>Z (float)</td>
<td>1</td>
</tr>
<tr>
<td>Pull-down ON</td>
<td>0</td>
<td>X (crowbar)</td>
</tr>
</tbody>
</table>

![CMOS circuit diagram](https://via.placeholder.com/150)
Series and Parallel

- nMOS: 1 = ON
- pMOS: 0 = ON
- **Series**: both must be ON
- **Parallel**: either can be ON

(a) 
\[ \begin{array}{c|c|c|c}
\text{g1} & \text{g2} & a & b \\
\hline
0 & 0 & ON & OFF \\
1 & 0 & OFF & OFF \\
0 & 1 & OFF & OFF \\
1 & 1 & OFF & ON \\
\end{array} \]

(b) 
\[ \begin{array}{c|c|c|c}
\text{g1} & \text{g2} & a & b \\
\hline
0 & 0 & OFF & OFF \\
1 & 0 & OFF & OFF \\
0 & 1 & OFF & OFF \\
1 & 1 & OFF & OFF \\
\end{array} \]

(c) 
\[ \begin{array}{c|c|c|c}
\text{g1} & \text{g2} & a & b \\
\hline
0 & 0 & OFF & ON \\
1 & 0 & ON & ON \\
0 & 1 & ON & ON \\
1 & 1 & ON & ON \\
\end{array} \]

(d) 
\[ \begin{array}{c|c|c|c}
\text{g1} & \text{g2} & a & b \\
\hline
0 & 0 & OFF & OFF \\
1 & 0 & OFF & OFF \\
0 & 1 & OFF & OFF \\
1 & 1 & OFF & ON \\
\end{array} \]
Conduction Complement

- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: $Y=0$ when both inputs are 1
  - Thus $Y=1$ when either input is 0
  - Requires parallel pMOS

- Rule of Conduction Complements
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel
Activity:
- Sketch a 4-input CMOS NOR gate
Compound Gates

- Compound gates can do any inverting function
- Ex: \( Y = A \cdot B + C \cdot D \) (AND-AND-OR-INVERT, AOI22)

(a) 
(b) 
(c) 
(d) 
(e) 
(f)
Example: O3AI

\[ Y = \overline{(A + B + C)} \cdot D \]
Signal Strength

- *Strength* of signal
  - How close it approximates ideal voltage source
- \( V_{DD} \) and GND rails are strongest 1 and 0
- nMOS pass strong 0
  - But degraded or weak 1
- pMOS pass strong 1
  - But degraded or weak 0
- Thus nMOS are best for pull-down network
Pass Transistors

Transistors can be used as switches

\[
\begin{align*}
\text{Input} & \quad g = 1 & \quad \text{Output} \\
& \quad 0 \rightarrow \text{strong} 0 \\
& \quad 1 \rightarrow \text{degraded} 1 \\
\end{align*}
\]
Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

\[ \begin{array}{c}
\text{Input} & \text{Output} \\
g = 0, \ gb = 1 & g = 1, \ gb = 0 \\
\text{upper} & \text{strong } 0 \\
a \rightarrow b & 0 \rightarrow \\
\text{lower} & \text{strong } 1 \\
a \rightarrow b & 1 \rightarrow \\
g = 1, \ gb = 0 \\
g = 1, \ gb = 0
\end{array} \]
Tristates

- Tristate buffer produces Z when not enabled

<table>
<thead>
<tr>
<th>EN</th>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Nonrestoring Tristate

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y

![Diagram of nonrestoring tristate circuit]
Tristate Inverter

- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output

\[ EN = 0 \]
\[ Y = 'Z' \]

\[ EN = 1 \]
\[ Y = \bar{A} \]
Multiplexers

- 2:1 multiplexer chooses between two inputs

<table>
<thead>
<tr>
<th>S</th>
<th>D1</th>
<th>D0</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
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</tr>
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<td>1</td>
<td>1</td>
<td>X</td>
<td>1</td>
</tr>
</tbody>
</table>
Gate-Level Mux Design

- \( Y = S D_1 + \bar{S} D_0 \) (too many transistors)
- How many transistors are needed?

![Diagram of gate-level mux design](image-url)
Transmission Gate Mux

- Nonrestoring mux uses two transmission gates
  - Only 4 transistors
Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing

- Noninverting multiplexer adds an inverter
4:1 Multiplexer

- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates
D Latch

- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*

![Diagram of D Latch]
D Latch Design

- Multiplexer chooses D or old Q
D Latch Operation

CLK = 1

CLK = 0

D

Q

Q

CLK

D

Q
D Flip-flop

- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. positive edge-triggered flip-flop, master-slave flip-flop
D Flip-flop Design

- Built from master and slave D latches
D Flip-flop Operation

CLK = 0

CLK = 1

CLK

D

Q
Race Condition

- Back-to-back flops can malfunction from clock skew
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*

![Race Condition Diagram]

- CLK1
  - D → Q1
- CLK2
  - Q1 → Q2

- CLK1
  - Waveform
- CLK2
  - Waveform
- Q1
  - Waveform
- Q2
  - Waveform
Nonoverlapping Clocks

- Nonoverlapping clocks can prevent races
  - As long as nonoverlap exceeds clock skew
  - Industry manages skew more carefully
Gate Layout

- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - $V_{DD}$ and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts
Example: Inverter

(a)

(b) Substrate T

Well Tap

V_{DD}

A Y

GND
Example: NAND3

- Horizontal n-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 $V_{DD}$ rail at top
- Metal1 GND rail at bottom
- $32 \lambda$ by $40 \lambda$
Stick Diagrams

- Stick diagrams help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

V_{DD} - A - Y - GND

V_{DD} - A - B - C - Y - GND

Legend:
- blue: metal1
- red: poly
- green: ndiff
- yellow: pdiff
- x: contact

1: Circuits & Layout

CMOS VLSI Design 4th Ed.
Wiring Tracks

- A wiring track is the space required for a wire
  - $4\lambda$ width, $4\lambda$ spacing from neighbor = $8\lambda$ pitch
- Transistors also consume one wiring track
Well spacing

- Wells must surround transistors by $6\lambda$
  - Implies $12\lambda$ between opposite transistor flavors
  - Leaves room for one wire track
Area Estimation

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in $\lambda$
Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

\[ Y = (A + B + C) \cdot D \]

\[ V_{DD} \]

\[ \text{GND} \]

6 tracks = 48

5 tracks = 40
Summary

- MOS Transistors are stack of gate, oxide, silicon
- Can be viewed as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Next lecture:
  - A simple MIPS Microprocessor
  - Reading: 1.7-1.12