6. Data Hazard (12 points)

Consider the following code segment, executed on a 5-stage pipelined processor, as discussed in class.

```
1 lw  $t1, 0($t0)
2 lw  $t2, 4($t0)
3 add $t3, $t1, $t2
4 sw  $t3, 12($t0)
5 lw  $t4, 8($t0)
6 add $t5, $t1, $t4
7 sw  $t5, 16($t0)
```

For (a) and (b), assume that you do not have any forwarding path.

(a) (2 points) Which one(s) will experience data hazards among (1) - (7)?

```
3, 4, 6, 7
```

(b) (2 points) In a, how long will it take to complete the execution of (1) - (7)?

```
(7-1) + 5 + \frac{2 \times 4}{5} = 19 \text{ cycles}
```

For (c) - (e), assume that you added the forwarding paths (from EX/MEM and MEM/WB stages).

(c) (2 points) Which one(s) will experience data hazards among (1) - (7)?

```
3, 6
```

(d) (2 points) How long will it take to complete the execution of (1) - (7)?

```
(7-1) + 5 + \frac{2 \times 1}{7} = 13 \text{ cycles}
```

```
\text{instr #3, 6}
```
(e) (4 points) Let's say a compiler can re-arrange the instructions such that it can reduce the number of execution cycles. Please provide the instruction sequence to minimize the number of execution cycles. How many cycles will it take to complete the execution of (1) - (7)?

1. No stalls

\[ \therefore \ (7-1) + 5 = 11 \text{ cycles} \]

2
3
4
5
6
7
7. Multiple Choice (10 points)

(a) (1 point) You have a virtually-indexed and virtually-tagged (VIVT) cache. Which of the following descriptors does not apply to VIVT?

A. Fast cache access than physically-indexed and physically-tagged cache
B. Homonym (the same virtual address maps to different physical addresses upon context switch)
C. Synonym (different virtual addresses map to the same physical address when data is shared by multiple processes)
D. Very common in commercial processors

(b) (1 point) You have the following cache. What type of cache is the L1 cache in the following diagram shows?

A. VIVT cache
B. VIPT cache
C. PIPT cache
D. PIVT cache

(c) (1 point) Which of the following is not true about CISC ISA?

A. The CISC ISA requires a more complex decoder than the RISC ISA.
B. The instruction length is variable in CISC ISA.
The code size based on CISC ISA is typically larger than RISC ISA for the same program described by a high-level programming language such as C/C++.

- Intel's x86 processors adopt CISC ISA.

(d) (1 point) For a given program described by a high-level program programming language such as C/C++, which one does not affect “average” CPI?

- Compiler
- ISA
- Processor Organization
- Transistor Speed

(e) (1 point) You have (1) direct mapped, (2) 2-way set-associative, (3) 4-way set-associative, and (4) fully-associative 8KB caches with the line size of 64 bytes. Which one will have the shortest access time (or hit time) in general?

- Direct mapped cache
- 2-way set-associative cache
- 4-way set-associative cache
- Fully-associative caches

(f) (1 point) You have a 16KB direct-mapped cache with the line size of 64 bytes. When you reduce the line size to 32 bytes, what happens? Please choose everything relevant.

- The access time (hit time) increases
- The number of sets increases
- The access time (hit time) decreases
- The number of sets decreases

(g) (1 point) You have (1) direct mapped, (2) 2-way set-associative, (3) 4-way set-associative, and (4) fully-associative 8KB caches with the line size of 64 bytes. Which one will give you the highest hit rate (or lowest miss rate) in general?

- Direct mapped cache
- 2-way set-associative
- 4-way set-associative
- Fully-associative

(h) (1 point) The hit time of your 32KB direct-mapped and 2-way set associative caches is 1.3ns and 2ns, respectively. The hit rate of your 32KB direct-mapped and 2-way set associative caches is 0.8 and 0.9, respectively. The miss penalty for both caches are 100 cycles. Choose all the correct statements

- The hit time of the direct-mapped cache in terms of processor cycles is the same as that of the 2-way set-associative cache assuming the cycle time of your processor is 1 GHz.
- The 2-way set-associative cache leads to lower average memory access time than the direct mapped cache in terms of processor cycles assuming the cycle time of your processor is 1 GHz.
- The hit time of the direct-mapped cache in terms of processor cycles is smaller than that of the 2-way set-associative cache assuming the cycle time of your processor is 750 MHz.
D. The 2-way set-associative cache leads to higher average memory access time than the direct mapped cache in terms of processor cycles assuming the cycle time of your processor is 750 MHz.

(i) (1 point) Please pick all the wrong statements for a computer supporting virtual memory.
A. The virtual address is generated by the CPU.
B. Multiple virtual addresses from different processes cannot point to the same physical address.
C. The virtual memory space can be the same as or larger than the physical memory space.
D. The virtual memory can provide some protection from malicious programs.

(j) (1 point) Please choose all the wrong statements assuming a typical 5-stage pipelined processor with a separate instruction and data memories (as shown in the textbook and lecture slides).
A. A structural hazard can happen.
B. A data hazard can be completely eliminated by providing data forwarding from EX/MEM and MEM/WB stages.
C. A control hazard always happens when there is a conditional branch.
D. Although the processor does not have any forwarding path the compiler can resolve the data hazards.

I gave the full point to all the students for this problem as I found some issues.