Peak Detector using the LM358

Outline

Very often you will find yourself in need of a way to retain the maximum value of a time-varying voltage signal. This need often arises when you need to monitor a time-varying signal for a transient (short-lived) event. The peak detector can be periodically cleared so that it can return to monitoring the signal for another event. This module will guide you through the procedure of using an LM358 operational amplifier (Op Amp) as a peak detector.

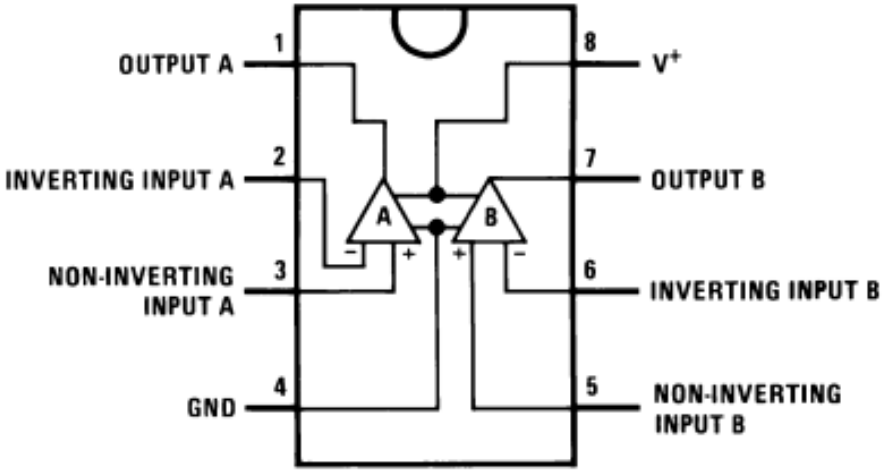

***Figure 1**: Pin configuration and Functions of the LM 358 Op Amp. Source: Figure 5.1 of datasheet*

Figure 1 shows the pin configuration of the LM 358 Op Amp. Although the power supply labels (at pins 4 and 8) suggest the chip should be powered by a single power supply, the data sheet reveals that it could be powered by a dual-supply configuration such as where a second battery would allow us to apply $-9\ V$ to pin 4 and $+9\ V$ to pin 8. This would allow us to operate "above and below" our nominal ground reference. It could also allow us to alter the peak detector to monitor for a large "negative" voltage. Note that there are two Op Amps contained in each IC.

Notes:

Learning Objectives

- To interpret critical information from the LM358 datasheet.
- To use node-voltage analysis to analyze an operational amplifier circuit.
- To build peak detector based on the LM358 operational amplifier.

Prerequisites

- Experience with ICs and schematic-to-breadboard circuit builds.
- Experience from lab with use of the function generator including adjustment for “high-Z” mode.

Parts Needed

- (1) LM358 Operational Amplifier (there are 2 per IC)
- (1) signal diode
- (1) $2.2\ k\Omega$ resistor
- (1) $100\ k\Omega$ resistor
- (1) $1000\ \mu F$ capacitor
- (1) nMOS transistor

Resources

Datasheet: https://www.ti.com/lit/ds/symlink/lm258-n.pdf?HQS=dis-mous-null-mousermode-dsf-pf-null-wwe&ts=1680032684902&ref_url=https%253A%252F%252Fwww.mouser.co.il%252F

Tutorial at All About Circuits: https://www.allaboutcircuits.com/video-tutorials/the-basic-op-amp-inverting-amplifier/

Notes:

Short Op Amp Tutorial

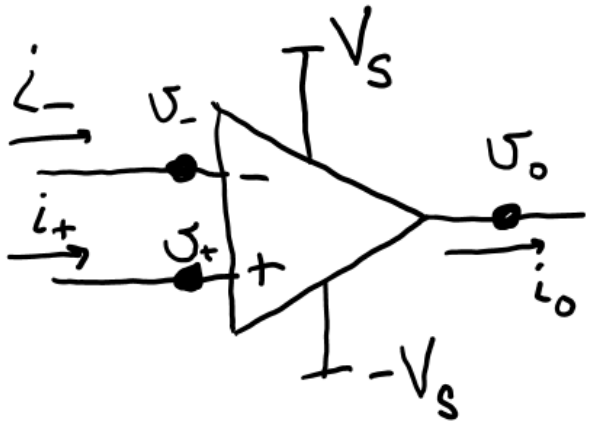

***Figure 2**: One circuit schematic diagram of the Op Amp that explicitly shows the power supply configuration.*

The Op Amp (see Figure 2) is an interesting device. It is designed to amplify the difference between *node voltages* v_+ and v_-, the voltages as the non-inverting and inverting input terminals. Mathematically, $v_o = A(v_+ - v_-)$. But not just a little amplification, a *LOT* of amplification. The amplification value, or so-called *open-loop gain*, A, is super large, $A \approx 100{,}000$. But since the power supply is too modest to support enormous voltages, the Op Amp would most likely ***not*** be able to do this. The output v_o would merely reach something close to the supplied power and stop. Instead, external circuitry is added to control the amplifying nature of the Op Amp and place the amplification within reasonable bounds. What you really need to know as a designer is how to **model** the Op Amp behavior **such that your analysis is suitably accurate**. Here, in simple terms, is what you need to know:

- The voltages at the two input nodes differ only by very tiny amounts (when the connections to the leads provide linear negative feedback as it does in many basic op amp circuits). In fact, you can **assume that $\boldsymbol{v_- = v_+}$** when you apply nodal analysis to the circuit.
- The input resistance as you look into the inverting and noninverting terminals is very large. So large, in fact, that you can **assume that $\boldsymbol{i_- = 0\ amps}$ and $\boldsymbol{i_+ = 0\ amps}$** when you apply nodal analysis to the circuit.

Node-voltage analysis is commonly used to evaluate Op Amp circuits.

Notes:

Let's summarize: You will likely apply node-voltage analysis to solve an Op Amp circuit's behavior and to do so you will use the Op Amp approximations in the following box.

Op Amp Approximations:

$$v_- = v_+$$

$$i_- = 0\ amps$$

$$i_+ = 0\ amps$$

Let's also make sure you understand the situation on the power rails. We will be using a dual-supply system, meaning it will take two voltage supplies to generate the $+V_S$ and the $-V_S$ voltages. Notice in Figure 3, that this means the negative terminal of the "upper" voltage supply needs to connect to the positive terminal of the "lower" voltage supply. We recommend that you **use orange wires to represent (connect to) the $-V_S$ power rail**. This may prevent you from making the mistake of thinking it is also connected to the red power rail. Shorting those two rails together would cause a total of $18\ V$ to be shorted! Please take your time, check your circuit, and be careful!

Notes:

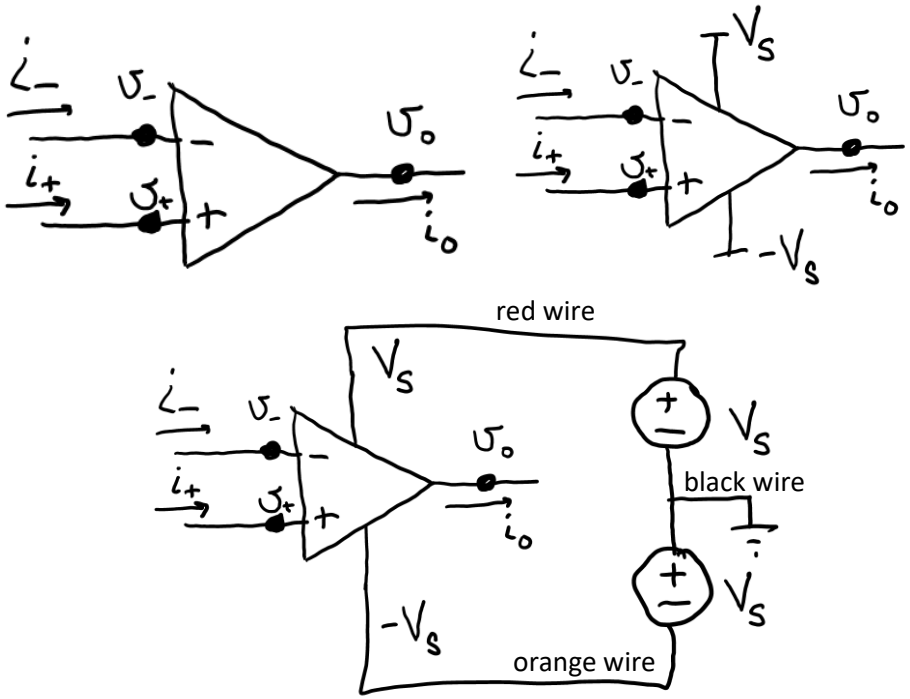

***Figure 3**: Three schematics of an Op Amp with dual-supply configuration. Clockwise from top-left: power supplies not shown; power rails shown; power rails explicitly showing the power supply configuration necessary.*

Notes:

A Family of Detectors

The peak detector might be seen as one circuit in a family of circuits designed to detect features of a time-varying signal. See Figure 4.

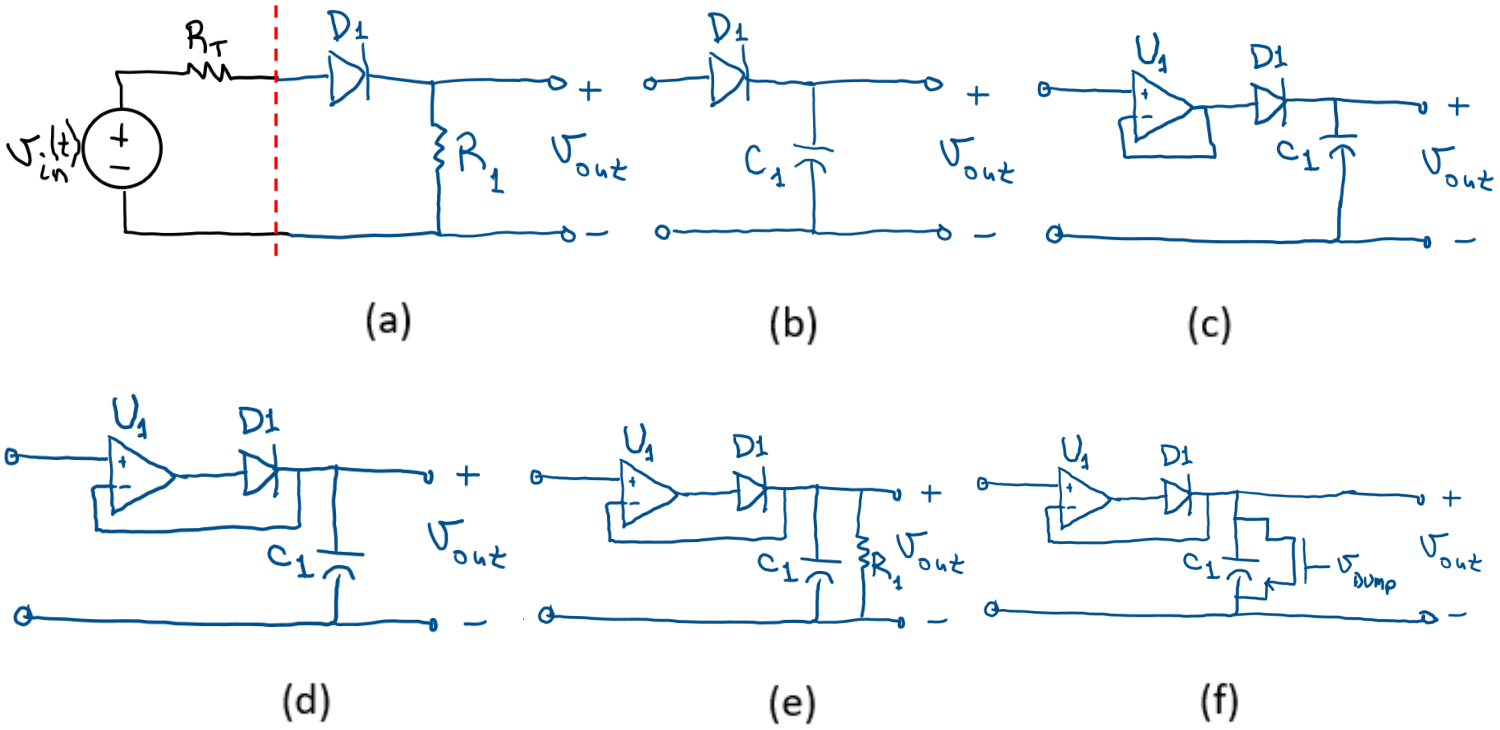

***Figure 4**: A "family" of detection-style circuits.*

In Figure 4 (a), we show the signal source as an ideal time-varying voltage signal $v_{in}(t)$ along with its Thevenin-equivalent resistance R_T. This Thevenin-modeled input is attached to a half-wave rectifier. Assuming the diode's turn-on voltage is $0\ V$ and $R_1 \gg R_T$, the output voltage $v_{out}(t)$ will imitate the input voltage $v_{in}(t)$ while $v_{in}(t) \geq 0$. For values of $v_{in}(t) < 0, v_{out}(t) = 0$. In Figure 4 (b) (for simplicity, we have stopped drawing the input's Thevenin circuit), the replacement of the resistor with a capacitor results in values of $v_{in}(t) > 0$ contributing charge to the capacitor to the highest voltage v_{in} attains (minus the actual turn-on voltage of the diode, of course). Since the charge of the capacitor has no path to dissipate, the capacitor can only accumulate charge over time. In this way, the capacitor becomes a record for the maximum value $v_{in}(t)$ has attained.

Notes:

Figure 4 (c) is identical to (b) in operation. This is because the configuration of the Op Amp makes it a "voltage follower," that is, the voltage at the output of the Op Amp is identical to $v_{in}(t)$. ICs like Op Amps are typically labeled with a "U" just as resistors are typically labeled with an "R"; I don't know why. Analysis of the voltage follower will be investigated in this procedure soon.

In Figure 4 (d), we have what may be the most-common example of a peak detector. In this figure, we have slightly shifted the location of the diode resulting in a situation where the amplifier compensates for non-zero diode turn-on voltages! That analysis will also be investigated soon.

In Figure 4 (e), the addition of a resistor provides a path for the capacitor to discharge. That is, while $v_{in}(t) > 0$ is charging the capacitor (quickly), a wise choice for the resistor R_1 could allow it to slowly discharge. Such a change is valuable if you want a peak detector that slowly, but automatically forgets a prior peak value so that it can detect a new peak again. Finally, Figure 4 (f) provides a peak detector where another signal v_{DUMP} provides a voltage to an n-channel enhancement-style MOSFET (nMOS) at a specific time when the capacitor is to drop its peak-detected charge and start tracking the peak voltage again.

Voltage Follower (Buffer)

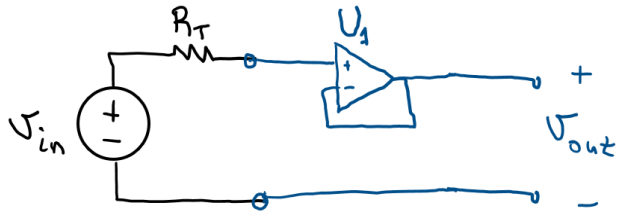

***Figure 5**: Use Op Amp approximations to analyze the relationship between v_{out} and v_{in}.*

Question 1: Given that we are using the HP 33120A function generator on our benchtop to test our circuits, what is the value of the function generator's Thevenin resistance R_T?

Notes:

Question 2: Use your Op Amp approximations to find these values of the voltage follower of Figure 5 (explain):

$i_+ =$
$i_- =$
$v_+ =$
$v_- =$

Question 3: Use your equations from Question 2 to explicitly prove that $v_{out} = v_{in}$ for the voltage follower. Explain every new step.

Let's try out our analysis on a real Op Amp circuit. Build the voltage follower of Figure 5 using the function generator as the source of the input. Configure the function generator to provide $v_{in}(t) = 3 \sin(0.2\pi t)$. That is, make it a sinusoidal signal with a peak-to-peak amplitude of $6\ V$ and a frequency of $1\ Hz$. For the Op Amp, power it with the benchtop voltage supply set to $+9\ V$ and $-9\ V$. You will also need the ground of the voltage supply connected to your circuit to provide the signal reference for your signals (like $v_{in}(t)$ and $v_{out}(t)$).

Question 4: Use your oscilloscope to view $v_{in}(t)$ and $v_{out}(t)$. Does $v_{in} = v_{out}$? Describe any differences you may see.

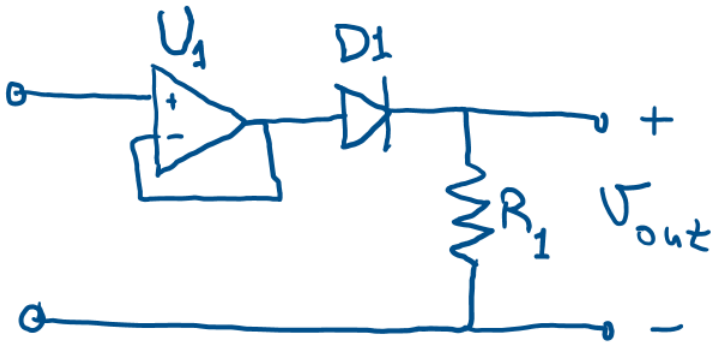

***Figure 6**: You will build this and describe what it does.*

Modify your circuit by adding a signal diode and a $100\ k\Omega$ resistor as in Figure 6. Again, use the oscilloscope to observe $v_{in}(t)$ and $v_{out}(t)$.

Question 5: Plot $v_{in}(t)$ and $v_{out}(t)$ and use the graph to explain what the circuit of Figure 6 does.

Notes:

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Build a Peak Detector

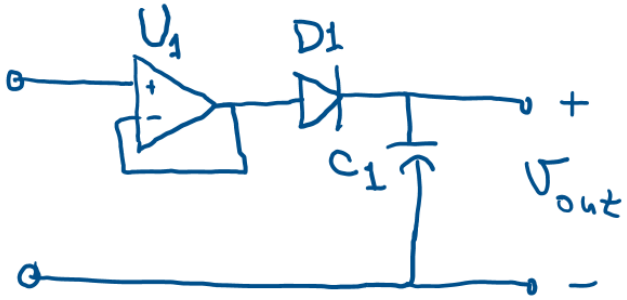

***Figure 7**: This is Figure 4 (c) repeated for your convenience.*

Modify your circuit by replacing the resistor with a $1000\ \mu F$ capacitor as in Figure 4 (c). Again, use the oscilloscope to observe $v_{in}(t)$ and $v_{out}(t)$. Increase the peak-to-peak amplitude of v_{in} to $10\ V$ while watching the oscilloscope.

Question 6: Explain what the circuit of Figure 4 (c) does.

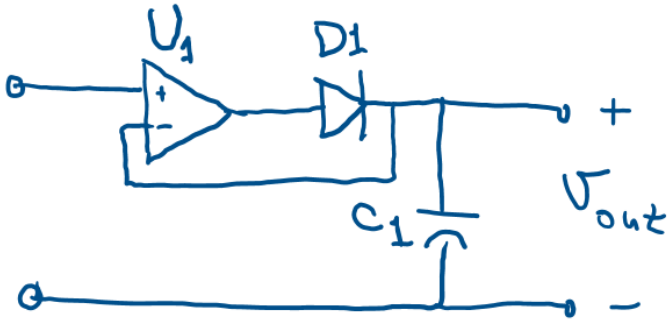

***Figure 8**: This is Figure 4 (d) repeated for your convenience.*

Modify your circuit by moving the diode "inside" the feedback path as in Figure 4 (d). Again, use the oscilloscope to observe $v_{in}(t)$ and $v_{out}(t)$.

Question 7: Explain what has changed between Figure 4 (c) and Figure 4 (d).

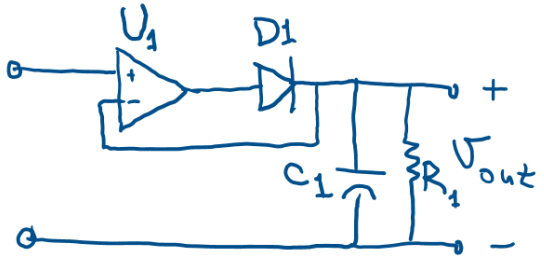

***Figure 9**: This is Figure 4 (e) repeated for your convenience.*

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Modify your circuit by placing a $2.2\ k\Omega$ resistor in parallel with the $1000\ \mu F$ capacitor as in Figure 4 (e). Again, use the oscilloscope to observe $v_{in}(t)$ and $v_{out}(t)$. Decrease the frequency of v_{in} as needed.

Question 8: Plot $v_{in}(t)$ and $v_{out}(t)$ and use the graph to explain what the circuit of Figure 4 (e) does. Be sure to discuss any RC time constants as appropriate.

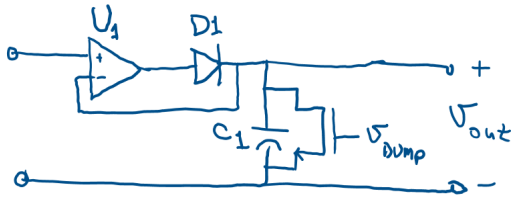

***Figure 10**: This is Figure 4 (f) repeated for your convenience.*

Modify your circuit by replacing the resistor with a MOSFET i as in Figure 4 (f). Again, use the oscilloscope to observe $v_{in}(t)$ and $v_{out}(t)$. Trigger the gate of the nMOS using a button-and-resistor design as you used in a previous lab.

Question 9: Plot $v_{in}(t)$ and $v_{out}(t)$ and use the graph to explain what the circuit of Figure 4 (f) does.