Circuits

Lecture 11
Uniform Circuit Complexity
Recall
Recall

- Non-uniform complexity
Recall

- Non-uniform complexity
- $P/1 \not\subseteq$ Decidable
Recall

- Non-uniform complexity
  - $P/1 \not\subseteq$ Decidable
  - $NP \subseteq P/log \Rightarrow NP = P$
Recall

- Non-uniform complexity
  - $P/1 \not\subseteq \text{Decidable}$
  - $NP \subseteq P/\log \implies NP = P$
  - $NP \subseteq P/poly \implies PH = \Sigma_2^P$
Recall

- Non-uniform complexity
  - $\mathsf{P}/1 \not\subseteq \mathsf{Decidable}$
  - $\mathsf{NP} \subseteq \mathsf{P/log} \Rightarrow \mathsf{NP} = \mathsf{P}$
  - $\mathsf{NP} \subseteq \mathsf{P/poly} \Rightarrow \mathsf{PH} = \Sigma_2^\mathsf{P}$
- Circuit Complexity
Recall

- Non-uniform complexity
  - $\text{P/1} \not\subseteq \text{Decidable}$
  - $\text{NP} \subseteq \text{P/log} \Rightarrow \text{NP} = \text{P}$
  - $\text{NP} \subseteq \text{P/poly} \Rightarrow \text{PH} = \Sigma_2^P$

- Circuit Complexity
  - $\text{SIZE}(\text{poly}) = \text{P/poly}$
Recall

Non-uniform complexity

- \( P/1 \notin \text{Decidable} \)
- \( \text{NP} \subseteq P/\log \implies \text{NP} = P \)
- \( \text{NP} \subseteq P/\text{poly} \implies \text{PH} = \Sigma_2^P \)

Circuit Complexity

- \( \text{SIZE}(\text{poly}) = P/\text{poly} \)
- \( \text{SIZE-} \text{-hierarchy} \)
Recall

- **Non-uniform complexity**
  - \( P/1 \nsubseteq Decidable \)
  - \( NP \subseteq P/log \Rightarrow NP = P \)
  - \( NP \subseteq P/poly \Rightarrow PH = \Sigma_2^P \)

- **Circuit Complexity**
  - \( SIZE(poly) = P/poly \)
  - **SIZE-hierarchy**
    - \( SIZE(T') \nsubseteq SIZE(T) \) if \( T = \Omega(t2^t) \) and \( T' = O(2^t/t) \)
Recall

- Non-uniform complexity
  - \( P/1 \not\subseteq \text{Decidable} \)
  - \( \text{NP} \subseteq P/\log \implies \text{NP} = P \)
  - \( \text{NP} \subseteq P/poly \implies \text{PH} = \Sigma_2^P \)

- Circuit Complexity
  - \( \text{SIZE}(\text{poly}) = P/poly \)
  - \( \text{SIZE}-\text{hierarchy} \)
    - \( \text{SIZE}(T') \not\subseteq \text{SIZE}(T) \) if \( T=\Omega(t2^t) \) and \( T'=O(2^t/t) \)
    - Most functions on \( t \) bits (that ignore last \( n-t \) bits) are in \( \text{SIZE}(T) \) but not in \( \text{SIZE}(T') \)
Uniform Circuits
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Uniform circuit family: constructed by a TM
Uniform Circuits

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- Undecidable languages are undecidable for these circuits families
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- Can relate their complexity classes to classes defined using TMs
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- Logspace-uniform:
Uniform Circuits

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- Logspace-uniform:
  - An $O(\log n)$ space TM can compute the circuit
$NC^i$ and $AC^i$
$\text{NC}^i$ and $\text{AC}^i$

$\text{NC}^i$: class of languages decided by bounded fan-in logspace-uniform circuits of polynomial size and depth $O(\log^i n)$
$\text{NC}^i$ and $\text{AC}^i$

$\text{NC}^i$: class of languages decided by bounded fan-in logspace-uniform circuits of polynomial size and depth $O(\log^i n)$

$\text{AC}^i$: Similar, but unbounded fan-in circuits
NC\textsuperscript{i} and AC\textsuperscript{i}

\begin{itemize}
  \item NC\textsuperscript{i}: class of languages decided by bounded fan-in logspace-uniform circuits of \textit{polynomial size and depth} \(O(\log^i n)\)
  \item AC\textsuperscript{i}: Similar, but unbounded fan-in circuits
  \item NC\textsuperscript{0} and AC\textsuperscript{0}: constant depth circuits
\end{itemize}
NC$^i$ and AC$^i$

- **NC$^i$**: class of languages decided by bounded fan-in logspace-uniform circuits of polynomial size and depth $O(\log^i n)$
  - **AC$^i$**: Similar, but unbounded fan-in circuits

- **NC$^0$ and AC$^0$**: constant depth circuits
  - **NC$^0$** output depends on only a constant number of input bits
NC$^i$ and AC$^i$

- **NC$^i$**: class of languages decided by bounded fan-in logspace-uniform circuits of polynomial size and depth $O(\log^i n)$
- **AC$^i$**: Similar, but unbounded fan-in circuits
- **NC$^0$ and AC$^0$**: constant depth circuits
  - NC$^0$ output depends on only a constant number of input bits
  - NC$^0 \subsetneq AC^0$: Consider $L = \{1,11,111,\ldots\}$
NC and AC
NC and AC

$NC = \bigcup_{i>0} NC^i$. Similarly AC.
NC and AC

\[ NC = \bigcup_{i>0} NC^i. \text{ Similarly AC.} \]

\[ NC^i \subseteq AC^i \subseteq NC^{i+1} \]
NC and AC

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- Clearly \( NC^i \subseteq AC^i \)
NC and AC

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Clearly \( NC^i \subseteq AC^i \)

\( AC^i \subseteq NC^{i+1} \) because polynomial fan-in can be reduced to constant fan-in by using a log depth tree.
NC and AC

\[ \text{NC} = \bigcup_{i>0} \text{NC}_i. \text{ Similarly AC.} \]

\[ \text{NC}_i \subseteq \text{AC}_i \subseteq \text{NC}_{i+1} \]

Clearly \[ \text{NC}_i \subseteq \text{AC}_i \]

\[ \text{AC}_i \subseteq \text{NC}_{i+1} \text{ because polynomial fan-in can be reduced to constant fan-in by using a log depth tree} \]

So \[ \text{NC} = \text{AC} \]
NC \subseteq P
NC \subseteq \mathcal{P}

Generate circuit of the right input size and evaluate on input
$\text{NC} \subseteq \text{P}$

- Generate circuit of the right input size and evaluate on input
- Generating the circuit
\[ \text{NC} \subseteq \text{P} \]

- Generate circuit of the right input size and evaluate on input
- Generating the circuit
  - in logspace, so poly time; also circuit size is poly
NC ⊆ P

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- Evaluating the gates
\[ \text{NC} \subseteq \text{P} \]

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  - Poly(n) gates
\textbf{NC} \subseteq \textit{P}

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- Evaluating the gates
  - Poly(n) gates

  - Per gate takes $O(1)$ time + time to look up output values of (already evaluated) gates
NC ⊆ P

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  - Generating the circuit
    - in logspace, so poly time; also circuit size is poly
  - Evaluating the gates
    - Poly(n) gates
    - Per gate takes $O(1)$ time + time to look up output values of (already evaluated) gates
- Open problem: Is NC = P?
Motivation for NC
Motivation for NC

Fast parallel computation is (loosely) modeled as having poly many processors and taking poly-log time
Motivation for NC

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- Corresponds to NC (How?)
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- Corresponds to NC (How?)
- Depth translates to time
- Total “work” is size of the circuit
An example
An example

 PARITY in NC¹
An example

- **PARITY in NC¹**

- **PARITY = \{ x \mid x \text{ has odd number of 1s} \}**
An example

- PARITY in $\mathsf{NC}^1$

- PARITY = \{ $x$ | $x$ has odd number of 1s \}

- Circuit should evaluate $x_1 \oplus x_2 \oplus \ldots \oplus x_n$
An example

PARITY in $\text{NC}^1$

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- Circuit should evaluate $x_1 \oplus x_2 \oplus ... \oplus x_n$
- Tree of $n-1$ XOR gates: log $n$ deep
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- Each XOR gate implemented in depth 3
An example

PARITY in NC¹

PARITY = { x | x has odd number of 1s }

Circuit should evaluate $x_1 \oplus x_2 \oplus \ldots \oplus x_n$

Tree of $n-1$ XOR gates: log $n$ deep

Each XOR gate implemented in depth 3
Another example
Another example

PATH ∈ AC¹
Another example

- $\text{PATH} \in \text{AC}^1$
- “Boolean” Matrix Multiplication
Another example

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- "Boolean" Matrix Multiplication

- $Z = XY$: $z_{ij} = \bigvee_{k=1..n} (x_{ik} \land y_{kj})$
Another example

PATH $\in \text{AC}^1$

"Boolean" Matrix Multiplication

$Z = XY$: $z_{ij} = \lor_{k=1..n} (x_{ik} \land y_{kj})$

$\text{AC}^0$ circuit (OR gate with fan-in n, AND gates)
Another example

PATH $\in \text{AC}^1$

"Boolean" Matrix Multiplication

$Z = XY$: $z_{ij} = \lor_{k=1..n} (x_{ik} \land y_{kj})$

$\text{AC}^0$ circuit (OR gate with fan-in n, AND gates)

If $X$ adjacency matrix (with self-loops), $X^t_{ij} = 1$ iff path from $i$ to $j$ of length $t$ or less
Another example

PATH ∈ AC^1

“Boolean” Matrix Multiplication

Z = XY: z_{ij} = \bigvee_{k=1..n} (x_{ik} \land y_{kj})

AC^0 circuit (OR gate with fan-in n, AND gates)

If X adjacency matrix (with self-loops), X^t_{ij}=1 iff path from i to j of length t or less

X^m_{ij} for m ≥ n is the transitive closure
Another example

PATH ∈ AC$^1$

“Boolean” Matrix Multiplication

$Z = XY$: $z_{ij} = \bigvee_{k=1}^{n} (x_{ik} \land y_{kj})$

AC$^0$ circuit (OR gate with fan-in n, AND gates)

If X adjacency matrix (with self-loops), $X^t_{ij} = 1$ iff path from i to j of length t or less

$X^m_{ij}$ for $m \geq n$ is the transitive closure

$O(\log n)$ matrix multiplications to compute $X^n_{ij}$
Another example

PATH ∈ AC¹

“Boolean” Matrix Multiplication
Z = XY: \( z_{ij} = \bigvee_{k=1..n} (x_{ik} \land y_{kj}) \)
AC⁰ circuit (OR gate with fan-in n, AND gates)

If X adjacency matrix (with self-loops), \( X^t_{ij} = 1 \) iff path from i to j of length t or less
Xₘᵢⱼ for \( m \geq n \) is the transitive closure
O(log n) matrix multiplications to compute \( X^n_{ij} \)
Total depth O(log n)
$\mathsf{NC}^1 \subseteq \mathsf{L}$
\( \text{NC}^1 \subseteq L \)

Generate circuit (implicitly) and evaluate
$\text{NC}^1 \subseteq \text{L}$

- Generate circuit (implicitly) and evaluate
- cf. $\text{NC} \subseteq \text{P}$. But now, to conserve space, a recursive evaluation (rather than bottom-up).
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- cf. $\text{NC} \subseteq \text{P}$. But now, to conserve space, a recursive evaluation (rather than bottom-up).
- For each gate, recursively evaluate each input wire
\[ \text{NC}^1 \subseteq \text{L} \]

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- cf. NC \( \subseteq \) P. But now, to conserve space, a recursive evaluation (rather than bottom-up).

- For each gate, recursively evaluate each input wire

- Storage: A path to the current node, from the output node: since bounded fan-in, takes \( O(1) \) bits per node; since logspace uniform that is sufficient to compute the node id in logspace
\( \text{NC}^1 \subseteq \text{L} \)

- Generate circuit (implicitly) and evaluate
- cf. \( \text{NC} \subseteq \text{P} \). But now, to conserve space, a recursive evaluation (rather than bottom-up).
- For each gate, recursively evaluate each input wire
  - Storage: A path to the current node, from the output node: since bounded fan-in, takes \( O(1) \) bits per node; since logspace uniform that is sufficient to compute the node id in logspace
  - And at each node along the path, the input wire values evaluated results so far (again \( O(1) \) bits per node)
\textbf{NC}^1 \subseteq L

- Generate circuit (implicitly) and evaluate

- cf. NC \subseteq P. But now, to conserve space, a recursive evaluation (rather than bottom-up).

- For each gate, recursively evaluate each input wire

- Storage: A path to the current node, from the output node: since bounded fan-in, takes \(O(1)\) bits per node; since logspace uniform that is sufficient to compute the node id in logspace

- And at each node along the path, the input wire values evaluated results so far (again \(O(1)\) bits per node)

- Length of path = depth of circuit = \(O(\log n)\)
\( \text{NL} \subseteq \text{AC}^1 \)
NL \subseteq AC^1

\footnotesize{Recall \ PATH \in AC^1}
\[ \text{NL} \subseteq \text{AC}^1 \]

Recall \( \text{PATH} \in \text{AC}^1 \)

Also recall \( \text{PATH} \) is NL-complete
\[ \text{NL} \subseteq \text{AC}^1 \]

- Recall \( \text{PATH} \in \text{AC}^1 \)
- Also recall \( \text{PATH} \) is NL-complete
  - with respect to log-space reductions
\textbf{NL} \subseteq \textbf{AC}^1

- Recall \text{PATH} \in \text{AC}^1
- Also recall \text{PATH} is NL-complete
  - with respect to log-space reductions
  - in fact, with respect to NC^1 reductions
Recall \( \text{PATH} \in \text{AC}^1 \)

Also recall \( \text{PATH} \) is NL-complete

with respect to log-space reductions

in fact, with respect to NC\(^1\) reductions

Exercise! (For NL machine \( M \), can build (in log-space) NC\(^1\) circuit which on input \( x \), outputs \((i,j)^{th}\) entry of the adjacency matrix of configuration graph of \( M(x) \).)
Recall $\text{PATH} \in \text{AC}^1$

Also recall $\text{PATH}$ is NL-complete

with respect to log-space reductions

in fact, with respect to $\text{NC}^1$ reductions

Exercise! (For NL machine $M$, can build (in log-space) $\text{NC}^1$ circuit which on input $x$, outputs $(i,j)^{th}$ entry of the adjacency matrix of configuration graph of $M(x)$.)

Combining the $\text{NC}^1$ circuits for reduction and the $\text{AC}^1$ circuit for $\text{PATH}$, we get an $\text{AC}^1$ circuit
Summary: NC$^i$ and AC$^i$
Summary: \( \text{NC}^i \) and \( \text{AC}^i \)

\[
\text{NC}^i \subseteq \text{AC}^i \subseteq \text{NC}^{i+1} \subseteq \text{NC} = \text{AC} \subseteq P
\]
Summary: $NC^i$ and $AC^i$

- $NC^i \subseteq AC^i \subseteq NC^{i+1} \subseteq NC = AC \subseteq P$
- $NC^0 \subsetneq AC^0 \subsetneq NC^1 \subseteq L \subseteq NL \subseteq AC^1$
Summary: $\text{NC}^i$ and $\text{AC}^i$

- $\text{NC}^i \subseteq \text{AC}^i \subseteq \text{NC}^{i+1} \subseteq \text{NC} = \text{AC} \subseteq \text{P}$
- $\text{NC}^0 \not\subseteq \text{AC}^0 \not\subseteq \text{NC}^1 \subseteq \text{L} \subseteq \text{NL} \subseteq \text{AC}^1$
- $\text{AC}^0 \not\subseteq \text{NC}^1$ as $\text{PARITY} \not\in \text{AC}^0$ (later)
Summary: $\text{NC}^i$ and $\text{AC}^i$

- $\text{NC}^i \subseteq \text{AC}^i \subseteq \text{NC}^{i+1} \subseteq \text{NC} = \text{AC} \subseteq \text{P}$
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- $\text{AC}^0 \subsetneq \text{NC}^1$ as $\text{PARITY} \notin \text{AC}^0$ (later)
- Open: whether $\text{NC}^i \subsetneq \text{AC}^i \subsetneq \text{NC}^{i+1}$ for larger $i$
Summary: $\text{NC}^i$ and $\text{AC}^i$

- $\text{NC}^i \subseteq \text{AC}^i \subseteq \text{NC}^{i+1} \subseteq \text{NC} = \text{AC} \subseteq \text{P}$
- $\text{NC}^0 \subsetneq \text{AC}^0 \subsetneq \text{NC}^1 \subseteq L \subseteq \text{NL} \subseteq \text{AC}^1$
- $\text{AC}^0 \subsetneq \text{NC}^1$ as $\text{PARITY} \notin \text{AC}^0$ (later)

Open: whether $\text{NC}^i \subsetneq \text{AC}^i \subsetneq \text{NC}^{i+1}$ for larger $i$

Open: Is $\text{NC} = \text{P}$? (Can all polynomial time decidable languages be sped up to poly-log time using parallelization?)
DC Uniform
DC Uniform

Recall Uniform circuit family: circuits in the family can be generated by a TM
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Suppose circuits are super-polynomially large. Cannot be logspace-uniform or P-uniform.
DC Uniform

- Recall Uniform circuit family: circuits in the family can be generated by a TM.
- Suppose circuits are super-polynomially large. Cannot be logspace-uniform or P-uniform.
- DC uniform allows exponentially large circuits.
DC Uniform

- Recall Uniform circuit family: circuits in the family can be generated by a TM.
- Suppose circuits are super-polynomially large. Cannot be logspace-uniform or P-uniform.
- DC uniform allows exponentially large circuits.
- Still requires polynomial time implicit computation of the circuit.
Recall Uniform circuit family: circuits in the family can be generated by a TM

Suppose circuits are super-polynomially large. Cannot be logspace-uniform or P-uniform.

DC uniform allows exponentially large circuits

Still requires polynomial time implicit computation of the circuit

Coincides with EXP (Why?)
$O(1)$ depth DC Uniform
O(1) depth DC Uniform

Restricted to depth $k$, $2^{\text{poly}(n)}$ size, unbounded fan-in
DC uniform circuit families decide exactly languages
in $\Sigma_k^P \cup \Pi_k^P$
Restricted to depth $k$, $2^{\text{poly}(n)}$ size, unbounded fan-in DC uniform circuit families decide exactly languages in $\Sigma_k^P \cup \Pi_k^P$

Given a DC uniform circuit (w.l.o.g alternating levels of AND and OR gates, and NOT gates only at the input level) of depth $k$, an equivalent quantified expression with $k$ alternations
O(1) depth DC Uniform

Restricted to depth $k$, $2^{\text{poly}(n)}$ size, unbounded fan-in DC uniform circuit families decide exactly languages in $\Sigma_k^P \cup \Pi_k^P$

Given a DC uniform circuit (w.l.o.g alternating levels of AND and OR gates, and NOT gates only at the input level) of depth $k$, an equivalent quantified expression with $k$ alternations

Given a quantified expression with $k$ alternations, an equivalent DC uniform circuit of depth $k$
O(1) depth DC Uniform
O(1) depth DC Uniform

- From circuit to quantified expression
O(1) depth DC Uniform

- From circuit to quantified expression

- Consider game played on the circuit: adversary picks an edge going into the AND level and Alice picks an edge going into the OR level, going through levels top to bottom
O(1) depth DC Uniform

» From circuit to quantified expression

» Consider game played on the circuit: adversary picks an edge going into the AND level and Alice picks an edge going into the OR level, going through levels top to bottom

» Alice wins if adversary “breaks off the path” (by picking either a non-wire edge or a wire not continuing the path), or if the path terminates at literal of value 1 (w/o breaking)
O(1) depth DC Uniform

- From circuit to quantified expression

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- Alice wins if adversary “breaks off the path” (by picking either a non-wire edge or a wire not continuing the path), or if the path terminates at literal of value 1 (w/o breaking).

- Input accepted by the circuit iff Alice has a winning strategy (i.e., if the quantified expression is true).

Can check in poly time
O(1) depth DC Uniform

- From circuit to quantified expression

Consider game played on the circuit: adversary picks an edge going into the AND level and Alice picks an edge going into the OR level, going through levels top to bottom.

Alice wins if adversary “breaks off the path” (by picking either a non-wire edge or a wire not continuing the path), or if the path terminates at literal of value 1 (w/o breaking).

Input accepted by the circuit iff Alice has a winning strategy (i.e., if the quantified expression is true).

Each edge has a polynomially long label, and quantified variables take values from the same domain. Checking if edge is a correct wire in poly time (uniformity).
$O(1)$ depth DC Uniform
O(1) depth DC Uniform

From quantified expression to circuit:
O(1) depth DC Uniform

- From quantified expression to circuit:
  - Circuit has sub-circuits evaluating the poly-time condition for each possible assignment of the quantified variables.
From quantified expression to circuit:

Circuit has sub-circuits evaluating the poly-time condition for each possible assignment of the quantified variables.

Hang these sub-circuits at the leaves of a k-level AND-OR tree appropriately.
From quantified expression to circuit:

Circuit has sub-circuits evaluating the poly-time condition for each possible assignment of the quantified variables.

Hang these sub-circuits at the leaves of a k-level AND-OR tree appropriately.

Circuit can be implicitly computed in polynomial time. Size $2^{O(\text{total length of variables})}$
Today
Today

- $NC^i$ and $AC^i$
Today

- $NC^i$ and $AC^i$
- DC-uniform
Today

- NC\textsuperscript{i} and AC\textsuperscript{i}
- DC-uniform
- PH levels and EXP
Today

- $\text{NC}^i$ and $\text{AC}^i$
- DC-uniform
- PH levels and EXP
- Later, more circuits and non-uniform computation (time permitting)
Today

- $\text{NC}^i$ and $\text{AC}^i$
- $\text{DC}$-uniform
- PH levels and EXP
- Later, more circuits and non-uniform computation (time permitting)
- $\text{PARITY} \notin \text{AC}^0$
Today

- $\text{NC}^i$ and $\text{AC}^i$
- DC-uniform
- PH levels and EXP
- Later, more circuits and non-uniform computation (time permitting)
- PARITY $\notin \text{AC}^0$
- Decision trees, Branching programs
Today

- $\text{NC}^i$ and $\text{AC}^i$
- DC-uniform
- PH levels and EXP
- Later, more circuits and non-uniform computation (time permitting)
- PARITY $\not\in \text{AC}^0$
- Decision trees, Branching programs
- Connections between circuit lowerbounds and other complexity class separations