Chapter 3 – Instruction-Level Parallelism and its Exploitation (Part 4)

ILP vs. Parallel Computers
Dynamic Scheduling (Section 3.4, 3.5)
Dynamic Branch Prediction (Section 3.3)
Hardware Speculation and Precise Interrupts (Section 3.6)
Multiple Issue (Section 3.7)
Static Techniques (Section 3.2, Appendix H)
Limitations of ILP (Section 3.10)
Multithreading (Section 3.12)
Putting it Together (Miniprojects)
Limits of ILP

How much can ILP buy us?

Limits studies make optimistic assumptions to find the limit for ILP

But may miss impact of compiler, future advances

A highly optimistic study [Wall’93]

- Infinite number of physical registers (no register WAW, WAR)
- Infinite number of in-flight instructions
- Perfect branch prediction
- Perfect memory address alias analysis
- Single cycle FU
- Single cycle memory (perfect caches)
Limits of ILP (contd.)

(This and next four figures are from an old edition of the book)

<table>
<thead>
<tr>
<th>SPEC benchmarks</th>
<th>Instruction issues per cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>gcc</td>
<td>55</td>
</tr>
<tr>
<td>espresso</td>
<td>63</td>
</tr>
<tr>
<td>li</td>
<td>18</td>
</tr>
<tr>
<td>fpppp</td>
<td>75</td>
</tr>
<tr>
<td>doduc</td>
<td>119</td>
</tr>
<tr>
<td>tomcatv</td>
<td>150</td>
</tr>
</tbody>
</table>

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**Limits of ILP – Impact of Optimistic Assumptions**

Limiting Instruction window size

Finding dependences among n instr requires $n^2$ comparisons

2000 instructions implies 4 million comparisons!

Following use 2K window and 64 issue limit

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Limits of ILP – Impact of Optimistic Assumptions

Realistic branch prediction

No charge for mispredictions

Following use tournament predictor

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Limits of ILP – Impact of Optimistic Assumptions

Finite registers

Following uses 256 int and 256 fp for renaming

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Limits of ILP – Impact of Optimistic Assumptions

Imperfect memory alias analysis

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But Limits Studies may be Pessimistic!

For most optimistic study

WAR and WAW hazards through memory
Unnecessary dependences (e.g., loop iteration count)
Overcoming data flow limit – value prediction

For more realistic studies

Address value prediction and speculation
Speculating on multiple paths
Often superscalar instruction slots are wasted
Why not use them for other threads?

**Multithreading**

- Coarse-grained
- Fine-grained

Simultaneous multithreading (SMT) or hyperthreading

(Vs. multiprocessing)
Multithreading: Instruction + Thread Level Parallelism

Vs. Multiprocessing?
Impact of SMT: 1 vs. 4 threads for TPC-C

![Graph showing relative increase in miss rate or latency for different cache levels and latency categories.]
SMT Speedup & Energy Efficiency: 1 vs. 4 threads

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