Chapter 3 – Instruction-Level Parallelism and its Exploitation (Part 4)

ILP vs. Parallel Computers
Dynamic Scheduling (Section 3.4, 3.5)
Dynamic Branch Prediction (Section 3.3)
Hardware Speculation and PreciseInterrupts (Section 3.6)
Multiple Issue (Section 3.7)
Static Techniques (Section 3.2, Appendix H)
Limitations of ILP (Section 3.10)
Multithreading (Section 3.12)
Putting it Together (Mini-projects)
Limits of ILP

How much can ILP buy us?

Limit studies make optimistic assumptions to find the limit for ILP

But may miss impact of compiler, future advances

A highly optimistic study [Wall’93]

- Infinite number of physical registers (no register WAW, WAR)
- Infinite number of in-flight instructions
- Perfect branch prediction
- Perfect memory address alias analysis
- Single cycle FU
- Infinite number of FUs
- Single cycle memory (perfect caches)
**Limits of ILP (contd.)**

(This and next four figures are from an **old** edition of the book)

![Bar chart showing instruction issues per cycle for SPEC benchmarks](image)

- gcc: 55
- espresso: 63
- fpppp: 75
- duc: 119
- tomcatv: 150

© 2003 Elsevier Science (USA). All rights reserved.

* This figure has been taken from Computer Architecture, A Quantitative Approach, 3rd Edition Copyright 2003 by Elsevier Inc. All rights reserved. It has been used with permission by Elsevier Inc.
Limits of ILP – Impact of Optimistic Assumptions

Limiting Instruction window size

Finding dependences among n instr requires n^2 comparisons

2000 instructions implies 4 million comparisons!

Following use 2K window and 64 issue limit

* This figure has been taken from Computer Architecture, A Quantitative Approach, 3rd Edition Copyright 2003 by Elsevier Inc. All rights reserved. It has been used with permission by Elsevier Inc.
Limits of ILP – Impact of Optimistic Assumptions

Realistic branch prediction

No charge for mispredictions

Following use tournament predictor
Finite registers

Following uses 256 int and 256 fp for renaming
Limits of ILP – Impact of Optimistic Assumptions

Imperfect memory alias analysis

Instruction issues per cycle

© 2003 Elsevier Science (USA). All rights reserved.
But Limits Studies may be Pessimistic!

For most optimistic study

- WAR and WAW hazards through memory
- Unnecessary dependences (e.g., loop iteration count)
- Overcoming data flow limit – value prediction

For more realistic studies

- Address value prediction and speculation
- Speculating on multiple paths
Multithreading: Instruction + Thread Level Parallelism

Often superscalar instruction slots are wasted
Why not use them for other threads?

**Multithreading**
- Coarse-grained
- Fine-grained
- Simultaneous multithreading (SMT) or hyperthreading
  (Vs. multiprocessing)
Multithreading: Instruction + Thread Level Parallelism

Vs. Multiprocessing?
Impact of SMT: 1 vs. 4 threads for TPC-C

Relative increase in miss rate or latency

L1 I miss rate  L1 D miss rate  L2 miss rate  L1 I miss latency  L1 D miss latency  L2 miss latency

Copyright © 2011, Elsevier Inc. All rights Reserved.
SMT Speedup & Energy Efficiency: 1 vs. 4 threads