Limits of ILP

How much can ILP buy us?
Limit studies make optimistic assumptions to find the limit for ILP
But may miss impact of compiler, future advances
A highly optimistic study [Wall'93]
  Infinite number of physical registers (no register WAW, WAR)
  Infinite number of in-flight instructions
  Perfect branch prediction
  Perfect memory address alias analysis
  Single cycle FU
  Infinite number of FUs
  Single cycle memory (perfect caches)

Limits of ILP (contd.)

(This and next four figures are from an old edition of the book)

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Limits of ILP – Impact of Optimistic Assumptions

Limiting Instruction window size
Finding dependences among n instr requires n^2 comparisons
2000 instructions implies 4 million comparisons!
Following use 2K window and 64 issue limit

Limits of ILP – Impact of Optimistic Assumptions

Realistic branch prediction
No charge for mispredictions
Following use tournament predictor
**Limits of ILP – Impact of Optimistic Assumptions**

Finite registers

Following uses 256 int and 256 fp for renaming

**Limits of ILP – Impact of Optimistic Assumptions**

Imperfect memory alias analysis

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**But Limits Studies may be Pessimistic!**

For most optimistic study

- WAR and WAW hazards through memory
- Unnecessary dependences (e.g., loop iteration count)
- Overcoming data flow limit – value prediction

For more realistic studies

- Address value prediction and speculation
- Speculating on multiple paths

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**Multithreading: Instruction + Thread Level Parallelism**

Often superscalar instruction slots are wasted

Why not use them for other threads?

**Multithreading**

- Coarse-grained
- Fine-grained
- Simultaneous multithreading (SMT) or hyperthreading

(Vs. multiprocessing)
Multithreading: Instruction + Thread Level Parallelism

Impact of SMT: 1 vs. 4 threads for TPC-C

SMT Speedup & Energy Efficiency: 1 vs. 4 threads