Chapter 3 – Instruction-Level Parallelism and its Exploitation (Part 4)

ILP vs. Parallel Computers
Dynamic Scheduling (Section 3.4, 3.5)
Dynamic Branch Prediction (Section 3.3)
Hardware Speculation and Precise Interrupts (Section 3.6)
Multiple Issue (Section 3.7)
Static Techniques (Section 3.2, Appendix H)
Limitations of ILP (Section 3.10)
Multithreading (Section 3.12)
Putting it Together (Mini-projects)

Limits of ILP

How much can ILP buy us?
Limits studies make optimistic assumptions to find the limit for ILP
But may miss impact of compiler, future advances
A highly optimistic study [Wall’93]
Infinite number of physical registers (no register WAW, WAR)
Infinite number of in-flight instructions
Perfect branch prediction
Perfect memory address alias analysis
Single cycle FU
Single cycle memory (perfect caches)

Limits of ILP (contd.)

Finding dependences among n instr requires n^2 comparisons
2000 instructions implies 4 million comparisons!
Following use 2K window and 64 issue limit
Limits of ILP – Impact of Optimistic Assumptions

Realistic branch prediction
No charge for mispredictions
Following use tournament predictor

Limits of ILP – Impact of Optimistic Assumptions

Finite registers
Following uses 256 int and 256 fp for renaming

Limits of ILP – Impact of Optimistic Assumptions

Imperfect memory alias analysis

But Limits Studies may be Pessimistic!

For most optimistic study
WAR and WAW hazards through memory
Unnecessary dependences (e.g., loop iteration count)
Overcoming data flow limit – value prediction

For more realistic studies
Address value prediction and speculation
Speculating on multiple paths
**Multithreading: Instruction + Thread Level Parallelism**

Often superscalar instruction slots are wasted
Why not use them for other threads?

Multithreading
   - Coarse-grained
   - Fine-grained
   - Simultaneous multithreading (SMT) or hyperthreading
   (Vs. multiprocessing)

**Impact of SMT: 1 vs. 4 threads for TPC-C**

**SMT Speedup & Energy Efficiency: 1 vs. 4 threads**