Agenda

● Background and introduction
● The core and the pipeline
● Memory, cache and cache coherence
● Multicore and multithreading in the T5
● Server specific features, power management and other interesting properties
Background and introduction

● T-series designed by Oracle for use in servers
  ○ SPARC T5-2 SERVER
  ○ SPARC T5-4 SERVER
  ○ SPARC T5-8 SERVER
  ○ SPARC T5-1B SERVER MODULE

● Announced at Hot Chips Conference, August 2012
Key stats

- Low powered and powerful system-on-chip
- 16 SPARC S3 cores running at 3.6 GHz
- 8 threads per core => 128 threads
- 28 nm manufacturing process
- Implements the 64-bit SPARC V9 ISA
  - RISC instruction set
  - Big endian
The SPARC S3 core

- 8 threads
- Dual issue
- Out-of-order execution
- Dynamic threading
The pipelines

- 3 pipelines
- Different instructions
- E.g. integer or load-store
- First 14 steps shared
The pipeline - shared steps

- Fetch instruction(s) and select thread
- Select schedules thread if ready
  - Wait or Ready
  - LRU in Select
- Decode instructions
  - Up to two instructions per cycle
- Rename registers
  - Rename destination/source
  - Add instructions to Pick Queue
- Issue instructions to execution units
  - Schedule instructions from pick queue
- Hazards
The pipeline - execution

Several execution units

- Stream processing unit (SPU)
  - Cryptographic processing
- Floating point/graphics unit (FGU)
- Load-Store unit (LSU)
  - Processing and ordering mem.Refs.
  - Out-of-order
- Integer execution unit (EXU(0/1))
Memory Hierarchy

Distributed Shared Memory

- L1 and L2 caches are local to each core
- L3 cache is shared in a chip
- Uses directory to maintain coherence
- 1, 2, 3, 4, 6, and 8 socket configurations
Cache

L1
- Write-through
- 16KB cache for data and instruction each
- 4 way set associative
- Line size of 32B
- Hit latency of 5 cycles

L2
- MESI (Mod, Exclusive, Shared, Inv)
- 8 way set associative
- Write-back Cache of 128 KB
- Line size of 32B
- Set inclusive
- Hit latency of 18 cycles
Cache

L3

- MOESI (Modified, Owned, Exclusive, Shared, Invalid)
- 8 Address interleaved 1MB banks
- 16-way set Associative
- Line Size of 64B
- Shared by 16 cores via crossbar interconnect
- Miss buffer
- 51 hit cycle
L3 - Data Array

- 8 Address interleaved sub banks
- Only one array is activated during read or write
- Takes 2 cycles to retrieve the data
- Access to same data array need at least 2 cycles apart
Crossbar

- 8 by 9
- Connects L2 cache to L3 cache
- Each pair of cores share a crossbar port
- L3 Cache banks in the other side of the port
- The 9th port is connected to non-cacheable unit.
- Two virtual channels towards L3 (request and response)
- One virtual channel towards L2 (response data and snoop messages)
L3 Cache Coherence

- In a multi-socket system, the various L3 caches must be coherent
- This is accomplished using interconnects between chips
  - A 4 x 4 crossbar links cache coherence circuitry to 7 ports
  - Each port carries 12.8 Gb/s
- Topology varies with socket count
L3 Cache Coherence cont.

- A distributed directory points to which chip has a cache line
- Physical address bits [10:8] specify which chip carries that part of the directory
- Directory structure varies with number of chips
  - Two chips - 8192 indices 32 way set associative
  - Four chips - 4096 indices 64 way set associative
  - Eight chips - 2048 indices 128 way set associative
- L3 caches use a Modified, Owned, Exclusive, Shared, Invalid scheme
Memory

- Each chip has 4 memory controllers
- Each memory controller connects to up to 2 buffer chips
- Each buffer connects to up to 2 DIMMs
  - Uses 1066-MHz DDR3
  - Assuming the use of 32 GB DIMMs, one socket is connected to 512 GB of RAM
- Memory is managed by paging
  - Allows pages of size 2GB
Multicore/thread

- Each SPARC T5 chip has 16 Sparc S3 cores
- Each core can handle 8 threads
  - Threads are managed by a Least Recently Used algorithm
  - This allows up to 128 threads per chip
- Upto 8 chips can be linked directly without glue logic
  - This allows a server such as the 8 socket SPARC T5-8 SERVER
  - These sort of systems offer 1024 threads
I/O-Subsystem

- The non-cachable unit connected to the crossbar handles I/O
- I/O subsystem handles 2 lanes per socket
  - x8 PCIe 3.0
  - 8 GB/s in each direction per lane
- Expansion slots could handle non-volatile storage or GPUs
- Cards commonly handle networking
  - Ethernet
  - Infiniband
  - NUMA
Other Server Specific Features

- Each core has hardware acceleration of encryption operations
  - These support 16 different encryption algorithms
- Each core also has a random number generator
- Reliability, availability, and service features
  - Support for ECC memory
  - A cyclic redundancy code is used for inter-socket links
  - One processor can handle another one’s errors by interrupt rerouting
References


Timothy Prickett Morgan (4 September 2012), "Oracle hurls Sparc T5 gladiators into big-iron arena", www.theregister.co.uk, The Register

"Oracle's SPARC T5-2, SPARC T5-4, SPARC T5-8, and SPARC T5-1B Server Architecture, An Oracle White Paper" (PDF), www.oracle.com, Oracle Corporation, February 2014