1. Does the execution below satisfy causal consistency? ___Yes__________
   If you answer No, explain why.

2. Does the execution above satisfy sequential consistency? ___No__________
   If you answer No, explain why.

   No valid (legal) permutation of the operations exists. In fact, no such permutation for the operations of just the first two processes exists.

3. In the above execution, determine all the operations that happened-before operation op6.

   op5 – due to program order
   op1, op3 – due to read-from relation
4. What is the consensus number of the *atomic snapshot object*? _____1______
   
   Briefly explain why.

   Read/write registers can simulate atomic snapshot object

5. In a **synchronous** system, is it possible to use only read/write registers to achieve consensus despite crash failures? **Explain briefly.**

   Yes. Read/write registers can be used to simulate message passing, and then use message passing algorithm. Other solutions can be designed as well.

6. Considers processes p0 and p1. Suppose that message delay from p0 to p1 is in the range [10 ms, 20 ms], and the message delay from p1 to p0 is in the range [10 ms, 20 ms]. Given this information, what is the least possible worst case skew achievable? **Explain briefly.**

   Uncertainty is 10 ms in each direction. Hence \( u/2 = 5 \) ms skew in the worst-case.

7. **State true or false:**

   (a) When simulating a **multi-valued** single-reader single-write register using **binary** single-reader single-write registers, the reader must perform a low-level write when performing a high-level Read.  
   ____False__________

   (b) Consider processes p0 and p1. If the message delay between p0 and p1 (in each direction) is uniformly distributed in \([\text{d-u},\text{d}]\), then in every execution of any clock synchronization algorithm the skew must be at least \( u/2 \).  ____False__________