A Timed Reaction

Laboratory Outline

In this module, you will learn one method to create a timed reaction to an impulsive voltage from, say, the momentary press of a button. Often, we desire a circuit to respond to a sensor for a short period of time and then to "reset" and wait for the next event before responding again. Examples might include detection of knocks on a door by a vibration sensor or detection of claps by a microphone. A timed reaction can be accomplished by taking advantage of the time constant of an "RC" (resistor plus capacitor) circuit.

An RC circuit pairs a capacitor to be charged and/or discharged with a current-limiting resistor. Large-valued capacitors require a longer charging/discharging time due to higher charge capacity (hold more Q) and large-valued resistors restrict the current also increasing the charging/discharging time. It is not surprising that the time constant (a value related to the expected charge and discharge times) is directly proportional to the choice of both the capacitance, C, and the resistance, R.

$$\tau = RC$$

Prerequisites

- Practical experience placing an IC on a breadboard and reading a datasheet.
- Comfort using a Schmitt-trigger invertor as well as an nMOS transistor.

Parts Needed

- A fixed-voltage supply, nominally 9 volts (battery)
- (1) $1\ k\Omega$ resistor, (1) $100\ k\Omega$ resistor,
- (1) $0.1\ \mu F$ capacitor, (1) $10\ \mu F$ capacitor
- nMOS (FQP30N06L)
- (1) pushbutton

Resources

Datasheet of nMOS: https://cdn.sparkfun.com/datasheets/Components/General/FQP30N06L.pdf

Wikipedia on Time Constants: https://en.wikipedia.org/wiki/RC_time_constant

Notes:

Procedure

Let's start our design by investigating the RC portion of a circuit. Build the circuit in Figure 1.

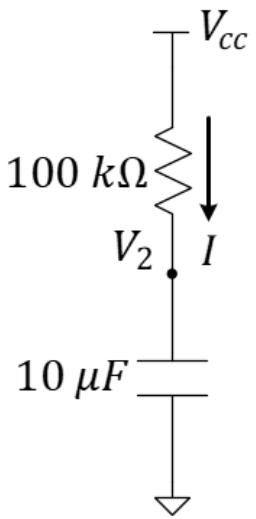

***Figure 1**: An "RC" circuit for investigating time constants.*

We can view the charging of the capacitor using an oscilloscope. The time constant, $\tau \approx (100k)(10\mu) = (0.1M)(10\mu) = (0.1)(10) = 1\ s$ such that the capacitor will charge (about 66% of the way to full charge) in about 1 second. Verify this by using channel 1 of your oscilloscope to view the voltage across the capacitor, V_2, as it charges. You can use a wire to momentarily short the capacitor (giving it a discharge path to ground) and upon its removal, you will see the capacitor charge again. You can also make discharging the capacitor easier by adding a button across the capacitor (see Figure 2). Be sure the orientation is correct that the capacitor is only shorted when the button is pressed.

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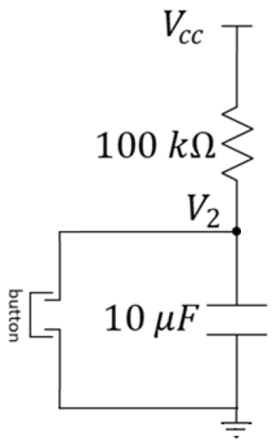

***Figure 2**: Addition of a button for visual observation of the capacitor's voltage.*

To leverage this circuit as a timed-response to a physical action, we can expand the circuit. Use a button to suddenly drain the capacitor when the button is pressed. After the button is released, the capacitor is allowed to charge again until the LED turns off. Build the circuit of Figure 3 and observe as the button drains the capacitor when pressed and the capacitor recharges after being released.

Figure 2 requires a physical interaction with a button sensor to trigger the timed reaction. How could we trigger the reaction with a response that comes from an arbitrary voltage signal like those produced by many sensors that are not mechanical buttons? This is where transistors excel. See Figure 3. We can use a MOSFET to suddenly drain the capacitor.

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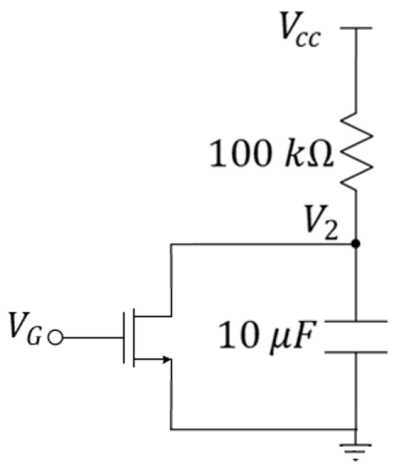

***Figure 3**: Replace the button with an nMOS transistor to quickly drain the capacitor's charge.*

When a voltage is applied to the gate of the nMOS, it suddenly turns on the transistor causing the drain and source to be nearly shorted. After the voltage at the gate is removed, the nMOS returns to cutoff and the capacitor is allowed to charge again until the LED turns off.

Build the circuit of Figure 3. Use an oscilloscope to monitor voltage V_2. Connect the battery to the power rails, then use a wire to connect V_G to the positive power rail. You should see that $V_2 \approx 0\ V$. When you disconnect the gate from the power rail, you will probably continue to see $V_2 \approx 0\ V$. Why? It's because the gate-to-source terminals behave like a small capacitor. This is shown in Figure 5 where the nMOS is replaced with a functional model (note that many devices have many models, the correct choice of model depends on how it is to be used and how accurate you want your model to represent real-life behavior). As long as that capacitor remains charged (and it currently has no strong discharge path) the transistor will remain on. We can fix this by adding a resistor ($10\ k\Omega$ will work well) between the gate and source terminals as shown in Figures 5 and 6.

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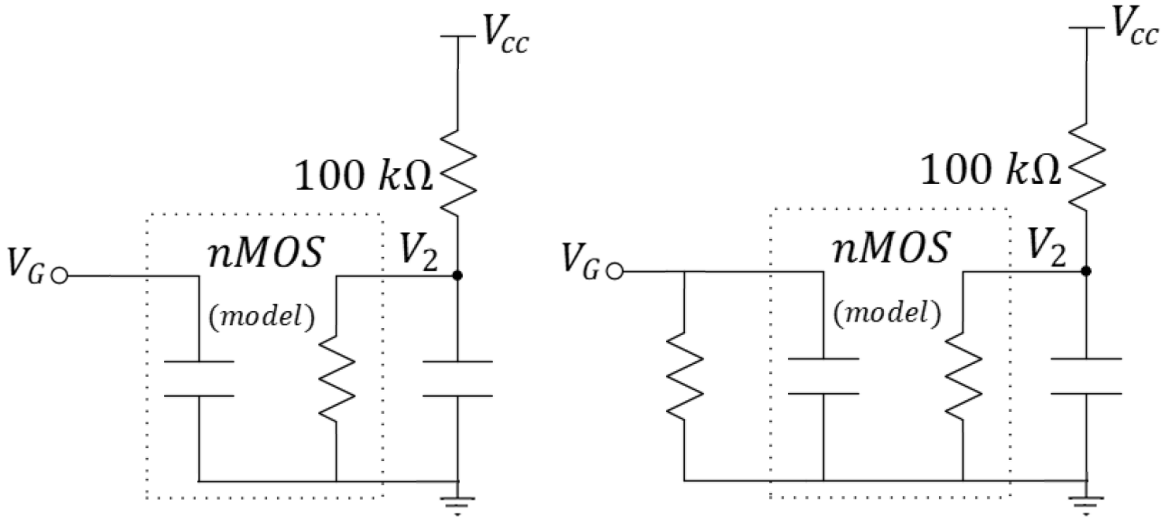

***Figure 5**: Addition of a resistor to allow discharge of the gate-to-source capacitance.*

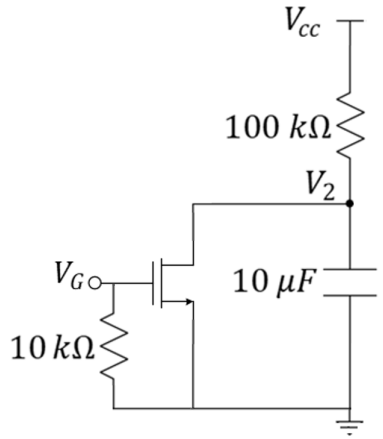

***Figure 6**: Addition of a $10\ k\Omega$ resistor to return the nMOS to its cutoff condition.*

The *pull-down* resistor keeps the transistor in cutoff by "pulling down" on the voltage at that node until the source driving V_G goes above the **th**reshold (turn-on) voltage of the nMOS transistor, V_{TH}. When V_G goes high, the transistor turns on draining the

Notes:

$10\ \mu F$ capacitor. When V_G falls low, the gate returns to ground voltage and the transistor returns to cutoff allowing the capacitor to recharge according to its time constant.

Question 1: Discuss the operation of the circuit of Figure 6.

Advanced Design

Build Figure 7 and test it using the oscilloscope to monitor the voltages across both capacitors (on two different channels). To excite the input, use a function generator (see Figure 8) with a square wave of 3 volts peak-to-peak, $1\ kHz$ frequency, 50% duty cycle, 1.5 volt offset, and High-Z parameter setting. You can find the input capacitance (looking into the gate of the MOSFET) from the datasheet listed as C_{iss}.

Question 2: What is the value of C_{iss}?

Question 3: What is the effect of adding the $0.1\ \mu F$ capacitor? That is, what capacitance will the input see at the gate of the MOSFET and what effect will adding the capacitor have on turning on the MOSFET?

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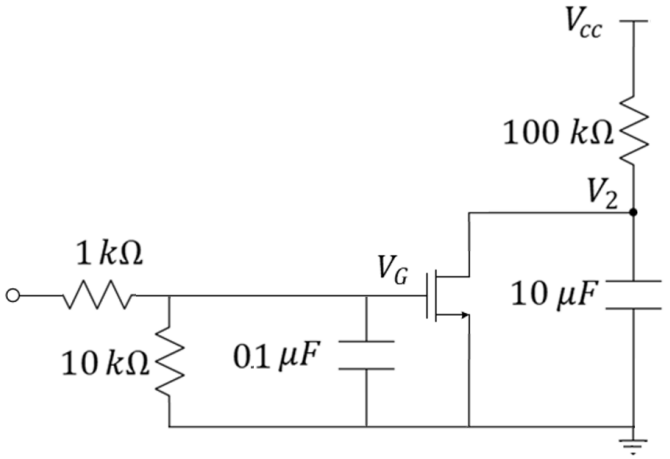

***Figure 7**: Further modification of the timed-reaction circuit.*

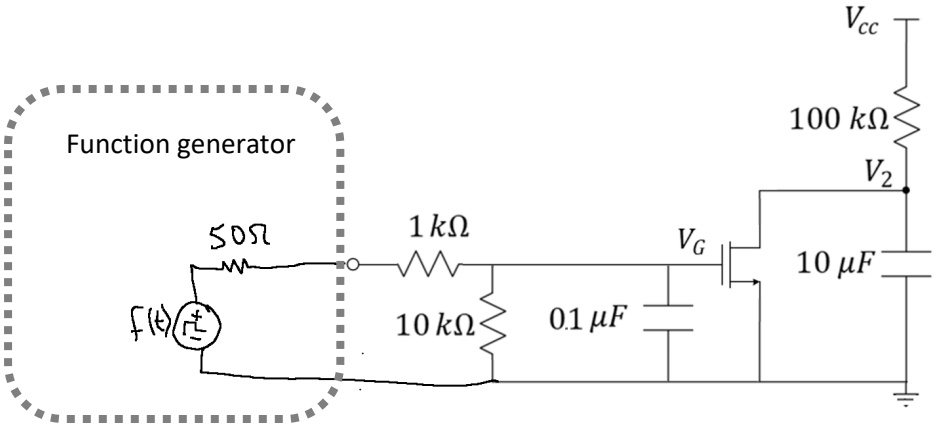

***Figure 8**: Driving the timed-reaction circuit with the function generator.*

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Question 4: While rise time for an RC circuit is given by $t_{rise} = 2.2RC$, the *time constant* is merely calculated $\tau = RC$. After the nMOS has been in cutoff (turned "off") for two "time constants" with respect to the $10\ \mu F$ capacitor, what will the voltage be across that $10\ \mu F$ capacitor? You can use the oscilloscope to find out.

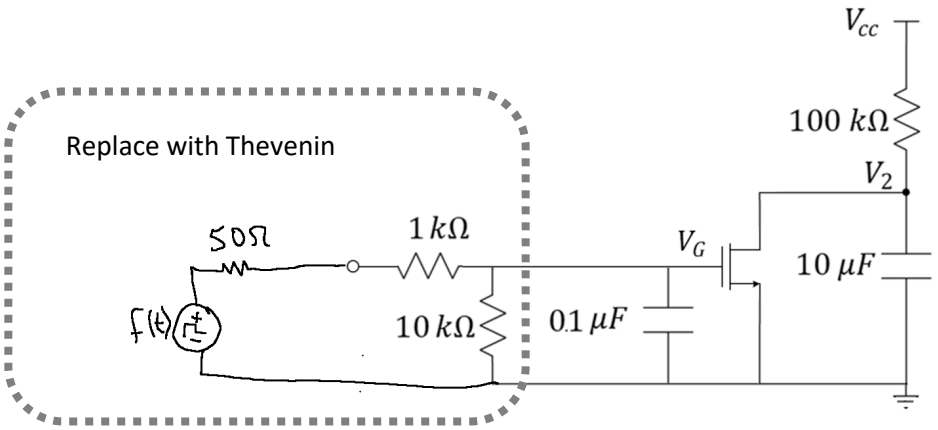

***Figure 8**: Driving the timed-reaction circuit with the function generator.*

Question 5: Determine the Thevenin equivalent of the boxed circuit in Figure 9. HINT: Treat $f(t)$ as you would any ideal voltage source as you did in class. You will need to find the new value of the ideal Thevenin-equivalent voltage source and you will need to find the Thevenin resistance.

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Question 6: Use the Thevenin model to discuss the operation of the circuit of Figure 9. Specifically, use R_T and your calculated capacitance seen at the gate of the MOSFET to estimate the charge and discharge times of the left side of the MOSFET. These will be directly proportional to the time it takes to turn on and off the MOSFET.

Question 7: What happens if you remove the $0.1\ \mu F$ capacitor?